Features

- Fast Read Access Time – 90 ns
- Low Power CMOS Operation
  - 100 µA Max Standby
  - 40 mA Max Active at 5 MHz
- JEDEC Standard Packages
  - 32-lead PLCC
  - 32-lead PDIP
  - 32-lead TSOP
- 5V ±10% Supply
- High-Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid Programming Algorithm – 50 µs/Byte (Typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Industrial Temperature Range
- Green (Pb/Halide-free) Packaging Option

8-Megabit (1M x 8) OTP EPROM

AT27C080

1. Description

The AT27C080 chip is a low-power, high-performance 8,388,608-bit one-time programmable read only memory (OTP EPROM) organized as 1M by 8 bits. The AT27C080 requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 90 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Atmel's scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 10 mA in active mode and less than 10 µA in standby mode.

The AT27C080 is available in a choice of packages, including; one-time programmable (OTP) plastic PLCC, PDIP and TSOP. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 1-Mbyte storage capability, the AT27C080 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

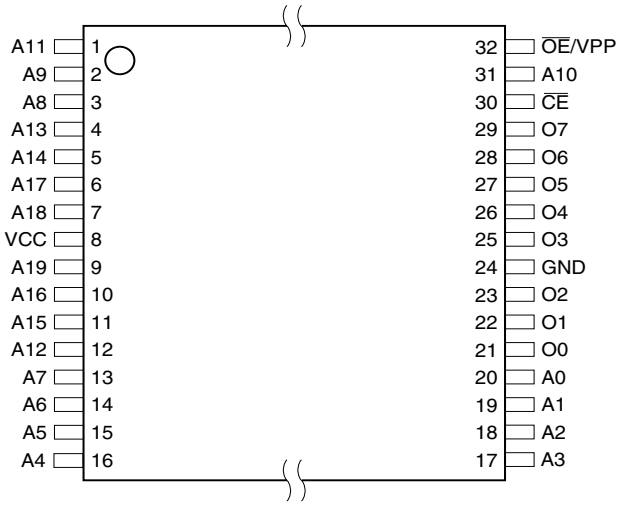
Atmel's AT27C080 has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

0360L–EPROM–12/07

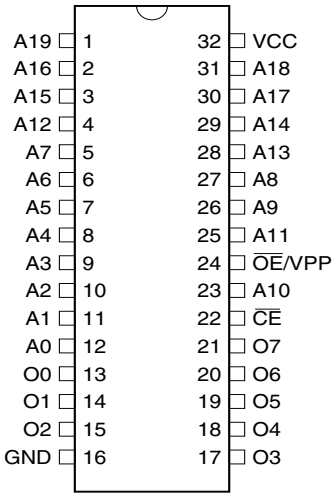
2. Pin Configurations

Pin Name	Function
A0 - A19	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$/VPP	Output Enable/Program Supply

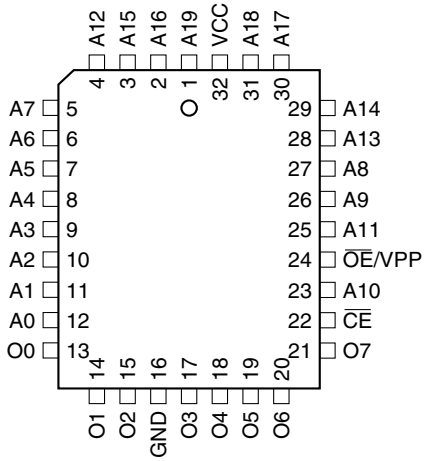
2.1 32-lead TSOP (Type 1) Top View



2.2 32-lead PDIP Top View



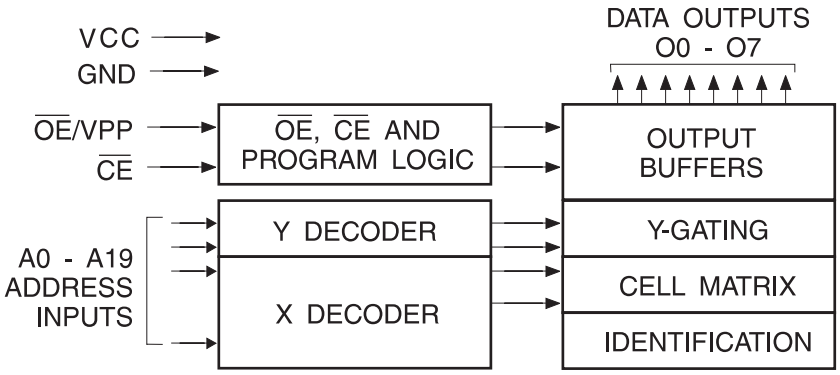
2.3 32-lead PLCC Top View



3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to +7.0V for pulses of less than 20 ns.

6. Operating Modes

Mode/Pin	$\overline{CE}$	$\overline{OE}/V_{PP}$	Ai	Outputs
Read	V_{IL}	V_{IL}	Ai	D_{OUT}
Output Disable	X	V_{IH}	X[1]	High Z
Standby	V_{IH}	X	X	High Z
Rapid Program[2]	V_{IL}	V_{PP}	Ai	D_{IN}
PGM Verify	V_{IL}	V_{IL}	Ai	D_{OUT}
PGM Inhibit	V_{IH}	V_{PP}	X	High Z
Product Identification[4]	V_{IL}	V_{IL}	A9 = V_H[3] A0 = V_{IH} or V_{IL} A1 - A19 = V_{IL}	Identification Code

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics.
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Operating Conditions for Read Operation

	AT27C080-90
Industrial Operating Temperature (Case)	-40° C - 85° C
V_{CC} Power Supply	5V ± 10%

8. DC and Operating Characteristics for Read Operation

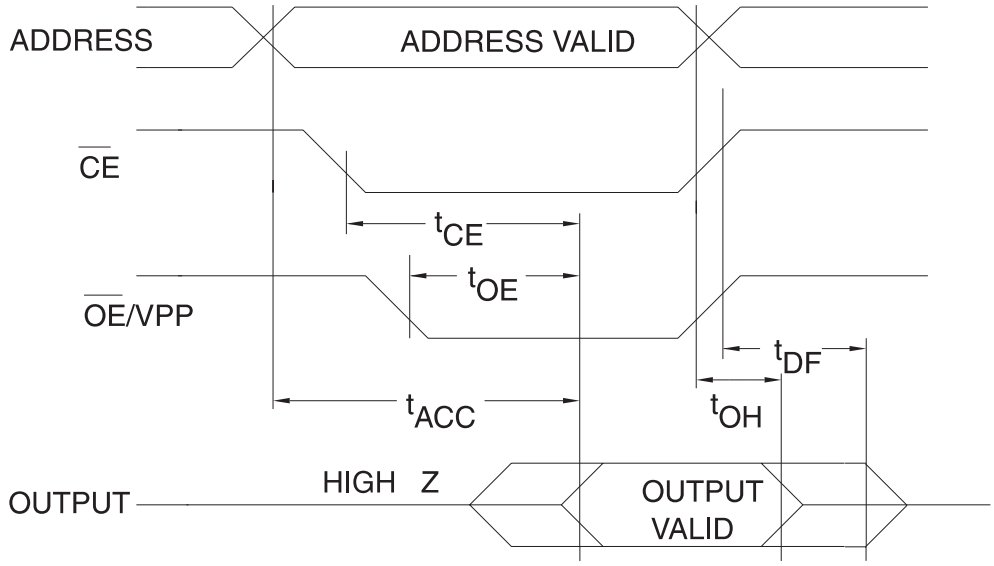
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} (Com., Ind.)		±1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC} (Com., Ind.)		±5.0	µA
I_{SB}	V_{CC}[1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ±0.3V		100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V		1.0	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}		40	mA
V_{IL}	Input Low Voltage		-0.6	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. V_{CC} must be applied simultaneously or before $\overline{OE}$/ V_{PP}, and removed simultaneously or after $\overline{OE}/V_{PP}$.

9. AC Characteristics for Read Operation

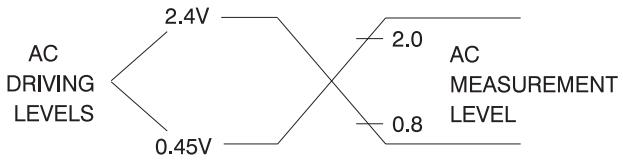
Symbol	Parameter	Condition	AT27C080-90		Units
			Min	Max	
t_{ACC}[4]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}/V_{PP}$ = V_{IL}		90	ns
t_{CE}[3]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		90	ns
t_{OE}[3][4]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20	ns
t_{DF}[2][5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			30	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}/V_{PP}$ whichever occurred first		0		ns

10. AC Waveforms for Read Operation[1]



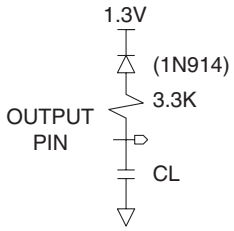
Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
2. t_{DF} is specified form $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first. Output float is defined as the point when data is no longer driven.
3. $\overline{OE}/V_{PP}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
4. $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
5. This parameter is only sampled and is not 100% tested.

11. Input Test Waveform and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

12. Output Test Load



Note: CL = 100 pF including jig capacitance.

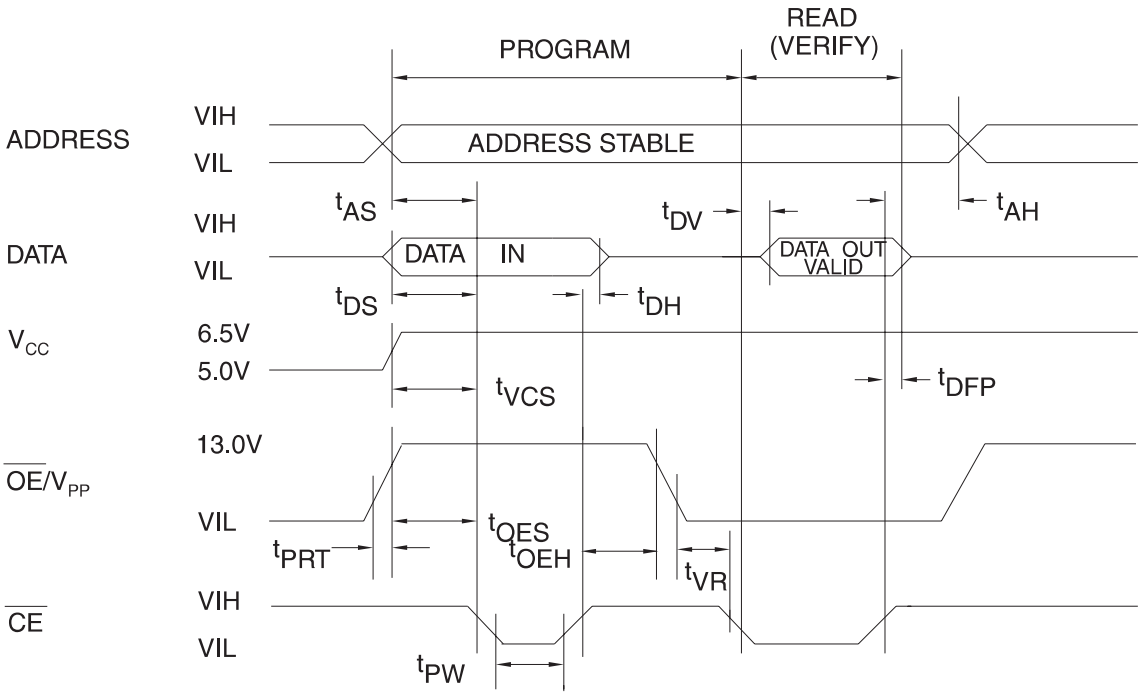
13. Pin Capacitance

f = 1 MHz, T = 25° C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms



Notes: 1. The Input Timing reference is 0.8V for V_{IL} and 2.0V for V_{IH}.

2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.

15. DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	$\overline{OE}/V_{PP}$ Supply Current	$\overline{CE} = V_{IL}$		25	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, $\overline{OE}/V_{PP}$ = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns Input Pulse Levels: 0.45V to 2.4V Input Timing Reference Level: 0.8V to 2.0V Output Timing Reference Level: 0.8V to 2.0V	2.0		µs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time		2.0		µs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time		2.0		µs
t_{DS}	Data SetupTime		2.0		µs
t_{AH}	Address Hold Time		0.0		µs
t_{DH}	Data Hold Time		2.0		µs
t_{DFP}	$\overline{CE}$ High to Output Float Delay[2]		0.0	130	ns
t_{VCS}	V_{CC} Setup Time		2.0		µs
t_{PW}	$\overline{CE}$ Program Pulse Width[3]		47.5	52.5	µs
t_{DV}	Data Valid from $\overline{CE}$			1.0	µs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time		2.0		ns
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time During Programming		50		ns

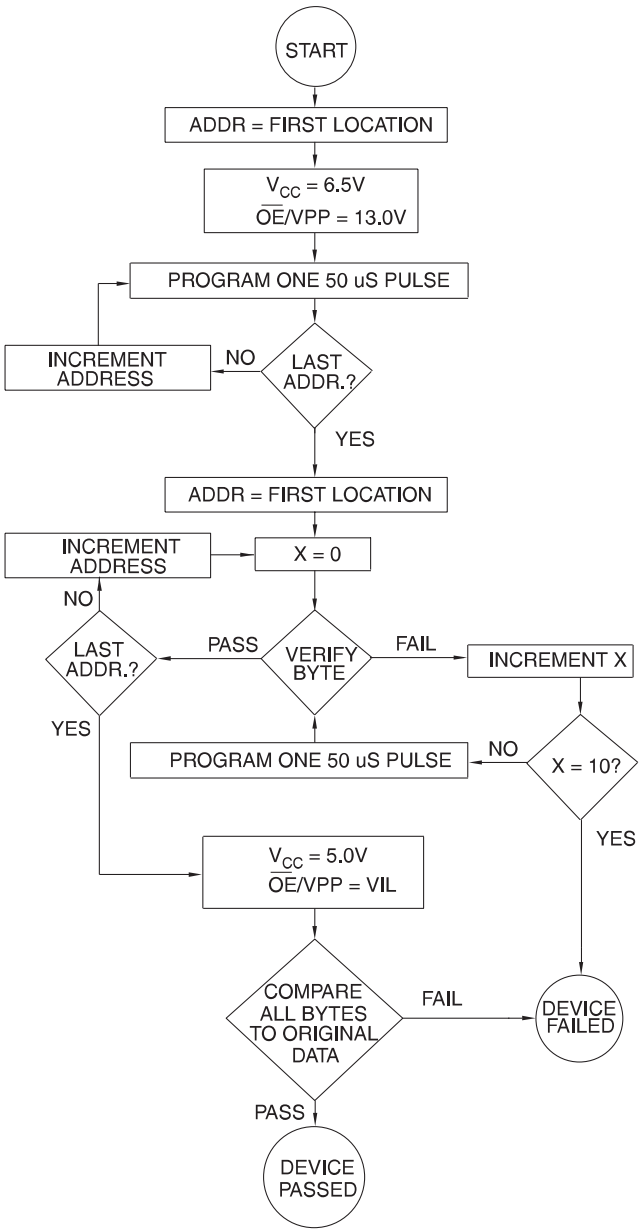
Notes:
1. V_{CC} must be applied simultaneously or before $\overline{OE}/V_{PP}$ and removed simultaneously or after $\overline{OE}/V_{PP}$.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
3. Program Pulse width tolerance is 50 µs ± 5%.

17. Atmel's AT27C080 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	0	1	0	8A

18. Rapid Programming Algorithm

A 50 µs $\overline{CE}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{OE}/V_{PP}$ is raised to 13.0V. Each address is first programmed with one 50 µs $\overline{CE}$ pulse without verification. Then a verification reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 50 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. $\overline{OE}/V_{PP}$ is then lowered to V_{IL} and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



19. Ordering Information

19.1 Standard Package

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	40	0.1	AT27C080-90JI AT27C080-90PI AT27C080-90TI	32J 32P6 32T	Industrial (-40° C to 85° C)

Note: Not recommended for new designs. Use Green package option.

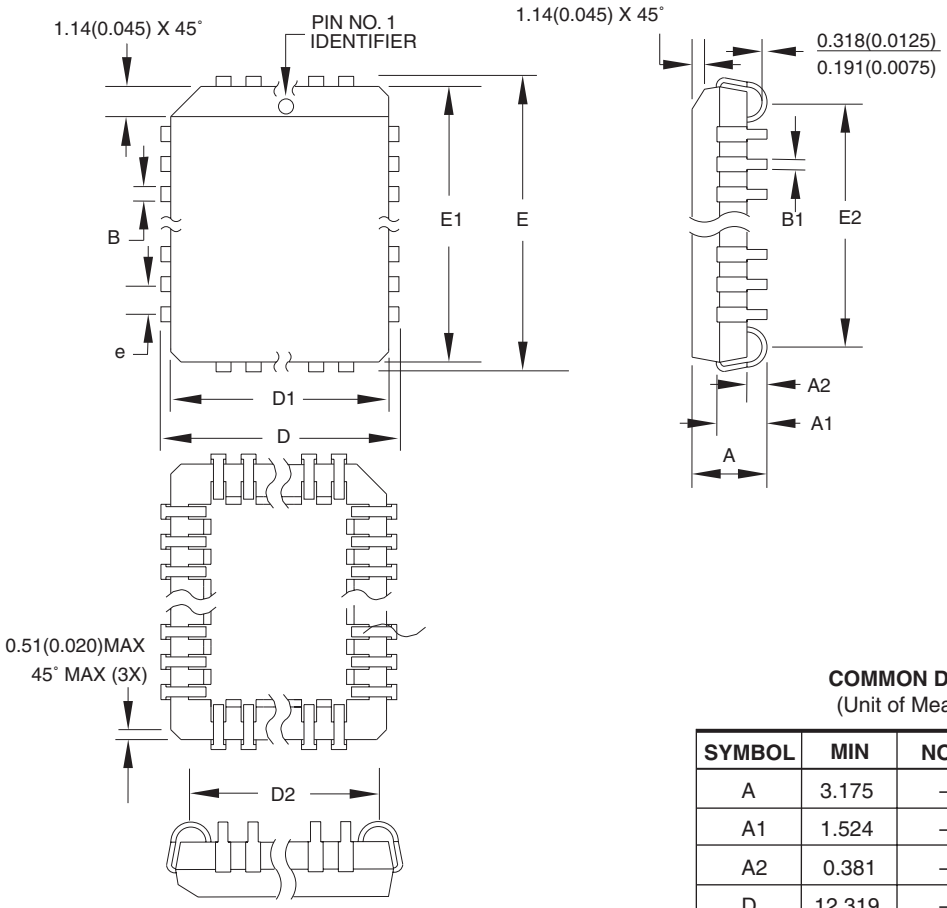
19.2 Green Package (Pb/Halide-free)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	40	0.1	AT27C080-90JU AT27C080-90PU AT27C080-90TU	32J 32P6 32T	Industrial (-40° C to 85° C)

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32P6	32-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
32T	32-lead, Plastic Thin Small Outline Package (TSOP)

20. Package Information

20.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

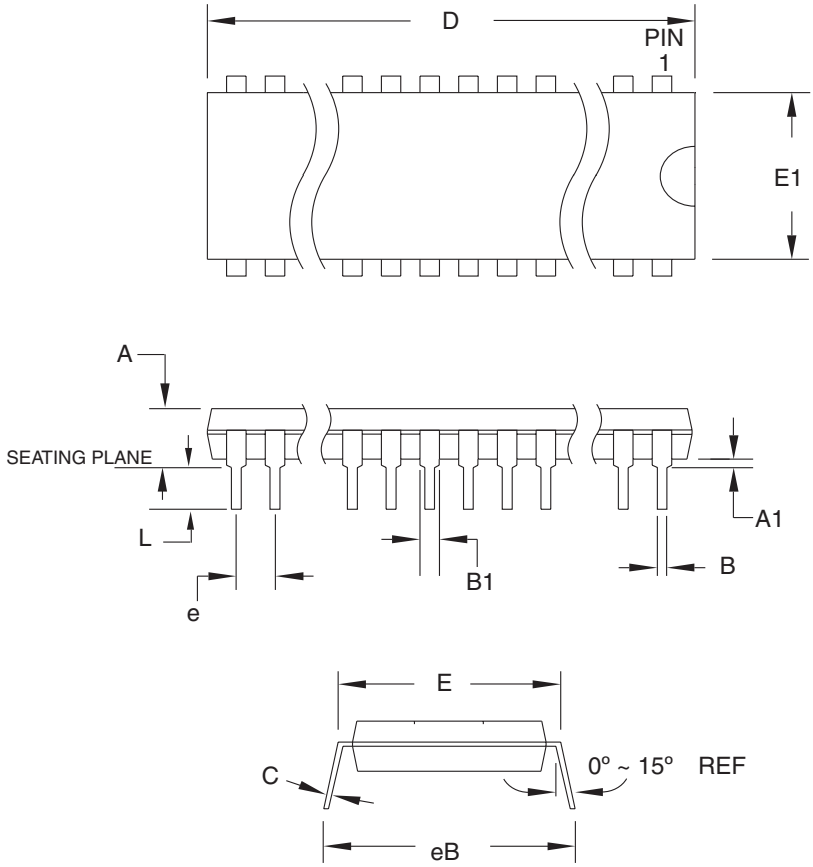
SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

20.2 32P6 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

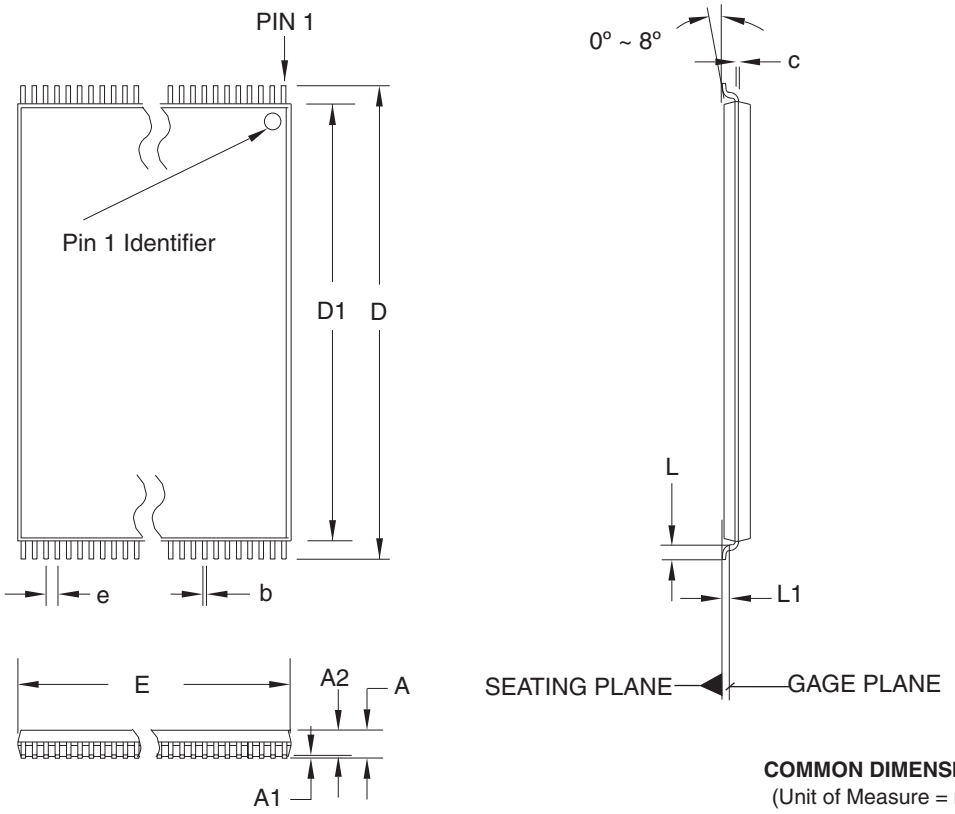
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	41.783	–	42.291	Note 1
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 1
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Note: 1. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32P6**, 32-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP)	32P6	B

20.3 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32T**, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	32T	B