Features

- **Single-voltage Operation**
  - **5V Read**
  - **5V Reprogramming**
- **Fast Read Access Time – 45 ns**
- **Internal Program Control and Timer**
- **8K Word Boot Block with Lockout**
- **Fast Erase Cycle Time – 1.5 seconds**
- **Word-by-word Programming – 10 µs/Word Typical**
- **Hardware Data Protection**
- **$\overline{\text{Data}}$ Polling for End of Program Detection**
- **Small 10 x 14 mm VSOP Package**
- **Typical 10,000 Write Cycles**

Description

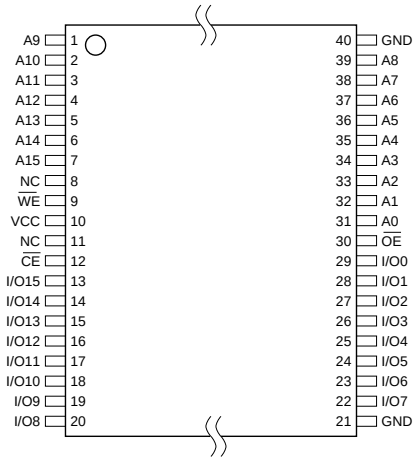
The AT49F1024A is a 5-volt-only in-system Flash memory organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the devices offer access times to 45 ns with power dissipation of just 275 mW over the commercial temperature range. When the device is deselected, the CMOS standby current is less than 100 µA.

To allow for simple in-system reprogrammability, the AT49F1024A does not require high-input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49F1024A is performed by erasing a block of data (entire chip or main memory block) and then programming on a word-by-word basis. The typical word programming time is a fast 10 µs. The end of a program cycle can be optionally detected by the $\overline{\text{Data}}$ Polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

Pin Configurations

Pin Name	Function
A0 - A15	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

VSOP Top View
Type 1
10 x 14 mm



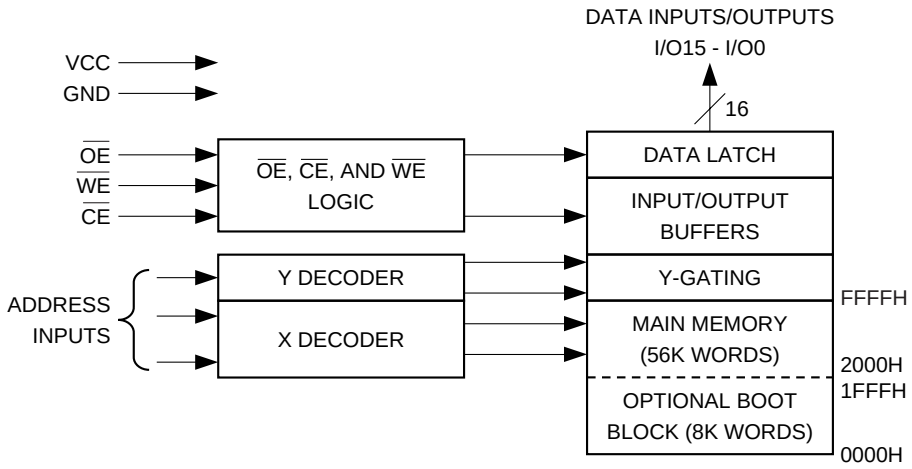
1-megabit (64K x 16) 5-volt Only Flash Memory

AT49F1024A

3415B–FLASH–12/03

The optional 8K word boot block section includes a reprogramming write lockout feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being erased or reprogrammed.

Block Diagram



Device Operation

READ: The AT49F1024A is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

CHIP ERASE: When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together from the same Chip Erase command (See Command Definitions table). If the boot block lockout function has been enabled, data in the boot section will not be erased. However, data in the main memory section will be erased. After a chip erase, the device will return to the read mode.

MAIN MEMORY ERASE: As an alternative to the chip erase, a main memory block erase can be performed, which will erase all words not located in the boot block region to an FFFFH. Data located in the boot region will not be changed during a main memory block erase. The Main Memory Erase command is a six-bus cycle operation. The address (555H) is latched on the falling edge of the sixth cycle while the 30H data input is latched on the rising edge of $\overline{WE}$. The main memory erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. Please see main memory erase cycle waveforms. The main memory erase operation is internally controlled; it will automatically time to completion.

WORD PROGRAMMING: Once the memory array is erased, the device is programmed (to a logic “0”) on a word-by-word basis. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is accomplished via the internal device command register and is a four-bus cycle operation (please refer to the Command Definitions table). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last, and the data latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The $\overline{Data}$ Polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write-protected region is optional to the user. The address range of the boot block is 0000H to 1FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method and can be erased using either the Chip Erase or the Main Memory Block Erase command. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections), a read from address location 0002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

$\overline{\text{DATA}}$ POLLING: The AT49F1024A features $\overline{\text{Data}}$ Polling to indicate the end of a program or erase cycle. During a program cycle, an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{\text{Data}}$ Polling, the AT49F1024A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F1024A in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

Command Definition (in Hex)

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	555	AA	AAA(2)	55	555	80	555	AA	AAA	55	555	10
Main Memory Erase	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	30
Word Program	4	555	AA	AAA	55	555	A0	Addr	D_{IN}				
Boot Block Lockout(3)	6	555	AA	AAA	55	555	80	555	AA	AAA	55	555	40
Product ID Entry	3	555	AA	AAA	55	555	90						
Product ID Exit(4)	3	555	AA	AAA	55	555	F0						
Product ID Exit(4)	1	xxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex).
   The ADDRESS FORMAT in each bus cycle is as follows: A11 - A0 (Hex); A11 - A15 (Don't Care).
2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
3. The 8K word boot sector has the address range 0000H to 1FFFH.
4. Either one of the Product ID Exit commands can be used.

Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F1024A-45
Operating Temperature (Case)	Com.	0°C - 70°C
V_{CC} Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High-Z
Program Inhibit	X	X	V_{IH}		
Program Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High-Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1 - A15 = V_{IL}, A9 = V_H[3], A0 = V_{IL}	Manufacturer Code[4]
				A1 - A15 = V_{IL}, A9 = V_H[3], A0 = V_{IH}	Device Code[4]
Software[5]				A0 = V_{IL}, A1 - A15 = V_{IL}	Manufacturer Code[4]
				A0 = V_{IH}, A1 - A15 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 001FH, Device Code: 0087H.
5. See details under “Software Product Identification Entry/Exit” on page 11.

DC Characteristics

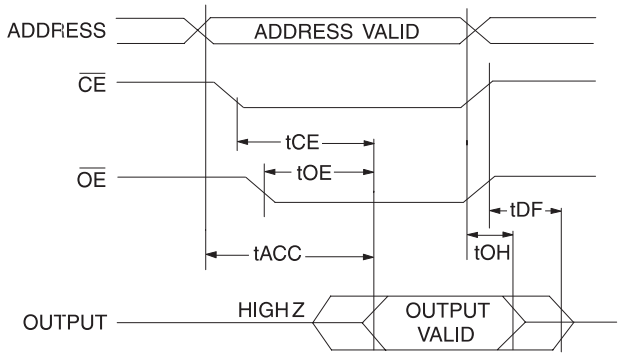
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10.0	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10.0	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		100.0	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1.0	mA
I_{CC} [1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50.0	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

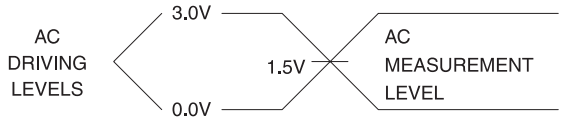
Symbol	Parameter	AT49F1024A-45		Units
		Min	Max	
t_{ACC}	Address to Output Delay		45	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		45	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	30	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		ns

AC Read Waveforms[1][2][3][4]



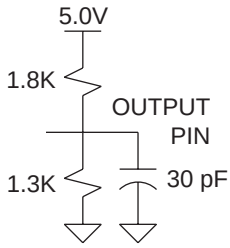
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

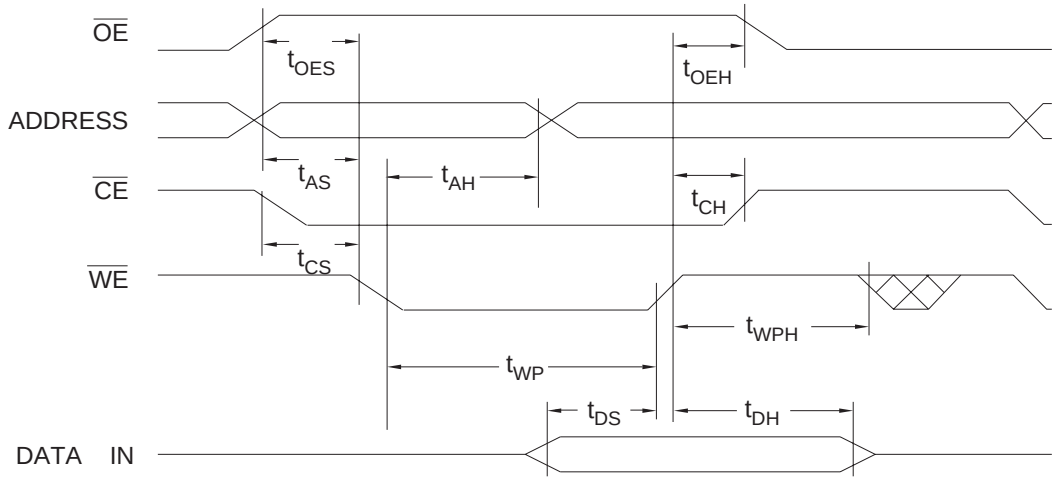
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

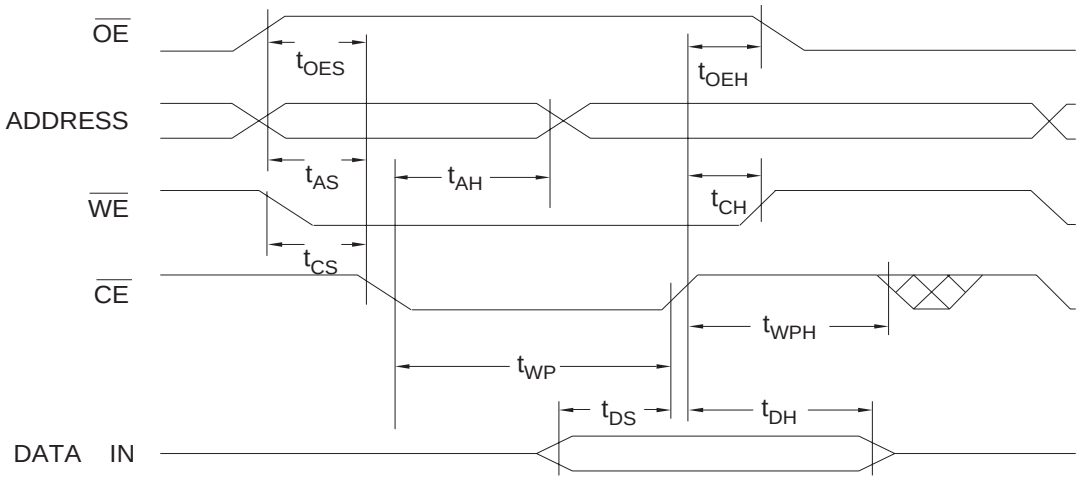
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	50		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	40		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



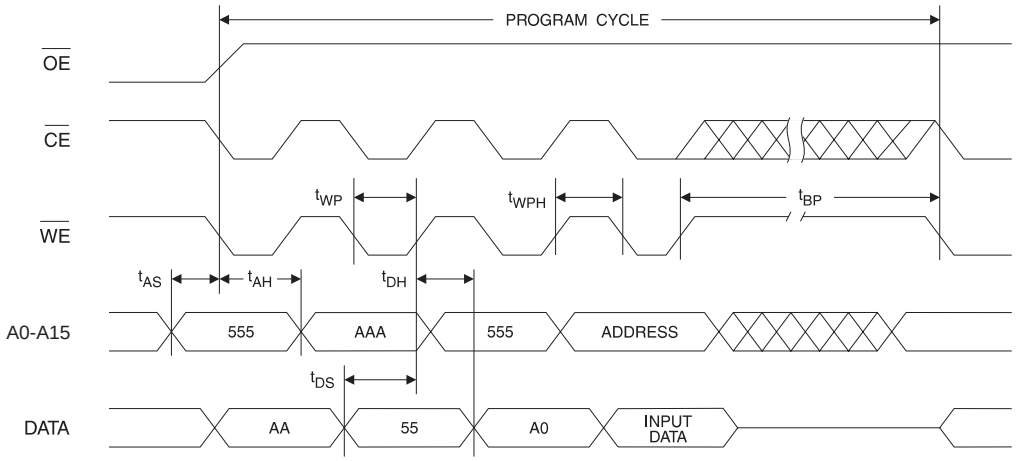
$\overline{CE}$ Controlled



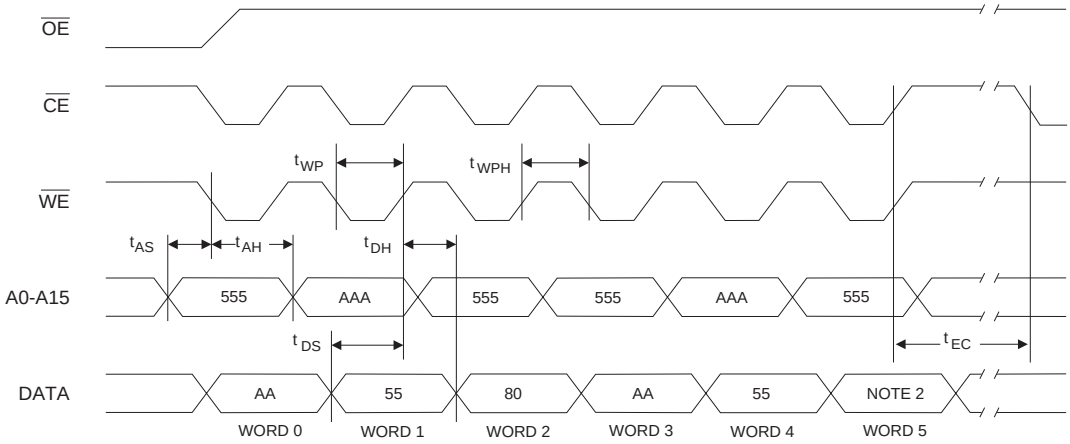
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Word Programming Time		10	50	µs
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Setup Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	50			ns
t_{WPH}	Write Pulse Width High	40			ns
t_{EC}	Erase Cycle Time		1.5	3	seconds

Program Cycle Waveforms



Main Memory or Chip Erase Cycle Waveforms



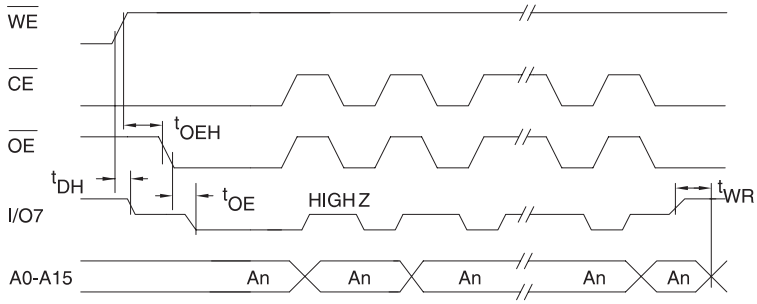
Notes: 1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 10H. For a main memory erase, the data should be 30H.

$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in “AC Read Characteristics” on page 6.

$\overline{\text{Data}}$ Polling Waveforms

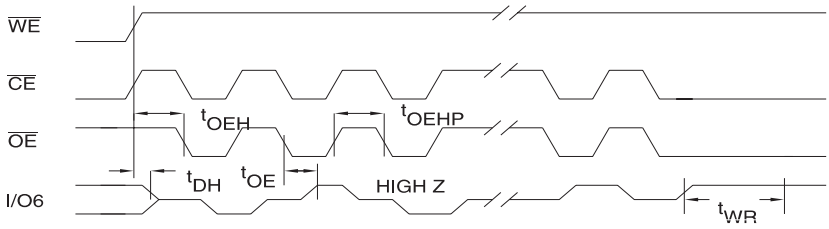


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

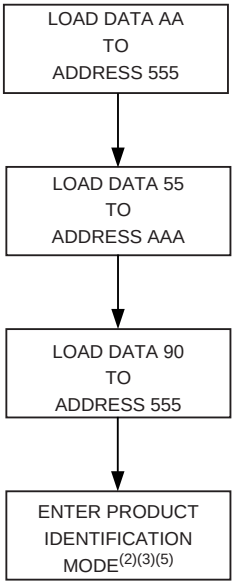
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in “AC Read Characteristics” on page 6.

Toggle Bit Waveforms(1)(2)(3)

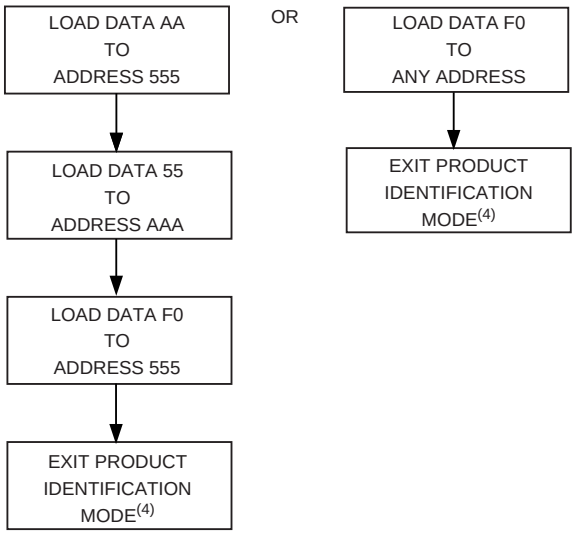


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

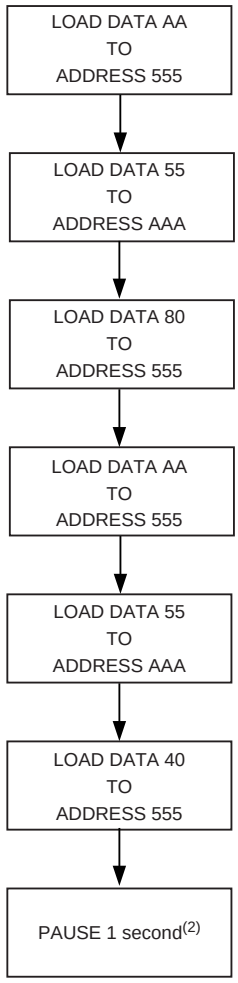


Software Product Identification Exit[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). Address Format: A11 - A0 (Hex); A11 - A15 (Don't Care).
2. A1 - A15 = V_{IL}.
   Manufacturer Code is read for A0 = V_{IL}.
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 001FH
   Device Code: 0087H

Boot Block Lockout Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex). Address Format: A11 - A0 (Hex); A11 - A15 (Don't Care).
2. Boot Block Lockout feature enabled.

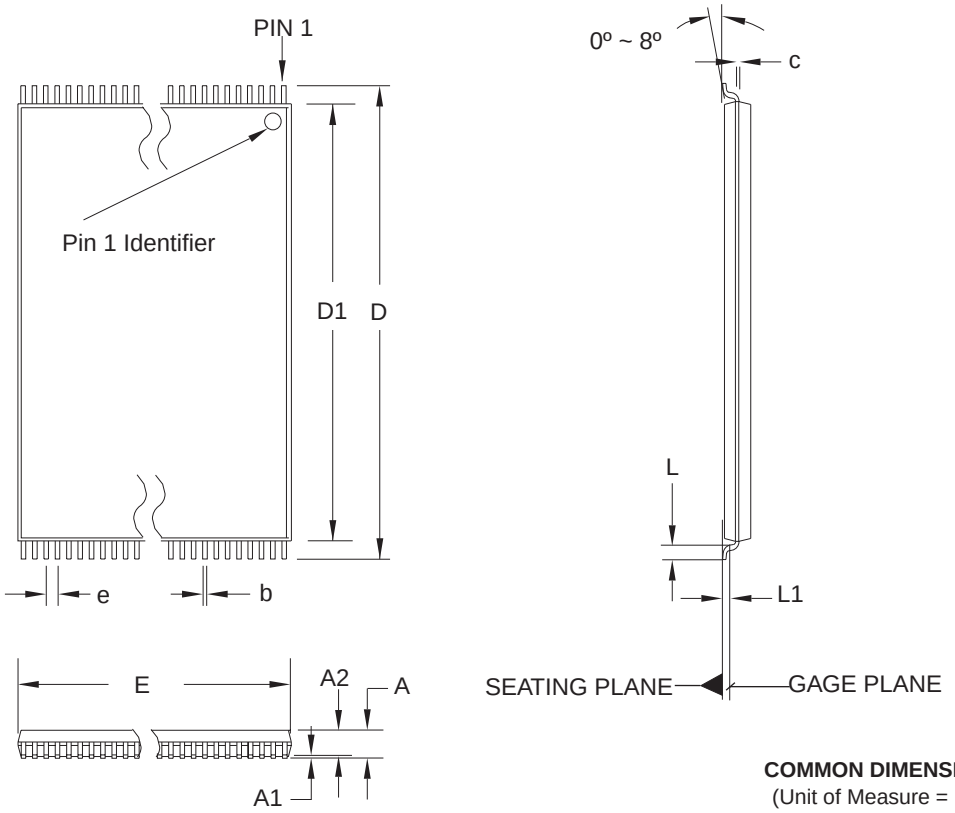
AT49F1024A Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	50	0.1	AT49F1024A-45VC	40V	Commercial (0° to 70° C)
45	50	0.1	AT49F1024A-45VL Lead Free	40V	Commercial (0° to 70° C)

Package Type	
40V	40-lead, 10 mm x 14 mm, Thin Small Outline Package (VSOP)

Packaging Information

40V – VSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	13.80	14.00	14.20	
D1	12.30	12.40	12.50	Note 2
E	9.90	10.00	10.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation CA.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40V**, 40-lead (10 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP)	40V	B