50mA Low-Noise Ultra Low-Dropout CMOS Regulator with $\overline{\text{Fault}}$ Indicator

DESCRIPTION

The EUP7182 low-noise, low-dropout, linear regulator operates from a 2.5V to 5.5V input and is guaranteed to deliver 50mA.
The EUP7182 is stable with small 1µF ceramic capacitor. Its performance suits battery powered applications because of its shutdown mode (60 nA typ), low quiescent current (110µA typ), and LDO voltage (110mV typ). The low dropout voltage allows for more utilization of a battery's available energy by operating closer to its end-of-life voltage. An output fault-detection circuit indicates loss of regulation.
The EUP7182 is available in SOT23-6 package with 1.8V, 2.5v, 2.8V, 3V and 3.3V versions.

FEATURE

- 2.5V to 5.5V Input Range
- 50mA Guaranteed Output Current
- 60dB PSRR at 1kHz
- 50µV RMS Output Voltage Noise (10Hz to 100kHz)
- 110mV Dropout at 50mA
- Low 110µA No-Load Supply Current
- ≤1µA Shutdown Current
- Fast Start-up Time
- Stable With 1µF Ceramic Output Capacitors
- Thermal Shutdown and Short-Circuit Protection
- Fault Indicator
- RoHS Compliant and 100% Lead (Pb)-Free

APPLICATIONS

- Wireless Handsets
- Battery Powered Electronics
- Portable Information Appliances

Block Diagram

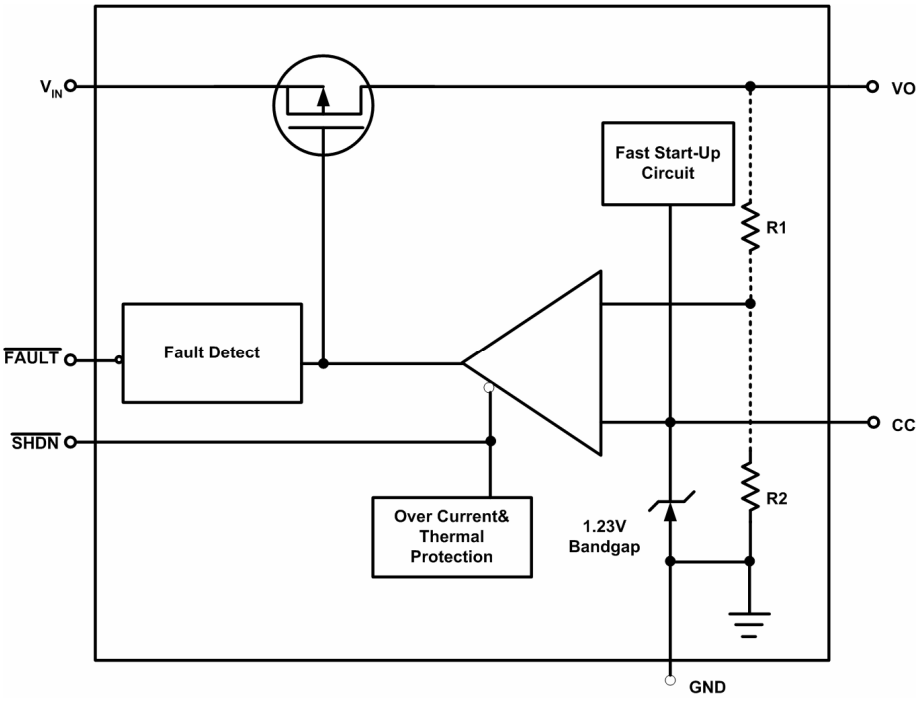


Figure1.

Typical Application Circuit

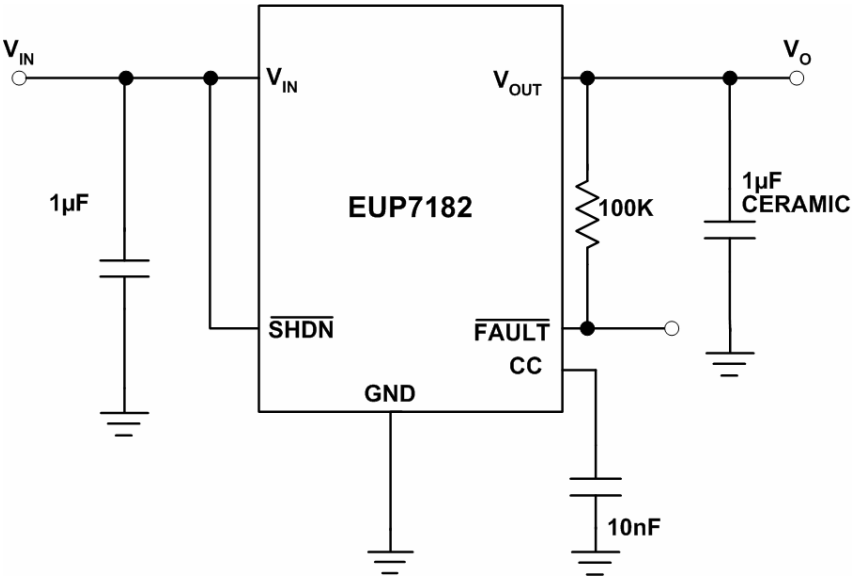
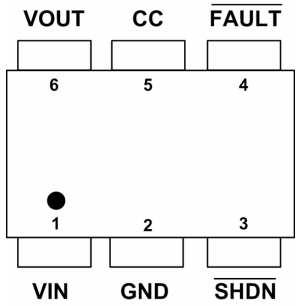


Figure2. Fixed Voltage LDO Regulator

Pin Configurations

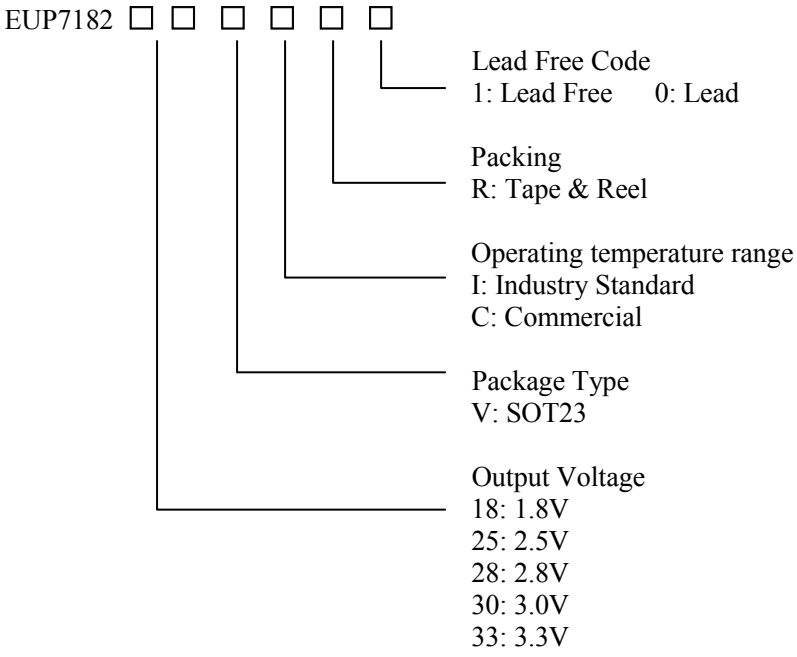
Package Type	Pin Configurations
SOT23-6	

Pin Description

PIN	PIN	DESCRIPTION
VIN	1	Input voltage of the LDO
GND	2	Common Ground
$\overline{SHDN}$	3	$\overline{SHDN}$ places the entire device in shutdown mode when held low.
$\overline{FAULT}$	4	Fault output. A high-impedance, open-drain output. If the circuit is out of regulation, $\overline{FAULT}$ goes low. In shutdown, this pin is high Impedance. Connect to GND if unused
CC	5	Compensation capacitor for noise reduction
VOUT	6	Output voltage of the LDO

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUP7182-18VIR1	SOT23-6	mDxxxx	-40°C to 85°C
EUP7182-25VIR1	SOT23-6	mBxxxx	-40°C to 85°C
EUP7182-28VIR1	SOT23-6	mExxxx	-40°C to 85°C
EUP7182-30VIR1	SOT23-6	mGxxxx	-40°C to 85°C
EUP7182-33VIR1	SOT23-6	mHxxxx	-40°C to 85°C



Absolute Maximum Ratings

- V_{IN}, V_{OUT}, $V_{\overline{SHDN}}$, V_{CC}, $V_{\overline{FAULT}}$ ---------- -0.3V to 6V
- Fault Sink Current ---------- 20mA
- Storage Temperature Range ---------- -65°C to 160°C
- Junction Temperature (TJ) ---------- 150°C
- Lead Temperature (10 sec.) ---------- 260°C

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V_{IN}= V_O +0.5V, $V_{\overline{SHDN}}$=V_{IN}, C_{IN}=C_{OUT}=1μF, C_{CC}=10nF, T_J =25°C. (Boldface limits apply for the operating temperature extremes: -40°C and 85°C)

Symbol	Parameter	Conditions	EUP7182			Unit
			Min	Typ	Max.	
V_{IN}	Input Voltage		**2.5**		**5.5**	V
ΔV_O	Output Voltage Tolerance	100μA ≤ I_{OUT} ≤ 50mA V_{IN}=V_O+0.5V,	-2		+2	% of $V_{OUT(NOM)}$
			-3		**+3**	
I_O	Maximum Output Current	Average DC Current Rating	**50**		**100**	mA
I_{LIMIT}	Output Current Limit			75	100	mA
I_Q	Supply Current	I_{OUT}=0mA		110	**200**	μA
	Shutdown Supply Current	V_O =0V, $\overline{SHDN}$ =GND		0.06	1	μA
V_{DO}	Dropout Voltage	I_{OUT} =1mA		1		mV
		I_{OUT} =50mA		110	**160**	
ΔV_O	Line Regulation	I_{OUT} = 1mA, (V_O +0.5V) ≤ V_I ≤ 5.5V	**-0.1**	0.05	**0.1**	%/V
	Load Regulation	100μA ≤ I_{OUT} ≤ 50mA		0.002		%/mA
e_n	Output Voltage Noise	I_{OUT} =10mA, 10Hz ≤ f ≤ 100kHz		50		μV_{RMS}
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{IH},(VO+0.5V) ≤ V_I ≤ 5.5V	2			V
		V_{IL},(VO+0.5V) ≤ V_I ≤ 5.5V			**0.4**	
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ =GND or IN		0.1	100	nA
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Detection Voltage of the V_{IN}-to-V_{OUT} Difference (Apply for V_{OUT} ≥ 2.5V and I_{OUT} ≤ 15mA)	I_{OUT} =10mA		25	**40**	mV
	$\overline{FAULT}$ Detection Threshold of the Output Voltgae			0.8×V_{OUT}		V
	$\overline{FAULT}$ Output Low Voltage	I_{SINK}=2mA		0.13	**0.25**	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Off-Leakage Current	$\overline{FAULT}$ =3.6V, $\overline{SHDN}$ =0V		0.1	100	nA
T_{SD}	Thermal Shutdown Temperature			160		°C
	Thermal Shutdown Hysteresis			20		
T_{ON}	Start-Up Time	V_O at 90% of Final Value		80		μs

Application Information

External Capacitors

Like any low-dropout regulator, the EUP7182 requires external capacitors for regulator stability. The EUP7182 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

Input Capacitor

A minimum input capacitance of 1μF is required between the EUP7182 input pin and ground (the amount of the capacitance may be increased without limit).This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground.

1μF ceramic capacitor are fine for most end use applications. If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

No-Load Stability

The EUP7182 will remain stable and in regulation with no external load. This is specially important in CMOS RAM keep-alive applications.

Output Capacitance

The EUP7182 is specifically designed to employ ceramic output capacitors as low as 2.2μF. Ceramic capacitors below 10μF offer significant cost and space savings, along with high frequency noise filtering. Higher values and other types and of capacitor may be used, but their equivalent series resistance (ESR) should be maintained below 0.5Ω. Ceramic capacitor of the value required by the EUP7182 are available in the following dielectric types: Z5U, Y5V, X5R, and X7R. The Z5U and Y5V types exhibit a 50% or more drop in capacitance value as their temperature increase from 25°C, an important consideration. The X5R generally maintain their capacitance value within ± 20%. The X7R type are desirable for their tighter tolerance of 10% over temperature.

Noise Bypass Capacitor

Connecting a 33nF capacitor between the C_{BYPASS} pin and ground significantly reduces noise on the regulator output. This cap is connected directly to a high impedance node in the bandgap reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy. The types of capacitors best suited for the noise bypass capacitor are ceramic and film.

Unlike many other LDO's , addition of a noise reduction capacitor does not effect the load transient response of the device. However, it does affect start-up time. The smaller the capacitance value, the quicker the start-up time.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D=(V_I-V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Fault Detection

The EUP7182 provides a $\overline{\text{FAULT}}$ pin that goes low during out of regulation conditions like current limit and thermal shutdown, or when it approaches dropout. The latter monitors the input-to-output voltage differential and compares it against a threshold that is slightly above the dropout voltage. This threshold also tracks the dropout voltage as it varies with load current. Refer to Fault Detect vs. Load Current curve in the typical characteristics section.

The $\overline{\text{FAULT}}$ pin requires a pull-up resistor since it is an open-drain output. This resistor should be large in value to reduce energy drain. A100kΩ pull-up resistor works well for most applications.

Shutdown

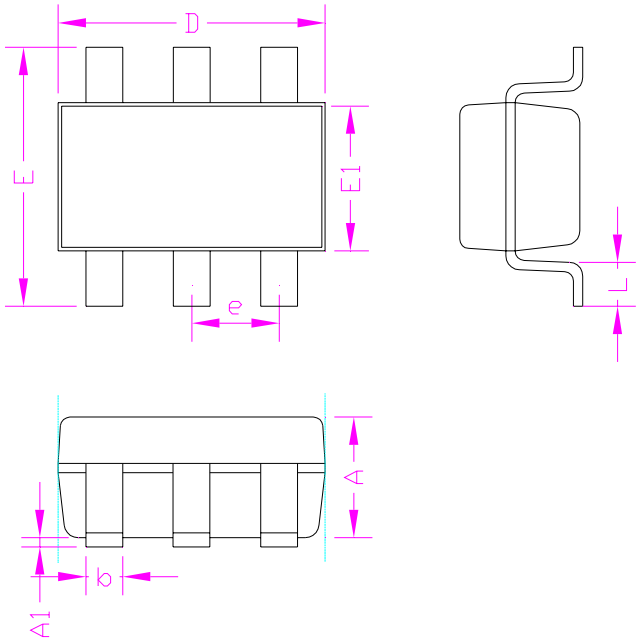
The EUP7182 goes into sleep mode when the $\overline{\text{SHDN}}$ pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 60nA typical. The $\overline{\text{SHDN}}$ pin may be directly tied to V_{IN} to keep the part on.

Fast Start-up

The EUP7182 provides fast start-up time for better system efficiency. The start-up speed is maintained when using the optional noise bypass capacitor.

Packaging Information

SOT23-6



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.45	-	0.057
A1	0.00	0.15	0.000	0.006
b	0.30	0.50	0.012	0.020
D	2.90		0.114	
E1	1.60		0.063	
e	0.95		0.037	
E	2.60	3.00	0.102	0.118
L	0.30	0.60	0.012	0.024