

1.5A DDR Termination Regulator

DESCRIPTION

The EUP7996 is a high performance linear regulator designed to provide power for termination of a DDR memory bus. It significantly reduces parts count, board space and overall system cost over previous switching solutions.

The EUP7996 contains a high-speed operational amplifier to provide excellent response to load transients. The EUP7996 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for chipset and DIMMs.

An additional feature found on the EUP7996 is an active low shutdown (SD) pin. When SD is pulled low the V_{TT} output will Tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

The EUP7996, used in conjunction with series termination resistors, provides an excellent voltage source for active termination schemes of high speed transmission lines as those seen in high speed memory buses. A typical DDR memory system is seen in Figure 1.

FEATURES

- Extremely low quiescent current (305uA)
- Fast transient response time
- Capable of sourcing and sinking 1.5A for DDR-I termination
- Reference out for other memory and control components
- Low-current shutdown mode
- Over-temperature protection
- High accuracy output voltage at full-load
- Low external component count
- Available in SOP-8, SOP(FD) package
- RoHS compliant and 100% lead (Pb)-free

APPLICATIONS

- DDR-I and DDR-II termination voltage

SIMPLIFIED SYSTEM DIRGRAM

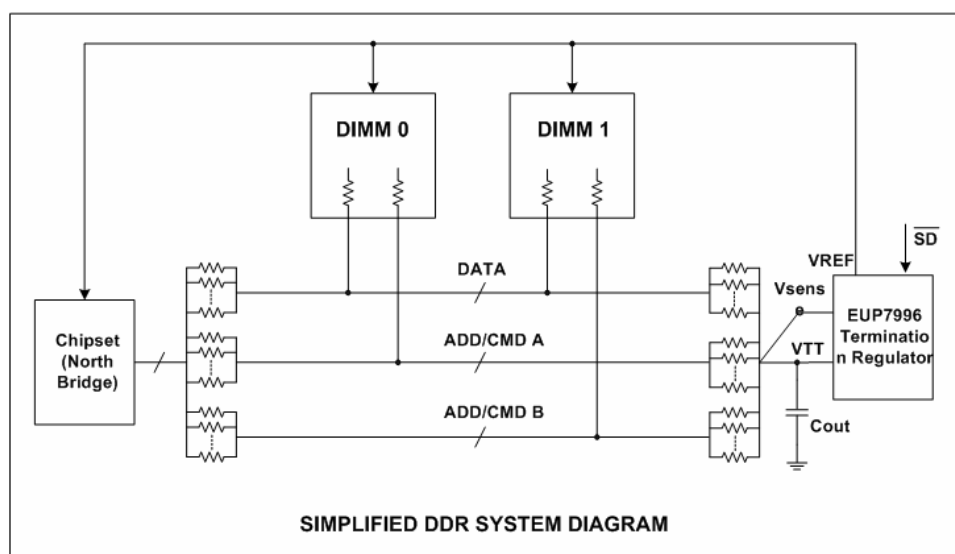


Figure 1.

Pin Configurations

Package Type	Pin Configurations (TOP VIEW)
Plastic SOP-8(FD)* * Thermal Pad	

Pin Description

PIN	SYMBOL	DESCRIPTION
1	GND	Ground
2	SD	Shutdown
3	VSENSE	Feedback pin for regulating V_{TT}
4	VREF	Buffered internal reference voltage of $V_{DDQ}/2$
5	VDDQ	Input for internal reference equal to $V_{DDQ}/2$
6	AVIN	Analog input pin
7	PVIN	Power Input pin
8	VTT	Output voltage for connection to termination resistors

Typical Application Circuit

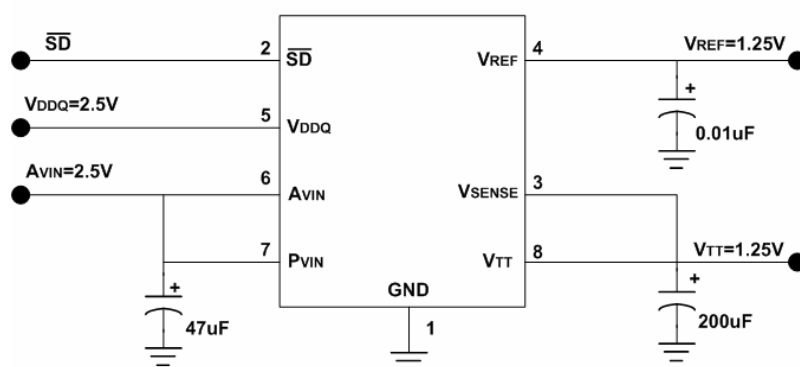


Figure 2. Recommended DDR-I Termination

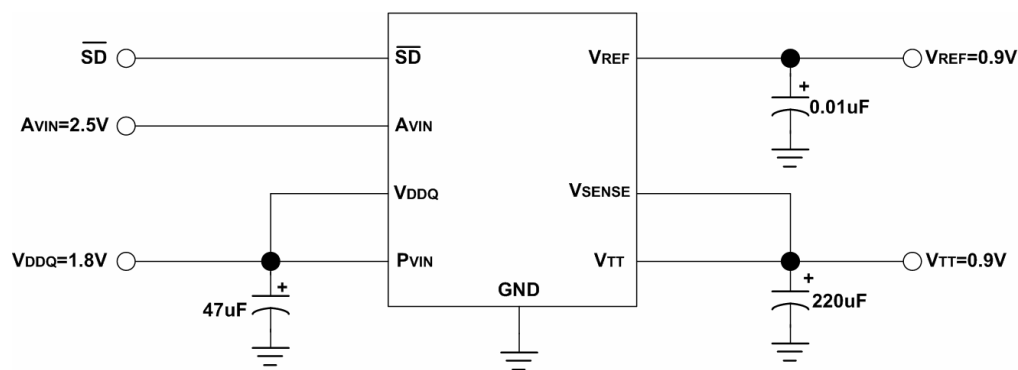


Figure 3. Recommended DDR-II Termination

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUP7996ADIR1	SOP-8	 Xxxx EUP7996 A	-40 °C to 125°C
EUP7996ADIR0	SOP-8	 Xxxx EUP7996 A	-40 °C to 125°C

EUP7996A □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
D: SOP

Absolute Maximum Ratings

Operating Range

■ Input voltage	----- 6V	■ Junction Temp. Range	----- -40°C to 125°C
■ Power dissipation	----- Internal limiting	■ AVIN to GND	----- -1.8V to 5.5V
■ ESD rating	----- 3KV	■ PVIN, VDDQ to GND	----- 1.8V to AVIN
■ Maximum junction temperature	----- 150 °C	■ SD Input Voltage	----- 0 to AVIN
■ Storage temperature range	----- -65°C to 150°C		
■ Lead temperature (soldering , 5 sec)	-- 260 °C		
■ SOP-8 thermal resistance, θ_{JA}	----- 67.9 °C/W		
■ SOP-8(FD) thermal resistance, θ_{JA}	---- 42.3 °C/W		

Electrical Characteristics

Specifications with standard typeface are for $T_A=25^\circ\text{C}$, unless otherwise specified, $AVIN=2.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage	$I_{REF}=0mA$ $PVIN=VDDQ=2.5V$ $PVIN=VDDQ=1.8V$	1.235 0.886	1.242 0.899	1.285 0.914	V
V_{TT}	V_{TT} Output Voltage	$PVIN=VDDQ=2.5V$ $I_{OUT}=0A$ $I_{OUT}=\pm 1.5A$	1.225 1.225	1.251 1.251	1.290 1.290	V
		$PVIN=VDDQ=1.8V$ $I_{OUT}=0A$ $I_{OUT}=\pm 0.9A$	0.885 0.885	0.892 0.892	0.915 0.915	V
V_{OS}	Output Offset Voltage	$PVIN=VDDQ=2.5V$ $I_{OUT}=0A$ $I_{OUT}=-1.5A$ $I_{OUT}=+1.5A$	-20 -25 -25	0 0 0	20 25 25	mV
		$PVIN=VDDQ=1.8V$ $I_{OUT}=0A$ $I_{OUT}=-1A$ $I_{OUT}=+0.9A$	-15 -20 -20	0 0 0	15 20 20	mV
I_Q	Quiescent Current (Note 2)	$I_{OUT}=0A$	200	305	500	μA
I_{SHDN}	Quiescent Current in Shutdown	$SD=0V$	50	75	200	μA
I_{LKG_SD}	Shutdown leakage current	$SD=0V$	--	0.16	--	μA
I_V	V_{TT} Leakage Current in Shutdown	$SD=0V$, $V_{TT}=1.25V$	--	0.13	--	μA

Over Temperature Protection

T_{SD}	Thermal Shutdown Temperature	Guaranteed by design	--	155	--	$^\circ C$
T_{SD_HYS}	Thermal Shutdown Hysteresis	Guaranteed by design	--	30	--	$^\circ C$

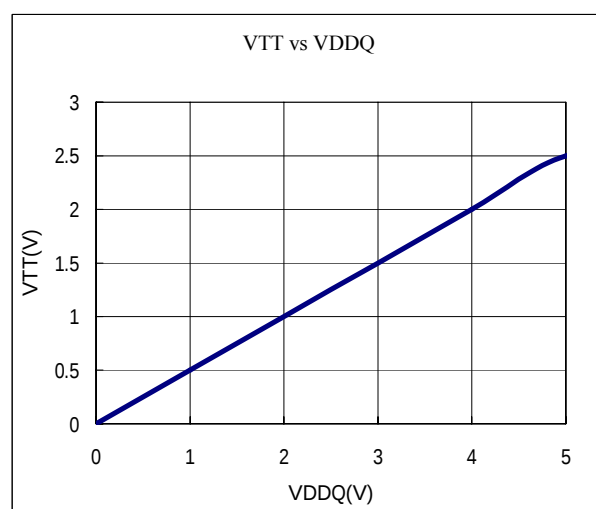
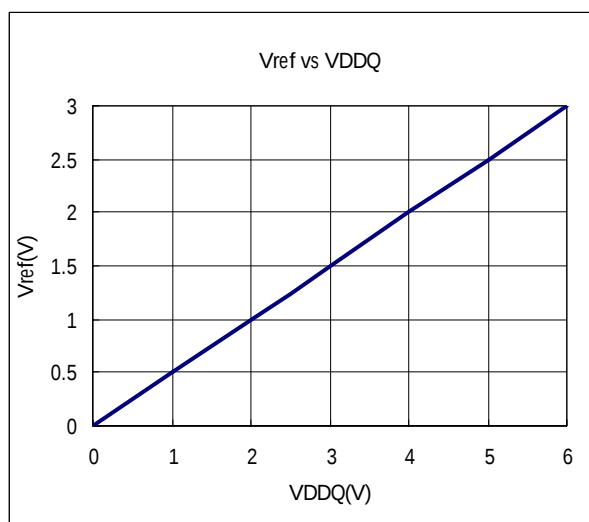
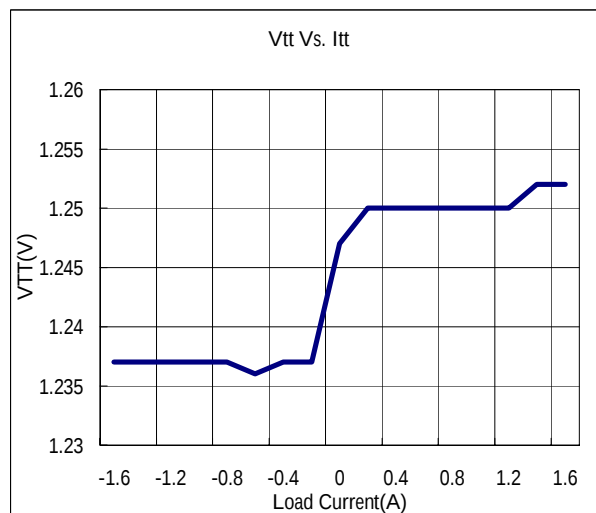
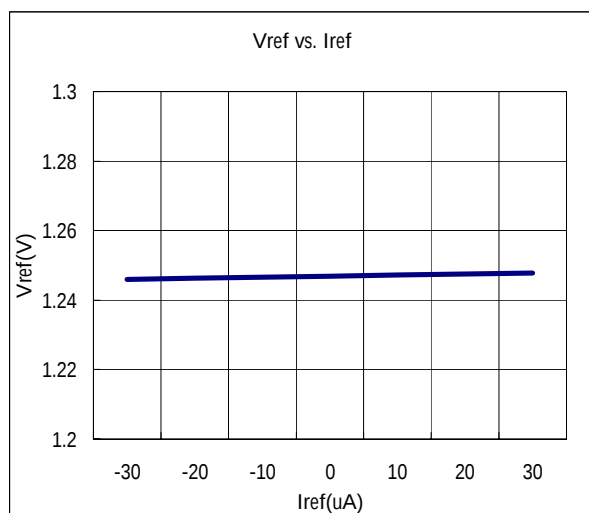
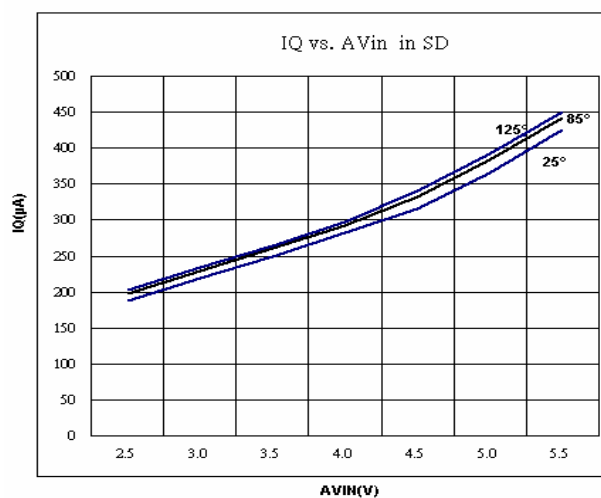
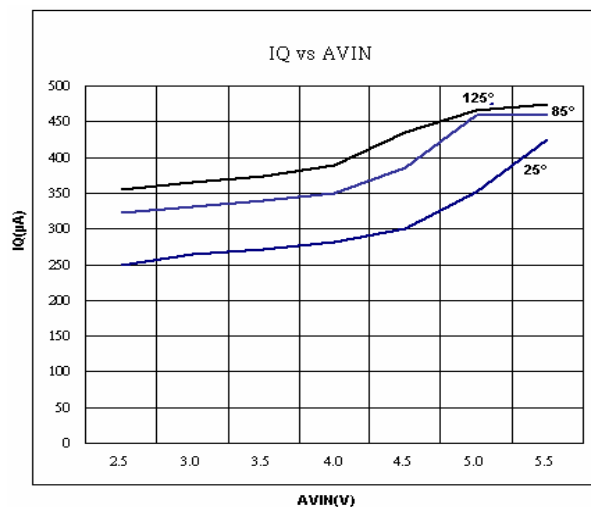
Shutdown function

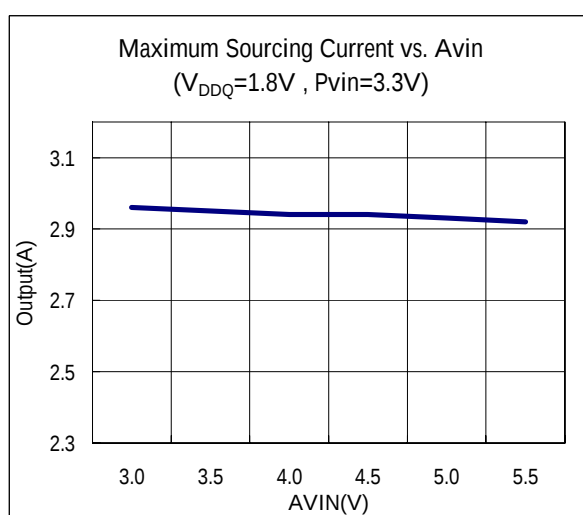
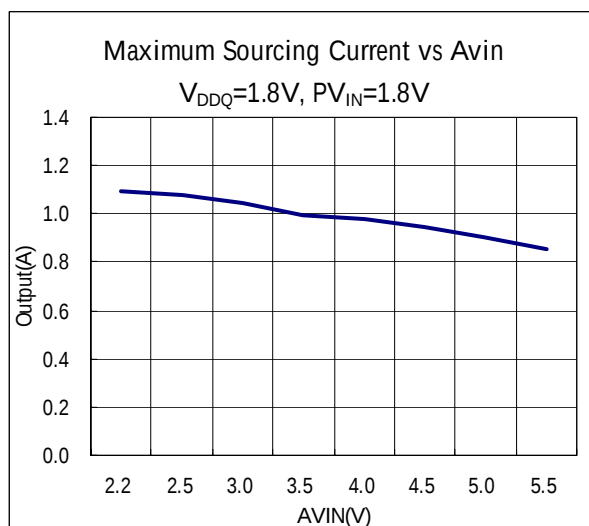
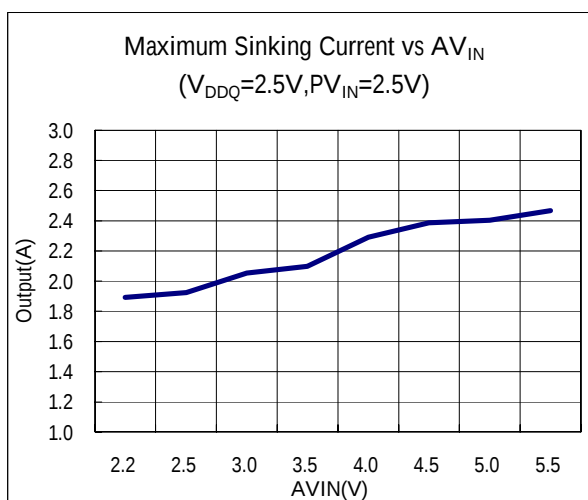
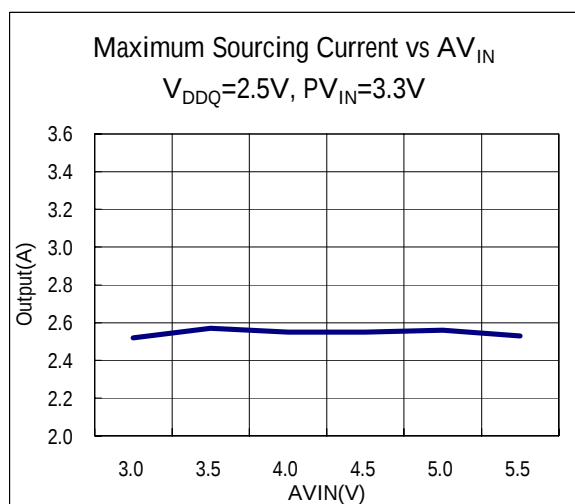
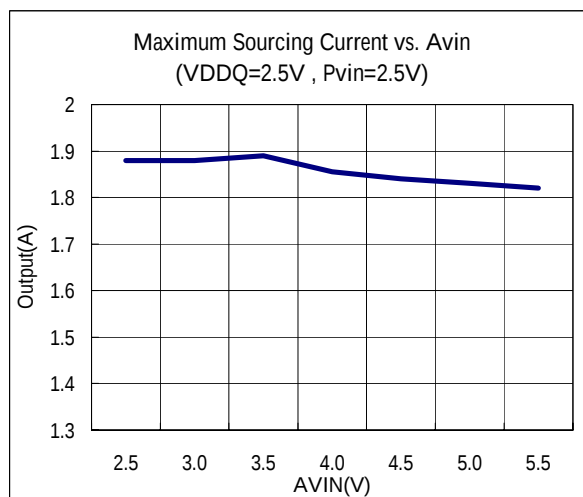
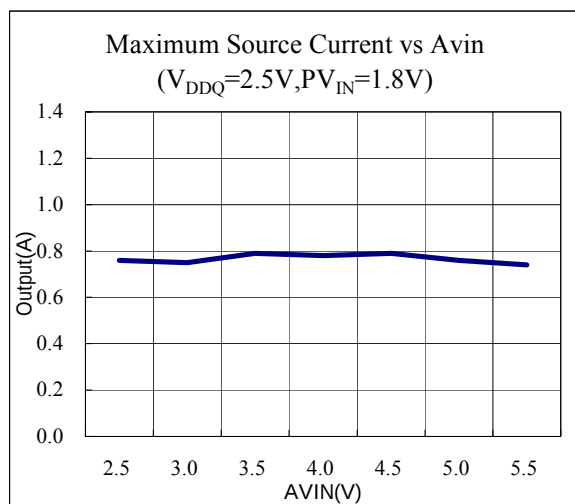
V_{IH}	Shutdown Threshold Trigger	Output = High	1.8	--	--	V
V_{IL}		Output = Low	--	--	0.6	

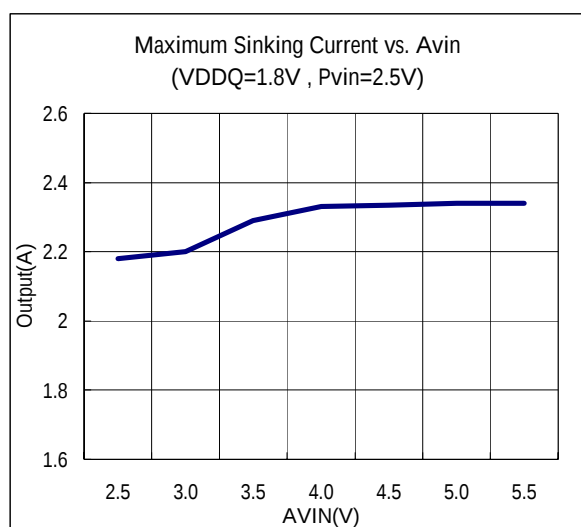
Note 1: V_{OS} offset is the voltage measurement defined as V_{TT} subtracted from V_{REF} .

Note 2: Quiescent current defined as the current flow into AVIN.

Typical Performance Characteristics

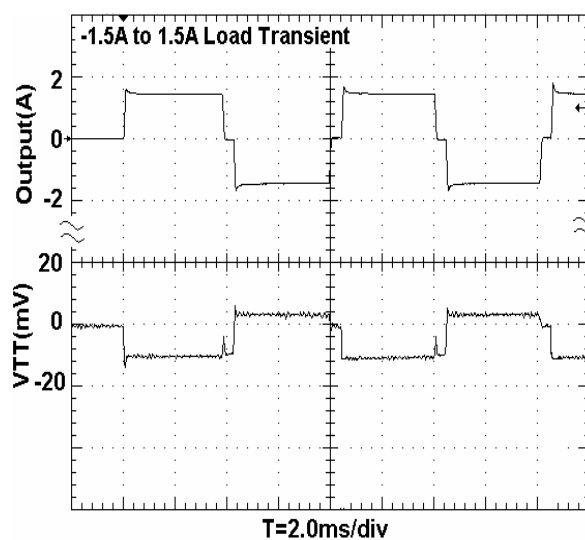






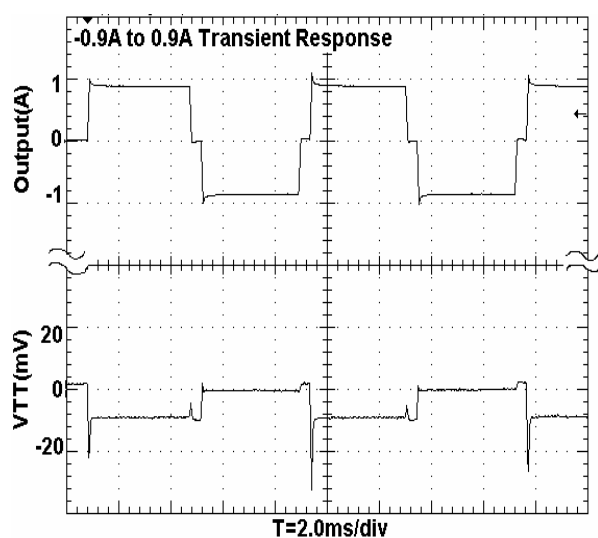
1.25Vtt Transient Response

AVIN==PVIN=VDDQ=2.5V Cour=330uF/16V



0.9Vtt Transient Response

AVIN=2.5V, PVIN=VDDQ=1.8V Cour=330uF/16V



Component Selection

INPUT CAPACITOR

The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 47 μ F. If the two supply rails (AVIN and PVIN) are separated then the 47 μ F capacitor should be placed as close to possible to PVIN rail. An additional 0.1 μ F ceramic capacitor can be placed on the AVIN rail to prevent excessive noise from coupling into the device.

OUTPUT CAPACITOR

As general recommendation, the output capacitor should be sized above 220 μ F with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by maximum current spikes expected from the DDR memory system to ensure V_{TT} staying within ± 40 mV of V_{REF} . Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient.

With motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors. Large aluminum electrolytic capacitors can be used for their low ESR and low cost. Additional 0.1 μ F ceramic capacitor is needed for high frequency decoupling.

When size and performance are critical, several hybrid capacitors such as OS-CON and SP that offer a large capacitance while maintaining a low ESR are the better solution.

PCB Layout Considerations

The EUP7996 regulator is packaged in plastic SOP-8 package. This small footprint package is unable to convectively dissipate at high current levels. The junction temperature should be kept well away from the thermal shutdown temperature in normal operation. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on several variables: the thickness of copper on PCB; the area of top side copper used; and the airflow. Using large traces and more copper on the top side of board with careful layout are possible to reduce thermal resistance on the part.

If the large ground trace around the IC is unavailable on top, numerous vias to connect the part and dissipate heat to the internal ground plane will help. The vias should be small enough to retain solder when the board is wave-soldered.

Additional improvements can be achieved with a constant airflow across the package.

Test Circuit

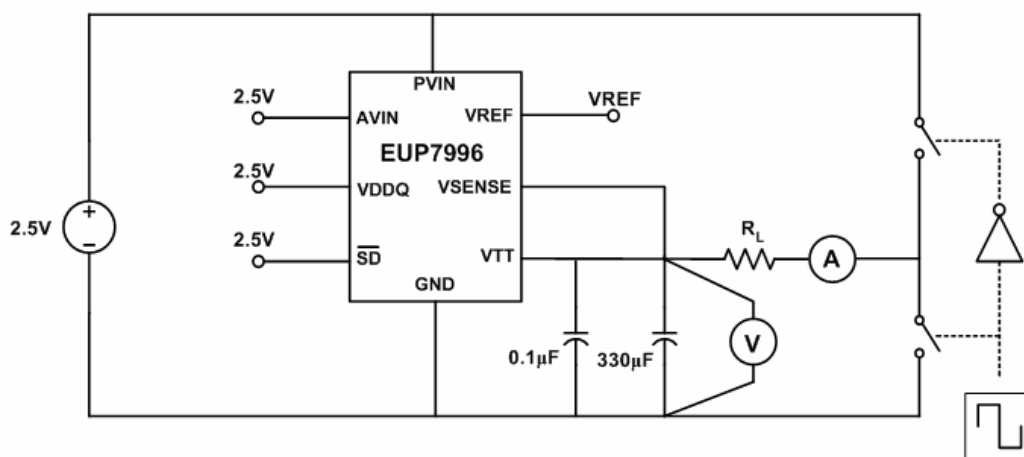
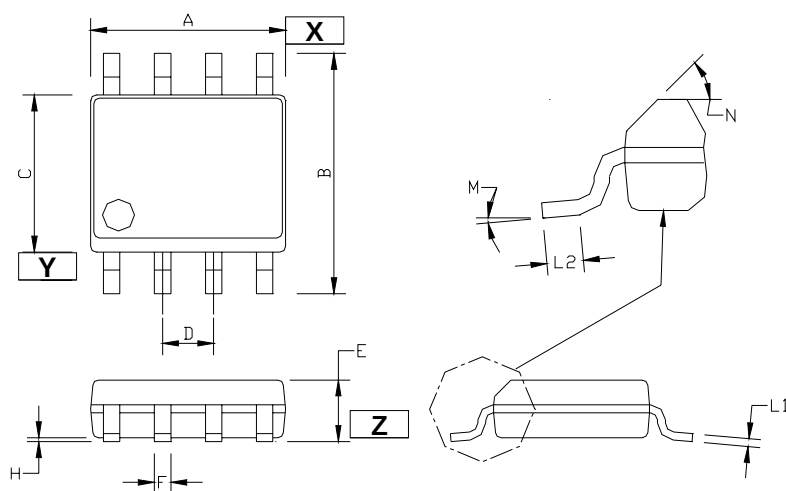
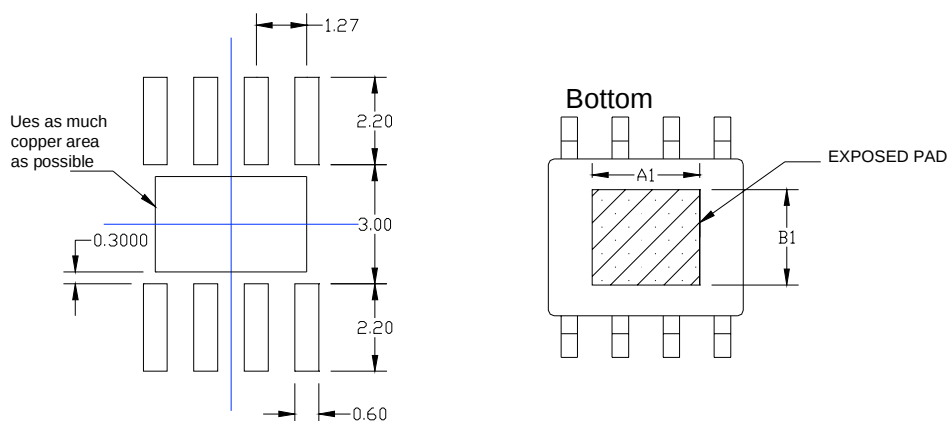


Figure 2. Load transient (+1.5A ~ -1.5A) test circuit

Mechanical Information



Standard Solder Map



Symbols	Dimension in Millimeters		Dimension in Inches	
	Min.	Max.	Min.	Max.
A	4.80	5.00	0.189	0.197
B	5.80	6.20	0.228	0.244
C	3.80	4.00	0.150	0.157
D	1.194	1.346	0.047	0.053
E	1.45	1.55	0.057	0.061
H	0.00	0.10	0.000	0.004
F	0.33	0.51	0.013	0.020
L1	0.19	0.25	0.007	0.010
L2	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	40°	50°	40°	50°
A1	2.6	2.8	0.102	0.110
B1	2.4	2.6	0.095	0.102

8 – Lead SOP(FD) Plastic Package