



# SP3244E-SP3245E

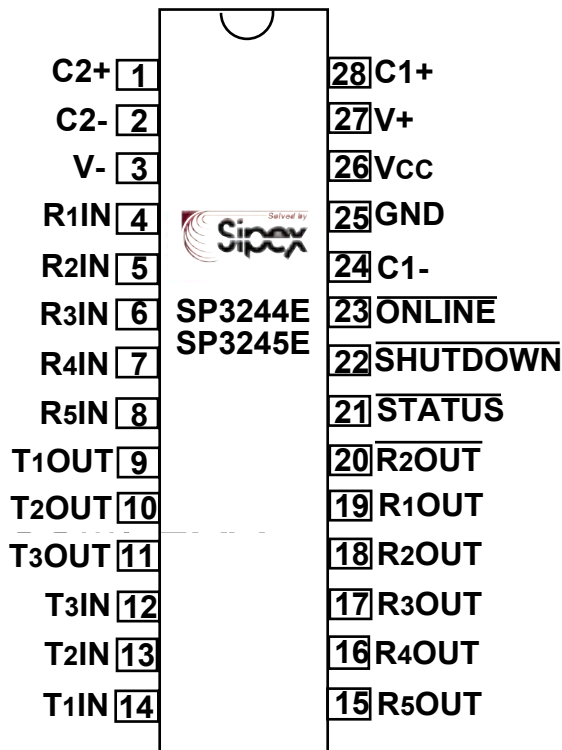
## 3.0V to 5.5V RS-232 Transceivers with Auto On-Line® Plus

### FEATURES

- Contains 3-Drivers and 5-Receivers;  
Single-chip DTE (PC or terminal) serial port transceiver
- Auto On-line® Plus
- SP3244E slew-controlled to 250Kbps under load
- SP3245E 1Mbps data rate for high-speed RS-232
- Meets true EIA/TIA-232-F and ITU V.28 standards from a +3.0V to +5.5V power supply
- Adheres to EIA/TIA-562 for interoperability with EIA/TIA-232 down to a +2.7V supply voltage
- Regulated charge pump yields stable RS-232 outputs regardless of Vcc variations
- ESD Specifications:
  - ±15KV Human Body Model
  - ±15KV IEC1000-4-2 Air Discharge
  - ±8KV IEC1000-4-2 Contact Discharge

### APPLICATIONS

- Portable RS-232
- Laptops and handheld PCs and PDA
- Cellular telephones, datacables, charging cradles
- Diagnostic/upload ports on embedded applications
- Use in conjunction with low-voltage UART or microcontroller
- SP3244E is cross-compatible with MAX3244E, ICL3244E
- SP3245E is cross-compatible with MAX3245E, ICL3245E



### DESCRIPTION

The SP3244E/3245E is a 3-driver/5-receiver device ideal for mobile phone, consumer and PDA applications. These devices use an internal high-efficiency, charge-pump power supply that requires only 0.1µF capacitors for 3.3V single-supply operation. This charge pump and Sipex's driver architecture allow the SP3244E/3245E to deliver compliant RS-232 performance from a power supply ranging from +3.0V to +5.5V. At voltages between +2.7V and +3.0V the driver outputs are compliant with RS-562 and can interface to RS-232 in portable applications.

The Auto On-line® Plus feature allows the device to automatically enter a low power shutdown mode if all receiver and driver inputs have been idle for 30 seconds. The device will "wake-up" from this automatic shutdown state upon detecting activity. This power saving feature functions without system intervention or modifications to software or drivers.

SP3244E supports serial data rates of 250kbps minimum under full load and while maintaining slew rates of less than 30V/µs. SP3245E is capable of high speed communication of up to 1Mbps.

[www.BDTIC.com/Exar/](http://www.BDTIC.com/Exar/)

NAME	FUNCTION	PIN NUMBER	
		(T)SSOP	QFN
C2+	Positive terminal of the inverting charge pump capacitor.	1	29
C2-	Negative terminal of the inverting charge pump capacitor.	2	30
V-	Regulated -5.5V output generated by the charge pump.	3	31
R1IN	RS-232 receiver input.	4	1
R2IN	RS-232 receiver input.	5	2
R3IN	RS-232 receiver input.	6	3
R4IN	RS-232 receiver input.	7	4
R5IN	RS-232 receiver input.	8	5
T1OUT	RS-232 driver output.	9	6
T2OUT	RS-232 driver output.	10	7
T3OUT	RS-232 driver output.	11	8
T3IN	TTL/CMOS driver input.	12	10
T2IN	TTL/CMOS driver input.	13	11
T1IN	TTL/CMOS driver input.	14	12
R5OUT	TTL/CMOS receiver output.	15	13
R4OUT	TTL/CMOS receiver output.	16	14
R3OUT	TTL/CMOS receiver output.	17	15
R2OUT	TTL/CMOS receiver output.	18	17
R1OUT	TTL/CMOS receiver output.	19	18
R2OUT	Non-inverting receiver 2 output; active in shutdown.	20	19
STATUS	Status output.	21	20
SHUTDOWN	Forced SHUTDOWN input. Drive low to shut down drivers, receivers and charge pump. Will override Auto On-line® Plus. Do not leave this pin open.	22	21
ONLINE	Auto On-line® input. Active low enabled automatic power saving feature. Equivalent to competitor's FORCEON pin. Do not leave this pin open.	23	22
C1-	Negative terminal of the voltage doubler charge pump capacitor.	24	23
GND	Ground connection.	25	24
VCC	Device power supply pin (3.0V to 5.5V).	26	26
V+	Regulated +5.5V output generated by the charge pump.	27	27
C1+	Positive terminal of the voltage doubler charge pump capacitor.	28	28

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Vcc).....-0.3V to + 6.0V  
V+ (Note 1).....-0.3V to + 7.0V  
V- (Note 1).....+0.3V to - 7.0V  
|V+| + |V-| .....+13V  
Input voltage at TTL input pin.. -0.3V to VCC +0.3V  
RxIN.....+/-18V  
Driver output (from Ground)..... +/-13.2V  
RxOUT, STATUS.....-0.3V to VCC + 0.3V  
Short Circuit Duration, TxOUT to GND, Continuous  
(One output at a time maximum)  
Storage Temperature.....-65°C to +150°C  
Operating Temperature SP324XECX.....0°C to +70°C  
Operating Temperature SP324XEEX.....-40°C to +85°C  
Lead Temperature (soldering, 10s).....+300°C

SSOP-28,  $\theta_{JA} = 67.1^{\circ}\text{C/W}$   
TSSOP-28,  $\theta_{JA} = 83.6^{\circ}\text{C/W}$   
QFN- 32,  $\theta_{JA} = 22.4^{\circ}\text{C/W}$

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted VCC = +3.0V to +5.5V, TAMB = TMIN to TMAX, C1–C4 = 0.1 $\mu$ F.

Typical values are at TAMB = +25°C, VCC = 3.3V.

PARAMETERS		SYMB	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DC CHARACTERISTICS</b>							
Supply Current, Auto On-Line® Plus		Icc3	Receivers idle, TxIN = Vcc or GND, ONLINE = GND, SHUTDOWN = Vcc Note 1		1	10	$\mu$ A
Supply Current, Shutdown		Icc2	SHUTDOWN = GND		1	10	$\mu$ A
Supply Current, Active		Icc1	ONLINE = SHUTDOWN = Vcc, No Load		1	5	mA
<b>Driver Input and Logic Input Pins:</b>							
Logic Input Voltage	High	V <sub>IH</sub>	Vcc = 3.3V	2			V
			Vcc = 5.0V	2.4			
	Low	V <sub>IL</sub>				0.8	
	Logic Threshold	V <sub>T</sub>			1.5		
Logic Input Leakage Current		I <sub>IL</sub>			0.01	±1.0	$\mu$ A
Logic Input Hysteresis		V <sub>HYS</sub>			100		mV
<b>Receiver Outputs and STATUS Output</b>							
Receiver Output Voltage Low		V <sub>OL</sub>	I <sub>OUT</sub> = -1.6mA			0.4	V
Receiver Output Voltage High		V <sub>OH</sub>	I <sub>OUT</sub> = 1mA	V <sub>CC</sub> -0.6			V
Receiver Output Leakage Current		I <sub>OZ</sub>	Receivers disabled. 0.4V < V <sub>O</sub> < 5.5V		±0.02	±1	$\mu$ A

Note 1: Characterized, not 100% tested.

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted  $V_{CC} = +3.0V$  to  $+5.5V$ ,  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ ,  $C1-C4 = 0.1\mu F$ .

Typical values are at  $T_{AMB} = +25^{\circ}C$ ,  $V_{CC} = 3.3V$ .

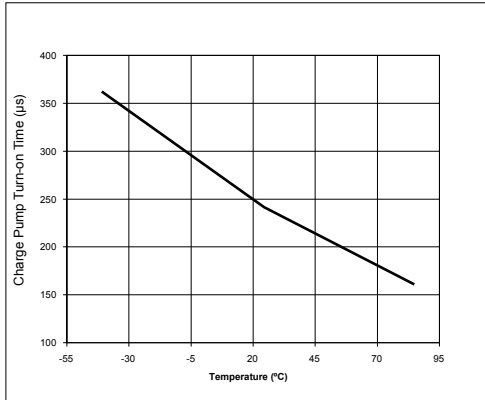
PARAMETERS	SYMB	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Receiver Inputs</b>						
Input Voltage Range			-15		+15	V
Input Threshold Low		$V_{CC} = 3.3V$	0.6	1.0		V
		$V_{CC} = 5.0V$	0.8	1.2		
Input Threshold High		$V_{CC} = 3.3V$		1.2	2.4	V
		$V_{CC} = 5.0V$		1.7	2.4	V
Input Hysteresis				200		mV
Input Resistance		$T_A = 25^{\circ}C$	3	4.5	7	k $\Omega$
<b>Driver Outputs</b>						
Output Voltage Swing	$V_O$	All transmitter outputs loaded with 3k $\Omega$ to GND	$\pm 5.0$	$\pm 5.6$		V
		Output load = Open Circuit			$\pm 15.0$	
Short Circuit Current		$V_{OUT} = 0V$			$\pm 60$	mA
Power-Off Impedance		$V_{CC} = V_+ = V_- = 0$ , transmitter outputs = $\pm 2V$	300	10M		$\Omega$
Output Leakage Current		$V_{CC} = 0$ or 3V to 3.3V, $V_{OUT} = \pm 12V$ , Drivers disabled			$\pm 25$	$\mu A$
Mouse Drivability		$T1IN = T2IN = GND$ , $T3IN = V_{CC}$ , $T3$ loaded with 3k $\Omega$ to GND, $T1OUT$ and $T2OUT$ loaded with 2.5mA each	$\pm 5.0$			V
<b>ESD Protection</b>						
ESD Protection for RxIn, TxOut pins		IEC 1000-4-2 Air Discharge		$\pm 15$		kV
		IEC 1000-4-2 Contact Discharge		$\pm 8$		
		Human Body Model		$\pm 15$		
All Other Pins		Human Body Model		$\pm 2$		kV
<b>Auto On-line® Plus (<math>\overline{ONLINE} = GND</math>, <math>\overline{SHUTDOWN} = V_{CC}</math>)</b>						
Rx Input Threshold to $\overline{STATUS}$ Output High					$\pm 2.7$	V
Rx Input Threshold to $\overline{STATUS}$ Output Low			$\pm 0.3$			V
Threshold to $\overline{STATUS}$ High	$t_{STH}$			0.4		$\mu s$
Threshold to $\overline{STATUS}$ Low	$t_{STL}$			30		$\mu s$
Rx or Tx Transition to Drivers Enabled	$t_{ONLINE}$			100		$\mu s$
Last Rx or Tx Transition to Drivers Disabled	$t_{OFFLINE}$	Note 1	15	30	60	sec

Note 1: Characterized, not 100% tested.

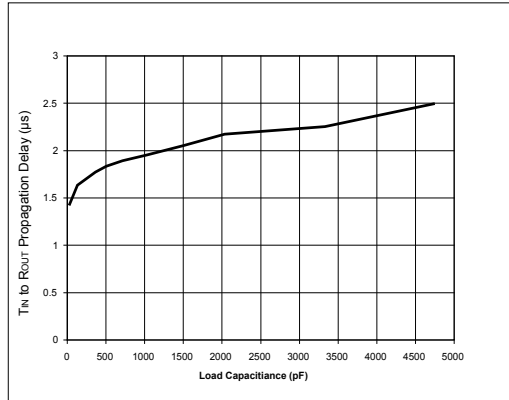
**TIMING CHARACTERISTICS**

Unless otherwise noted  $V_{CC} = +3.0V$  to  $+5.5V$ ,  $T_{AMB} = T_{MIN}$  to  $T_{MAX}$ ,  $C1-C4 = 0.1\mu F$ . Typical values are at  $T_{AMB} = +25^{\circ}C$ ,  $V_{CC} = 3.3V$ .

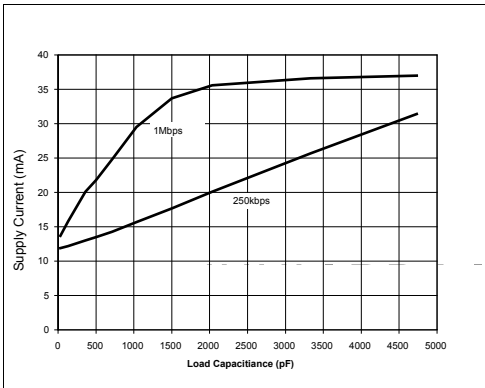
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>SP3244E</b>						
Maximum Data Rate		$R_L = 3k\Omega$ , $C_L = 1000pF$ . One transmitter switching.	250			kbps
Driver Propagation Delay	$td_{PHL}$ , $td_{PLH}$	$C_L = 1000pF$		1600		ns
Transition-Region Slew Rate		$R_L = 3k\Omega$ to $7k\Omega$ , $C_L = 150pF$ to $1000pF$ , measurements taken from $+3V$ to $-3V$ or from $-3V$ to $+3V$ .	4		30	V/ $\mu s$
Driver Skew		$ td_{PHL} - td_{PLH} $ at zero crossing		50		ns
Receiver Propagation Delay	$tr_{PHL}$ , $tr_{PLH}$	$R_{IN}$ to $R_{OUT}$ , $C_L = 150pF$		0.15		$\mu s$
Receiver Output Enable Time	$tr_{ZH}$ , $tr_{ZL}$			0.04	2.0	$\mu s$
Receiver Output Disable Time	$tr_{ZH}$ , $tr_{ZL}$			0.1	2.0	$\mu s$
Receiver Skew		$ t_{PHL} - t_{PLH} $ at 1.5V		40		ns
<b>SP3245E</b>						
Maximum Data Rate		$R_L = 3k\Omega$ , $C_L = 250pF$ . One transmitter switching.	1000			kbps
		$R_L = 3k\Omega$ , $C_L = 1000pF$ . One transmitter switching.	500			kbps
Driver Propagation Delay	$td_{PHL}$ , $td_{PLH}$	$C_L = 250pF$		700		ns
Transition-Region Slew Rate		$R_L = 3k\Omega$ to $7k\Omega$ , $C_L = 150pF$ to $250pF$ , measurements taken from $+3V$ to $-3V$ or from $-3V$ to $+3V$ .	24		150	V/ $\mu s$
Driver Skew		$ td_{PHL} - td_{PLH} $ at zero crossing		100		ns
Receiver Propagation Delay	$tr_{PHL}$ , $tr_{PLH}$	$R_{IN}$ to $R_{OUT}$ , $C_L = 150pF$		0.15		$\mu s$
Receiver Output Enable Time	$tr_{ZH}$ , $tr_{ZL}$			0.05	2.0	$\mu s$
Receiver Output Disable Time	$tr_{ZH}$ , $tr_{ZL}$			0.1	2.0	$\mu s$
Receiver Skew		$ t_{PHL} - t_{PLH} $ at 1.5V		90		ns



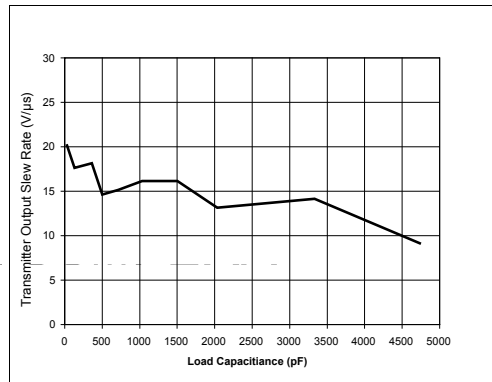
Turn on Time vs. Temperature



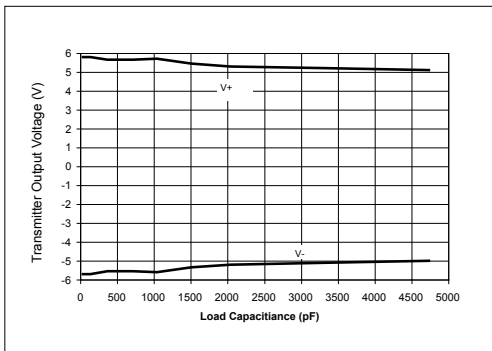
Transmitter Input to Receiver Output Propagation Delay vs. Load Capacitance



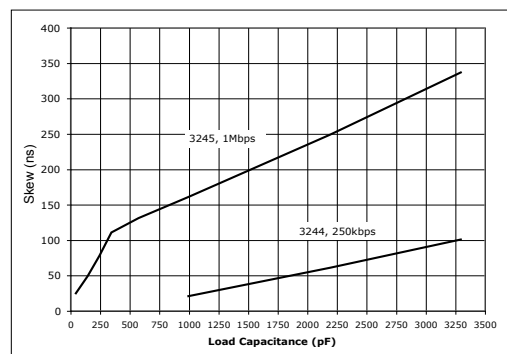
I<sub>CC</sub> vs. Load Capacitance



Transmitter Output Slew Rate vs. Load Capacitance

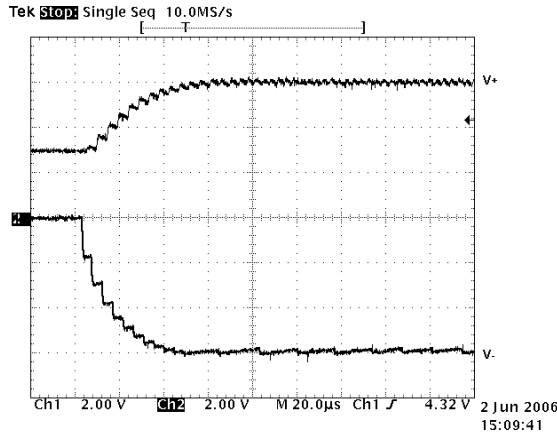


Transmitter Output vs. Load Capacitance

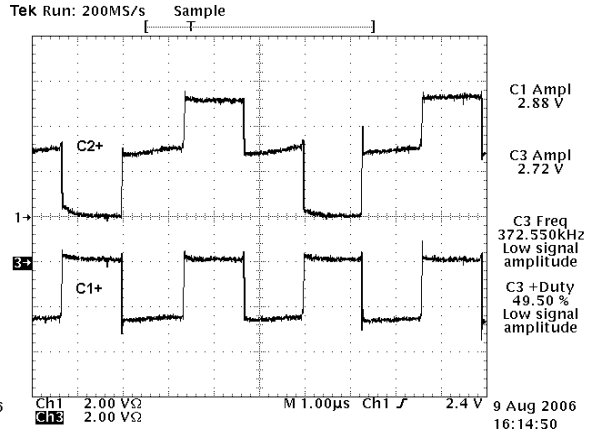


Transmitter Skew vs. Load Capacitance

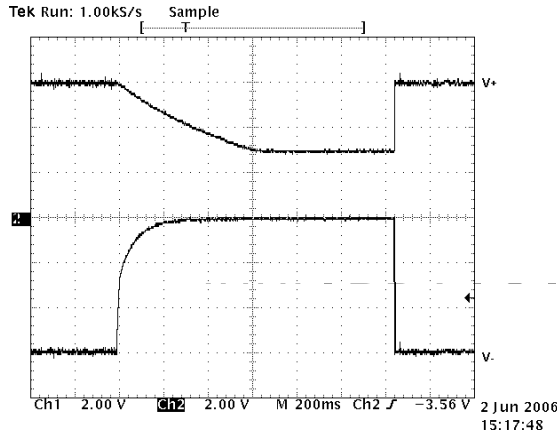
# TYPICAL PERFORMANCE CHARACTERISTICS



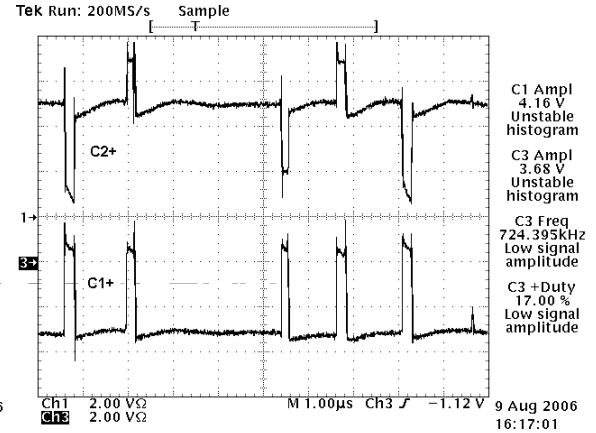
SP3244E Charge Pump Levels Out of Shut-down



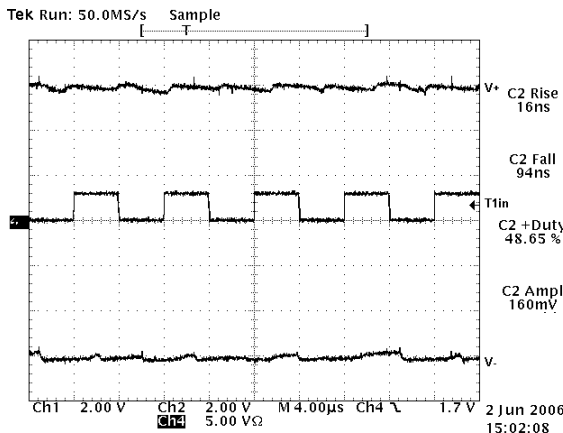
SP3244E C2+ Charge Pump Waveforms - Vcc=3.3V, All channels switching



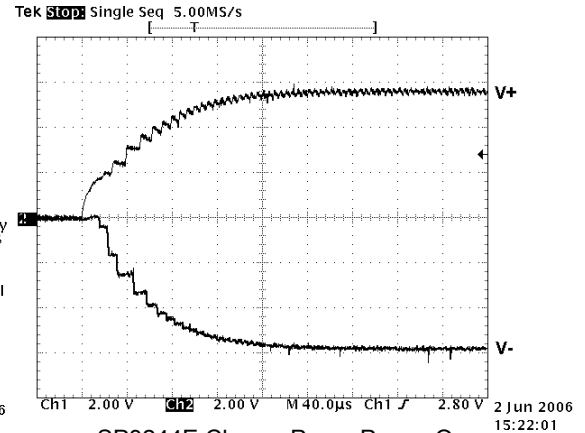
SP3244E Charge Pump Levels Into Shut-down



SP3244E C2+ Charge Pump Waveforms - Vcc=5.0V, All channels switching



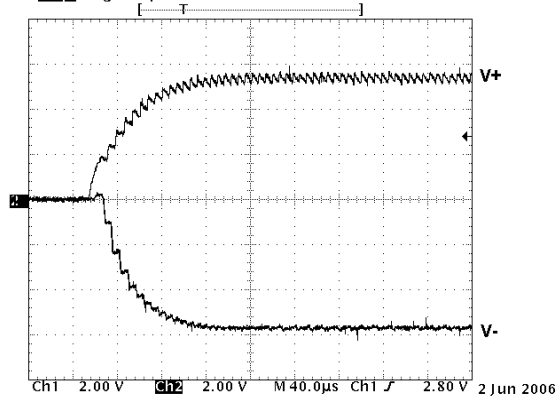
SP3244E Charge Pump Waveforms for 250kpbs Clock Rate



SP3244E Charge Pump Power On Time Vcc=3.3V, T=27C

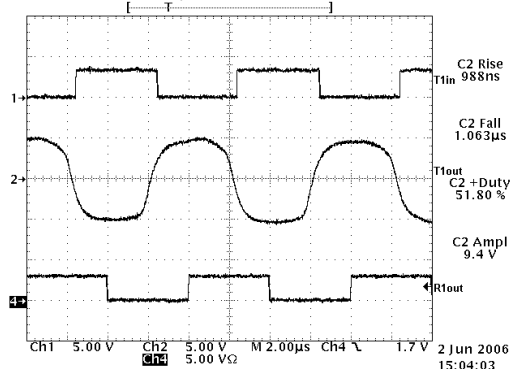
## TYPICAL PERFORMANCE CHARACTERISTICS

Tek **Stop** Single Seq 5.00MS/s



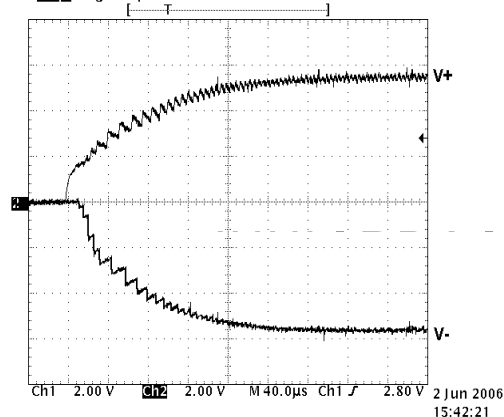
SP3244E Charge Pump Power On Time  
-  $V_{CC}=3.3V$ ,  $T=85^{\circ}C$

Tek Run: 100MS/s Sample



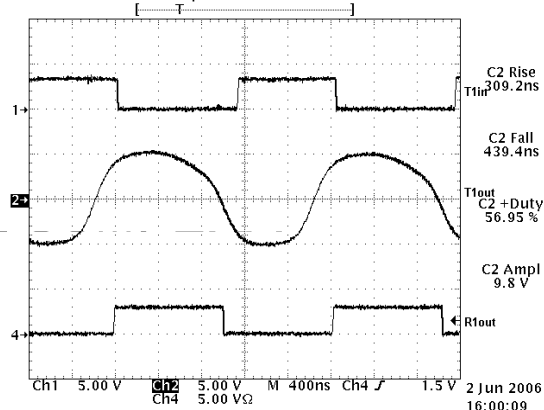
SP3244E Waveforms for 250kbps Clock Rate  
 $R_L=3k\Omega$   $C_L=4700pF$

Tek **Stop** Single Seq 5.00MS/s



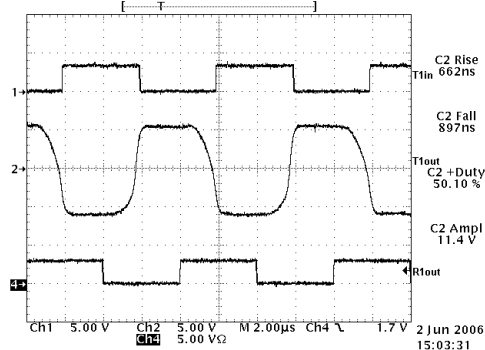
SP3244E Charge Pump Power On Time  
-  $V_{CC}=3.3V$ ,  $T=-40^{\circ}C$

Tek Run: 500MS/s Sample



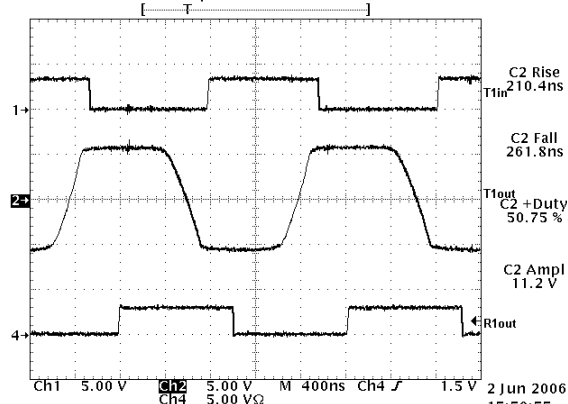
SP3245E Waveforms for 1Mbps Clock Rate  
 $R_L=3k\Omega$   $C_L=1000pF$

Tek Run: 100MS/s Sample



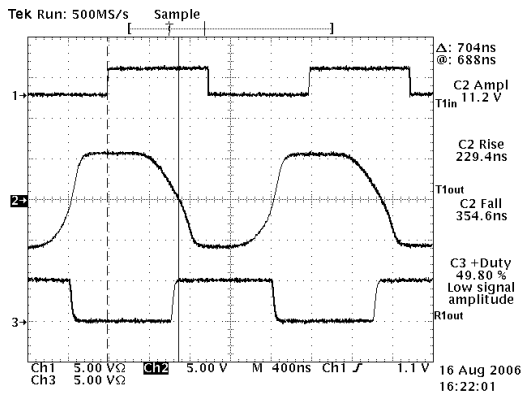
SP3244E Waveforms for 250kbps Clock Rate  
 $R_L=3k\Omega$   $C_L=1000pF$

Tek Run: 500MS/s Sample



SP3245E Waveforms for 1Mbps Clock Rate  
 $R_L=3k\Omega$   $C_L=50pF$

## TYPICAL PERFORMANCE CHARACTERISTICS



SP2345 Waveforms for 1Mbps Clock Rate  
 - RL=3k, CL=250pF

The SP3244E and SP3245E are 3-driver/5-receiver devices ideal for serial ports in battery-powered, portable, or handheld applications such as notebook or handheld computers. SP3244E/3245E transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols for reliable serial communication. The SP3244E/3245E devices feature Sipex's proprietary and patented (U.S. 5,306,954) on-board charge pump circuitry that generates  $\pm 5.5V$  RS-232 voltage levels from a single +3.0V to +5.5V power supply.

The SP3244E/3245E is an ideal choice for power sensitive designs. With the Auto On-line® Plus enabled the SP3244E/3245E reduces power consumption to a  $1\mu A$  supply current whenever the transceivers are idle. In shutdown, the internal charge pump and the drivers will shut down. Receivers remain active unless the device is put into manual shutdown using the SHUTDOWN pin. This feature allows design engineers to address power saving concerns without major design changes.

### Theory Of Operation

The SP3244E/3245E is made up of four basic circuit blocks:

1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. Auto On-line® Plus circuitry.

### Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is +5.4V with no load and +5V minimum fully loaded. The driver outputs are protected against infinite short circuits to ground without degradation in reliability. These drivers comply with the EIA/TIA-232-F and all previous RS-232 versions. Unused driver inputs should be connected to GND or VCC.

The SP3244E/3245E devices operate at this typical data rate when fully loaded. The drivers can guarantee output data rates fully loaded with  $3K\Omega$  in parallel with  $1000pF$  (SP3244E), or  $250pF$  (SP3245E) ensuring compatibility with popular PC-to-PC communication software. The slew rate of the driver output on the SP3244E is internally limited to a maximum of  $30V/\mu s$  in order to meet the EIA standards

(EIA RS-232D 2.1.7, Paragraph 5). The slew rate of SP3245E is not limited to enable higher speed data transfers. The transition of the loaded output from HIGH to LOW also meets the monotonic signal transition requirements of the standard.

### Receivers

The receivers convert EIA/TIA-232 signal levels to TTL or CMOS logic output levels. Receivers remain active unless the device is put into manual shutdown using the SHUTDOWN pin. The non-inverted output of Receiver 2 ( $\overline{R2OUT}$ ) will continue to be active in all modes, including shutdown.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal  $5K\Omega$  pull-down resistor to ground will commit the output of the receiver to a HIGH state.

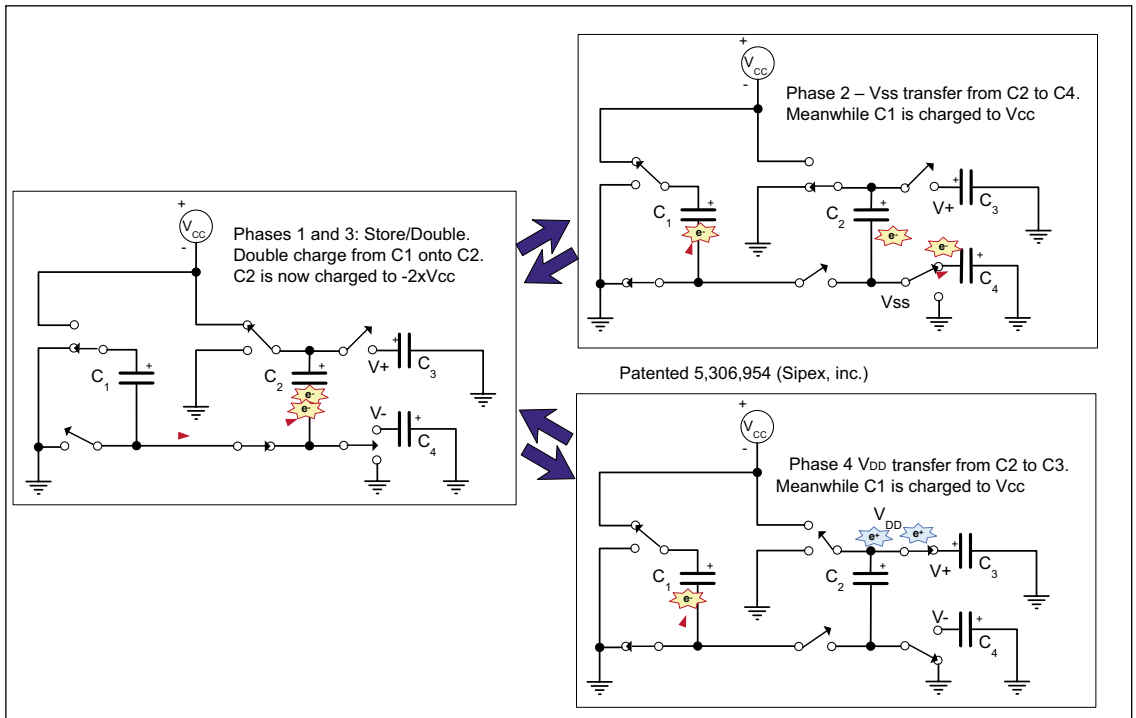
### Highly Efficient Charge Pump

The charge pump is used to generate positive and negative signal voltages for the RS-232 drivers. This enables fully compliant RS-232 and V.28 signals from a single 3.0 or 5.5V power supply.

The charge pumps use four external capacitors to hold and transfer electrical charge. The Sipex patented design (US Patent #5,306,954) uses a unique approach compared to older less efficient designs. The pumps use a four-phase voltage shifting technique to attain symmetrical V+ and V- power supplies. An intelligent control oscillator regulates the operation of the charge pump to maintain the proper voltages at maximum efficiency.

### Phase 1

VSS charge store and double. The positive terminals of capacitors C1 and C2 are charged from VCC with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to VCC the voltage potential across capacitor C2 is now  $2 \times V_{CC}$ .



Charge Pump Phases

Minimum Recommended Charge Pump Capacitor Values	
Input Voltage $V_{CC}$	Charge Pump Capacitor Value for SP32XX
3.0V to 3.6V	C1-C4=0.1 $\mu$ F
4.5V to 5.5V	C1=0.047 $\mu$ F, C2-C4=0.33 $\mu$ F
3.0V to 5.5V	C1-C4=0.22 $\mu$ F

Charge Pump Capacitor Values

## Phase 2

VSS transfer and invert: Phase two connects the negative terminal of C2 to the VSS storage capacitor and the positive terminal of C2 to ground. This transfers the doubled and inverted ( $V^-$ ) voltage onto C4. Meanwhile, capacitor C1 charged from VCC to prepare it for its next phase.

## Phase 3

VDD charge store and double: Phase three is identical to the first phase. The positive terminals of capacitors C1 and C2 are charged from VCC with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1– is superimposed onto C2–. Since C2+ is still connected to VCC the voltage potential across capacitor C2 is now  $2 \times V_{CC}$ .

## Phase 4

VDD transfer: The fourth phase connects the negative terminal of C2 to ground and the positive terminal of C2 to the VDD storage capacitor. This transfers the doubled ( $V^+$ ) voltage onto C3. Meanwhile, capacitor C1 charged from VCC to prepare it for its next phase.

The Sipex chargepump generates  $V^+$  and  $V^-$  independently from VCC. Hence in a no-load condition  $V^+$  and  $V^-$  will be symmetrical. Older charge pump approaches generate  $V^+$  and then use part of that stored charge to generate  $V^-$ . Because of inherent losses the magnitude of  $V^-$  will be smaller than  $V^+$  on these older designs.

Under lightly loaded conditions the intelligent pump oscillator maximizes efficiency by running only as needed to maintain  $V^+$  and  $V^-$ . Since interface transceivers often spend much of their time at idle this power-efficient innovation can greatly reduce total power consumption. This improvement is made possible by the independent phase sequence of the Sipex charge-pump design.

The clock rate for the charge pump typically operates at greater than 70kHz allowing the pump to run efficiently with small 0.1 $\mu$ F capacitors. Efficient operation depends on rapidly charging and discharging C1 and C2, therefore capacitors should be mounted close to the IC and have low ESR (equivalent series resistance). Inexpensive

## DESCRIPTION

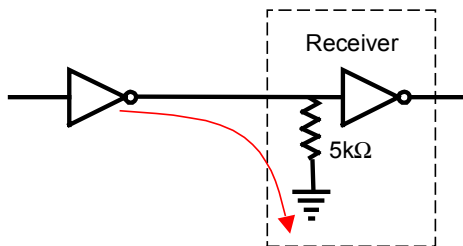
surface mount ceramic capacitors (such as are widely used for power-supply decoupling) are ideal for use on the charge pump. The charge pumps are designed to be able to function properly with a wide range of capacitor styles and values. If polarized capacitors are used the positive and negative terminals should be connected as shown on the Typical Operating Circuit.

Capacitance values may be increased if operating at higher VCC or to provide greater stability as the capacitors age. See Charge Pump Capacitor Value table on page 11.

## Auto On-line® Plus Circuitry

The SP3244E/3245E devices have the advanced Auto On-line® Plus feature that saves power by turning off the charge pumps and driver outputs when the transceiver inputs are idle for more than 30 seconds.

RS-232 signals use both positive and negative voltages of greater than  $\pm 5V$  magnitude. Receivers have nominal 5k $\Omega$  impedance to ground. Even when idle, drivers will maintain output signal voltage creating a continuous current flow. In low power battery operated devices this constant current drain can decrease battery life significantly.



Receiver 5k $\Omega$  Current path to GND

Auto On-line® Plus devices may be configured to emulate the behavior of devices with our earlier Auto On-line® feature. Auto On-line® Plus puts the device into a low power mode when driver and receiver inputs are idle and re-awakes upon detecting signal transitions. Auto On-line® puts the device into a low power mode when receiver inputs are left floating and re-awakes when receivers are driven greater than  $\pm 2.7V$  magnitude by incoming RS-232 signal.

Auto On-line® Plus provides greater power savings in typical operation because the transceiver will go into low power standby mode unless a communication link is in use. Signals such as CTS, RTS, DTR, DSR, or RI will typically change signal-state to establish handshaking before any actual data-communication takes place. Transitions on these handshake signals will wake up the Auto On-line® Plus transceiver to prepare it for sending data ( $t_{ONLINE}$  100 $\mu$ s typical).

Receivers remain active to detect incoming signals in Auto On-line® Plus standby mode. Receiver outputs may be disabled by entering manual shutdown by driving SHUTDOWN pin to logic 0. A special non-inverted receiver output R2OUT remains active in all modes, including SHUTDOWN pin at logic 0.

In some applications if there is a significant delay (greater than  $t_{OFFLINE}$ ) between the handshaking transitions and the start of data communication the transceiver may enter Auto On-Line® Plus standby mode before data communication begins. The  $t_{OFFLINE}$  interval is at least 15 seconds and no longer than 60 seconds.

In applications where the transceiver needs to remain active anytime it is connected to live RS-232 signals, even if those signals remain idle for longer than  $t_{OFFLINE}$ , then the STATUS output may be used to drive the ONLINE pin. The STATUS output pin functions the same in both Auto On-line® and Auto On-line® Plus devices. STATUS will output logic 1 if any of the receiver inputs are driven greater than  $\pm 2.7V$  magnitude by incoming RS-232 signals and drives logic 0 if receiver inputs are floating or driven to ground. Driving the ONLINE pin with the STATUS output disables Auto On-line® Plus (Forced On-Line) whenever RS-232 voltages are seen on any receiver inputs. If no RS-232 voltages are seen on the receiver inputs the Auto On-line® Plus transceiver will still activate its charge pump and driver outputs when the driver inputs are active. This allows the transceiver to signal a remote Auto On-Line® or Auto On-Line® Plus, on the other end of the data cable, to wake up.

modes, including SHUTDOWN pin at logic 0. Connecting STATUS output to drive both ONLINE and SHUTDOWN will wake the transceiver if any receiver inputs are driven greater than  $\pm 2.7V$  magnitude and put the transceiver into Forced Shutdown mode if all receiver inputs are floating or driven to ground.

### **$\pm 15KV$ ESD PROTECTION**

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver inputs of the SP3244E/3245E have extra protection against static electricity. Sipex uses state-of-the-art structures to protect these pins against ESD of  $\pm 15kV$  without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the SP3244E/3245E keep working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the SP3244E/3245E are characterized for protection to the following limits:

- $\pm 15kV$  using the Human Body Model
- $\pm 8kV$  using the Contact Discharge method specified in IEC 1000-4-2
- $\pm 15kV$  using the Air-Gap Discharge method specified in IEC 1000-4-2

The STATUS output pin remains active in all

## Auto On-Line® Plus Truth Table

Operating mode	ONLINE	SHUTDOWN	RxIN  > ± 2.7 V	Idle inputs (RxIN & TxIN)	TxOUT	RxOUT	R2OUT
Forced Shutdown	X	0	X	X	high-Z	high-Z	active
Forced Online	1	1	X	X	active	active	active
Auto On-line® Plus (Wake When Active)	0	1	X	active	active	active	active
Auto On-line® Plus (Off-Line When Idle)	0	1	X	idle > 30s	high-Z	active	active
Auto On-line® Plus (Wake On Cable)	STATUS	1	yes	X	active	active	active
Auto On-line® Plus (Wake When Active)	STATUS	1	no	active	active	active	active
Auto On-line® Plus (Off-Line When Idle)	STATUS	1	no	idle > 30s	high-Z	active	active
Auto On-line® (Wake On Cable)	STATUS	STATUS	yes	X	active	active	active
Auto On-line® (Auto Shutoff)	STATUS	STATUS	no	X	high-Z	active	active

**ESD Test Conditions**

ESD performance depends on a variety of conditions. Contact Sipex for a reliability report that documents test setup, methodology and results.

**IEC 1000-4-2**

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The SP3244E/3245E helps you design equipment to meet IEC 1000-4-2, without sacrificing boardspace and cost for external ESD-protection components. The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2.

Series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model.

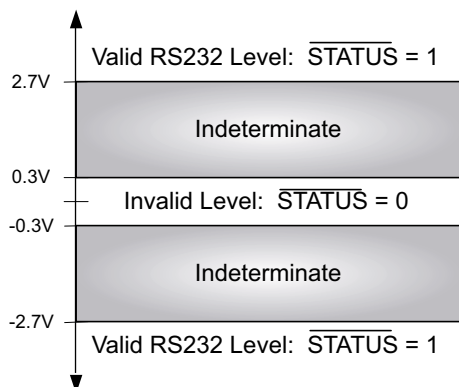
The air-gap test involves approaching the device with a charged probe. The contact discharge method connects the probe to the device before the probe is energized.

**Machine Model**

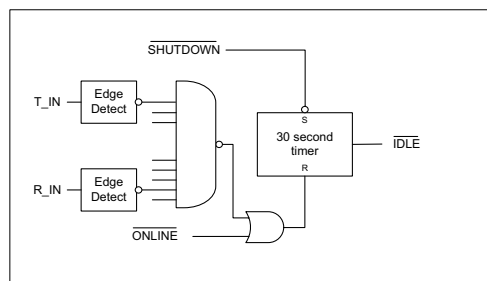
The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

**ESD Table**

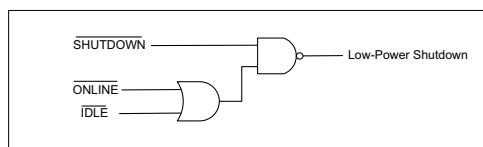
Device Pin Tested	Human Body Model	IEC1000-4-2		
		Air discharge	Contact discharge	Level
TxOUT	± 15kV	± 15kV	± 8kV	4
RxIN	± 15kV	± 15kV	± 8kV	4
TxIN, RxOUT, <u>ONLINE</u> , SHUTDOWN, STATUS	± 2kV	± 2kV	± 2kV	1



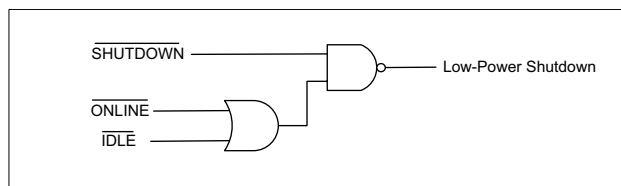
**Receiver Positive and Negative Threshold versus STATUS Output Signal**



**Auto On-line® Plus Logic**



**STATUS Output Logic**



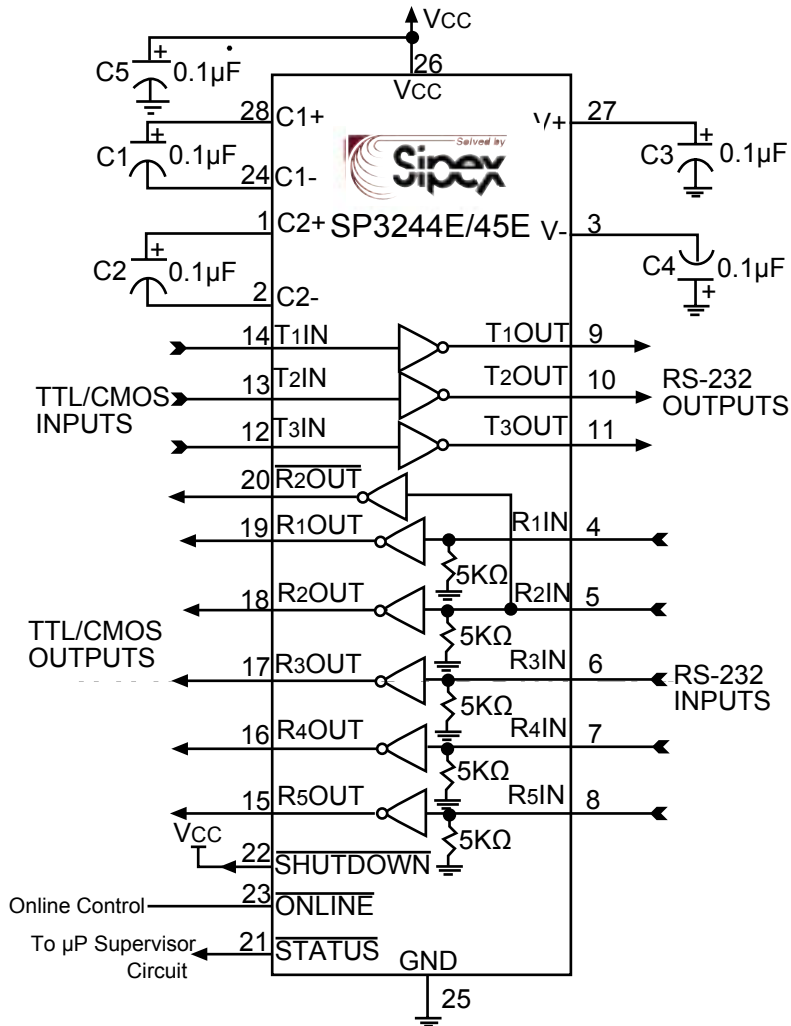
**Shutdown Logic**

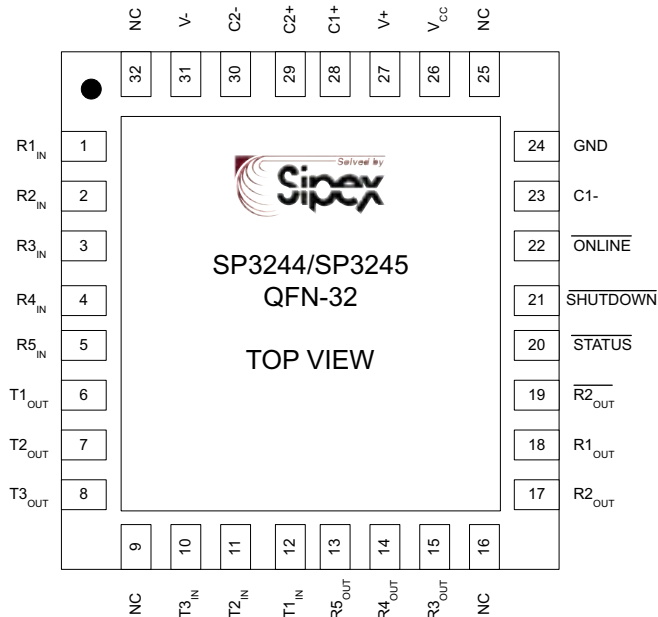
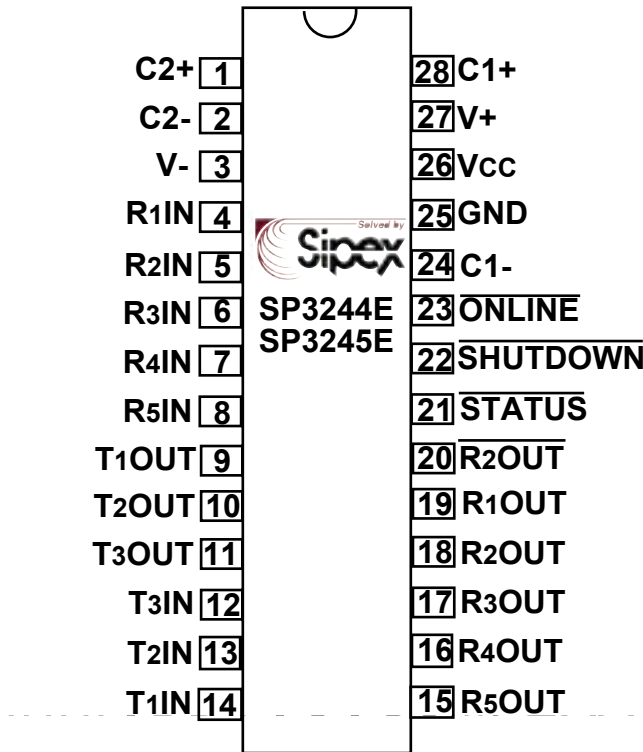


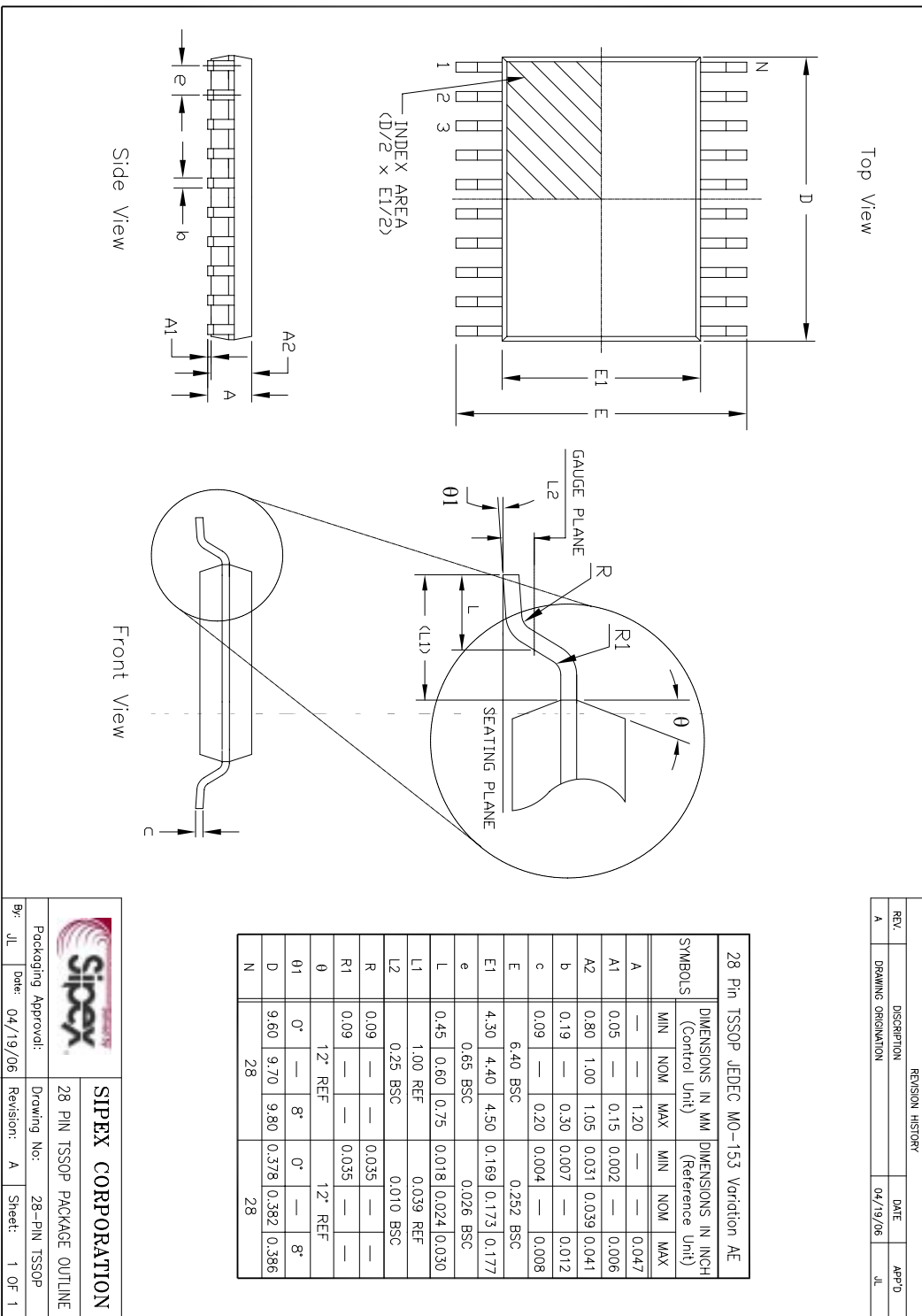
t<sub>STH</sub> (=0.4μs typ.)

tOFFLINE (=30s typ.)

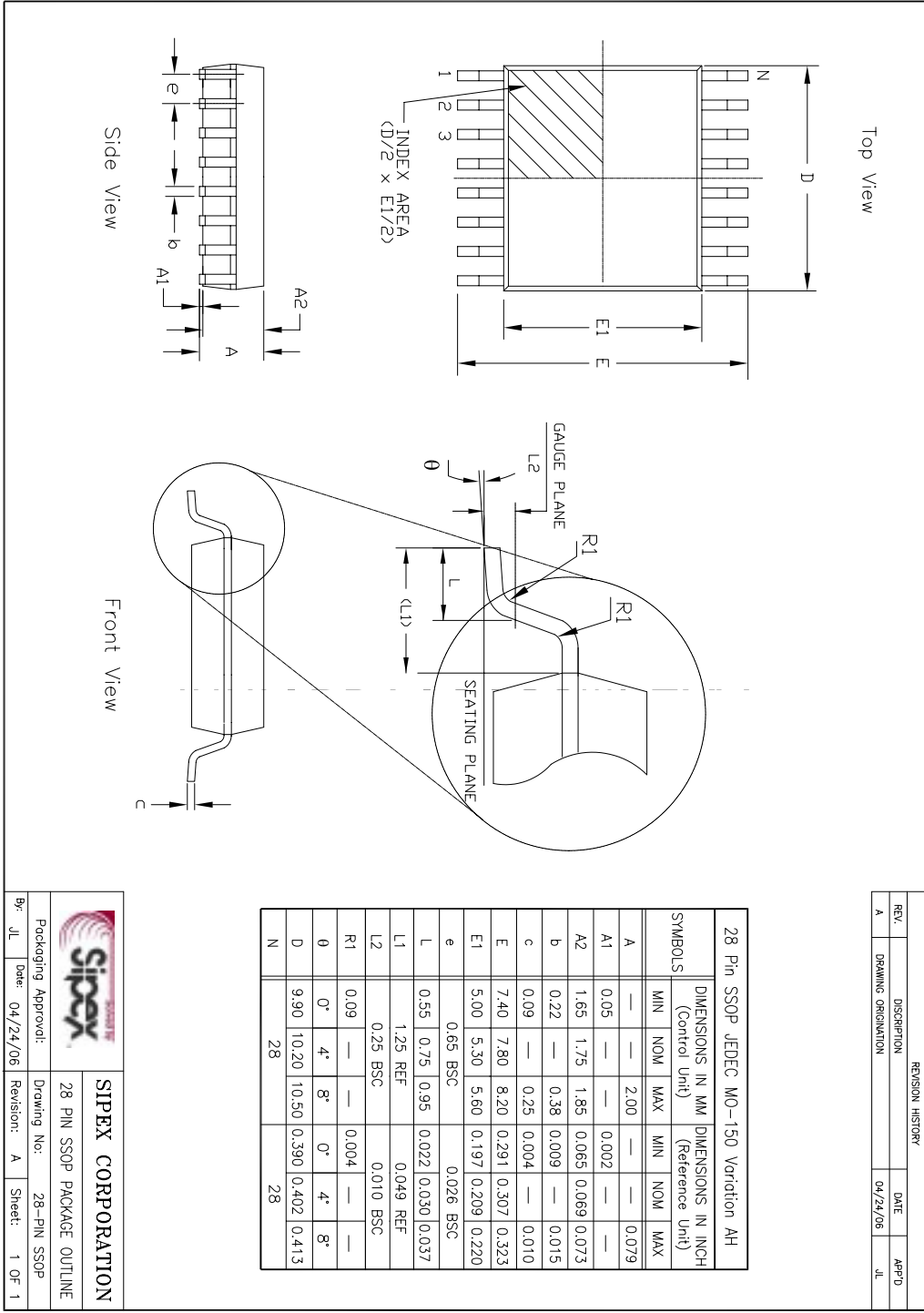
tONLINE (=100μs typ.)

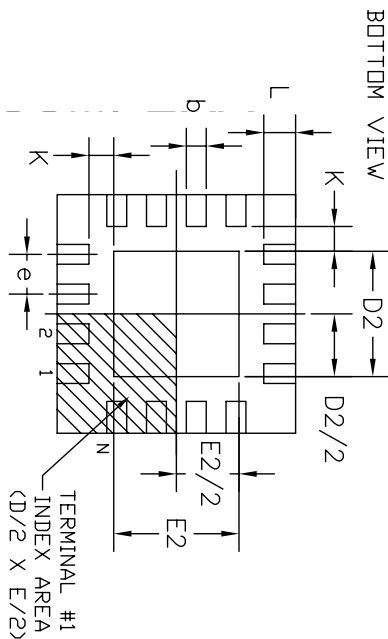
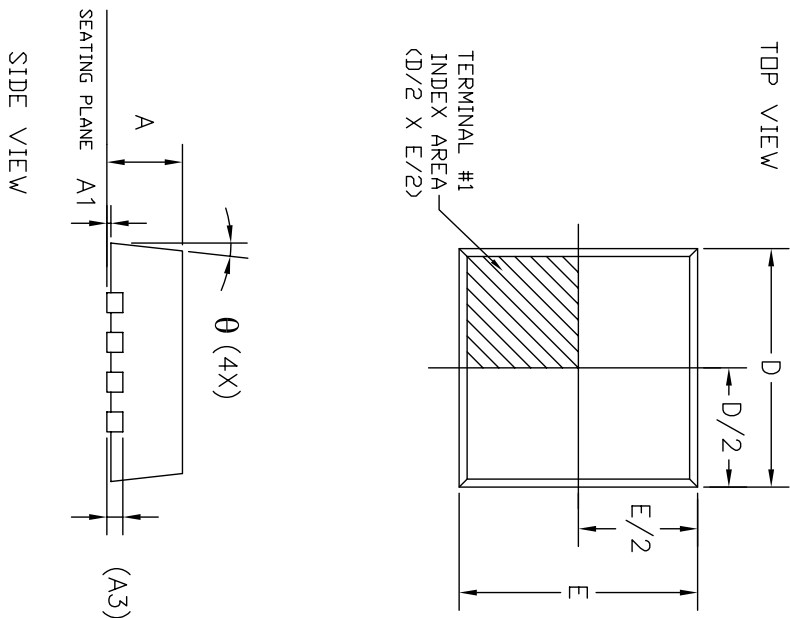






REVISION HISTORY			
REV	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	04/19/06	JL





32LD 5x5 QFN JEDEC MO-220 Variation VHHD-4						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF 0.008 REF					
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC 0.197 BSC					
D2	3.50	3.65	3.80	0.138	0.144	0.150
E	5.00 BSC 0.197 BSC					
E2	3.50	3.65	3.80	0.138	0.144	0.150
e	0.50 BSC 0.020 BSC					
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20	—		0.008	—	
θ	0°	14°		0°	14°	
N	32					
ND	8					
NE	8					

REVISION HISTORY			
REV	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	11/21/05	JL
B	MODIFY DRAWING FORMAT	07/20/06	JL



SIPEX CORPORATION

32 PIN 5x5 QFN PACKAGE OUTLINE

Packaging Approval:

Drawing No:

By: JL

Revision: B

Date: 07/20/06

Sheet: 1 OF 1

Part number	Temperature range	Package Type
SP3244ECA-L	From 0° to +70°C	28 pin SSOP
SP3244ECY-L	From 0° to +70°C	28 pin TSSOP
SP3244EEA-L	From -40° to +85°C	28 pin SSOP
SP3244EEY-L	From -40° to +85°C	28 pin TSSOP
SP3244EER1-L	From -40° to +85°C	32 pin QFN
SP3245ECA-L	From 0° to +70°C	28 pin SSOP
SP3245ECY-L	From 0° to +70°C	28 pin TSSOP
SP3245EEA-L	From -40° to +85°C	28 pin SSOP
SP3245EEY-L	From -40° to +85°C	28 pin TSSOP
SP3245EER1-L	From -40° to +85°C	32 pin QFN

Available in lead free packaging.

Available in Tape and Reel. To order add "/TR" suffix to part number,

Example: SP3244ECA-L= Standard: SP3244ECA-L/TR =Tape and Reel

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Solved by Sipex.

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