HMC424LP3 / 424LP3E

v08.0809

0.5dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 13 GHz

Typical Applications

The HMC424LP3 / HMC424LP3E is ideal for:

- Basestation Infrastructure
- Fiber Optics & Broadband Telecom
- Microwave & VSAT Radios
- Military & Space
- Test Instrumentation

Features

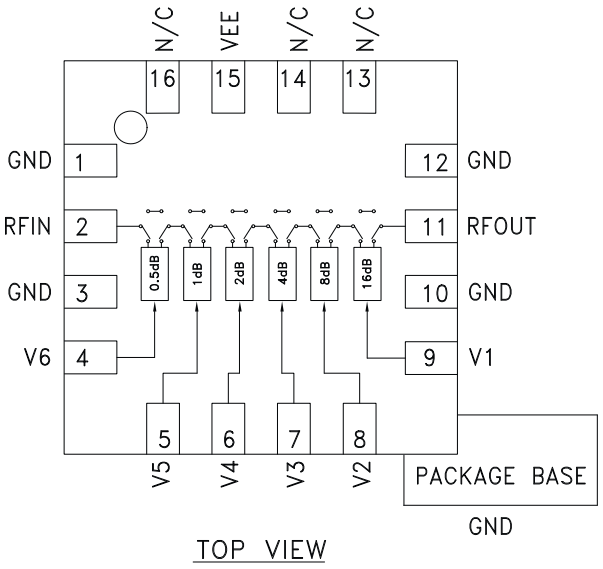
0.5 dB LSB Steps to 31.5 dB

Single Control Line Per Bit

± 0.5 dB Typical Bit Error

9mm² Leadless SMT Plastic Package

Functional Diagram



General Description

The HMC424LP3 & HMC424LP3E are broadband 6-bit GaAs IC digital attenuators in low cost leadless surface mount packages. Covering DC to 13 GHz, the insertion loss is less then 4 dB typical. The attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent at ± 0.5 dB typical step error with an IIP3 of +32 dBm. Six control voltage inputs, toggled between 0 and -5V, are used to select each attenuation state. A single Vee bias of -5V allows operation at frequencies down to DC.

Electrical Specifications, T_A = +25° C, With Vee = -5V & VCTL= 0/-5V

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 4 GHz 4.0 - 8.0 GHz 8.0 - 13.0 GHz		3.1 3.5 4.0	3.8 4.0 4.6	dB dB dB
Attenuation Range	DC - 13.0 GHz		31.5		dB
Return Loss (RF1 & RF2, All Atten. States)	DC - 13.0 GHz	9	12		dB
Attenuation Accuracy: (Referenced to Insertion Loss) 0.5 - 15.5 dB States 16 - 31.5 dB States	 DC - 13.0 GHz DC - 13.0 GHz	 ± 0.3 + 3% of Atten. Setting Max ± 0.3 + 5% of Atten. Setting Max			 dB dB
Input Power for 0.1 dB Compression	1.0 - 13.0 Ghz		22		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone) REF State All Other States	1.0 - 13.0 Ghz		 46 32		 dBm dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON/tOFF (50% CTL to 10/90% RF)	DC - 13.0 GHz		 30 50		 ns ns

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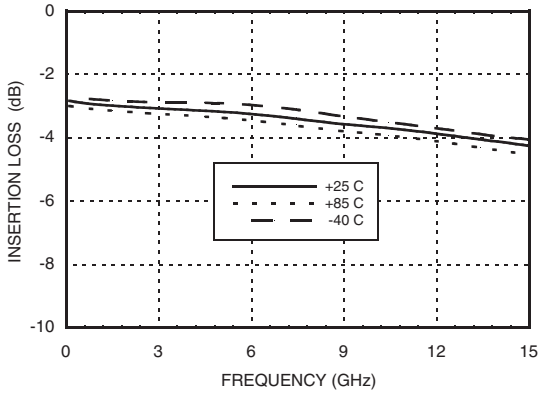
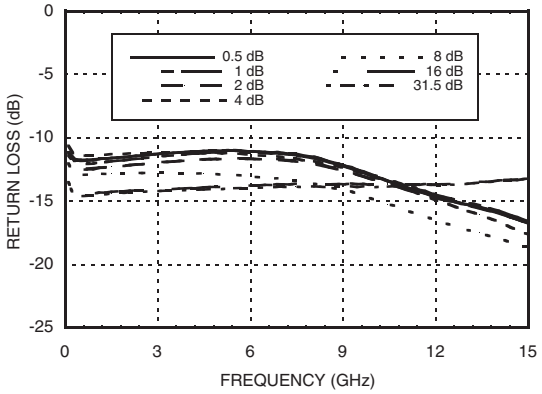
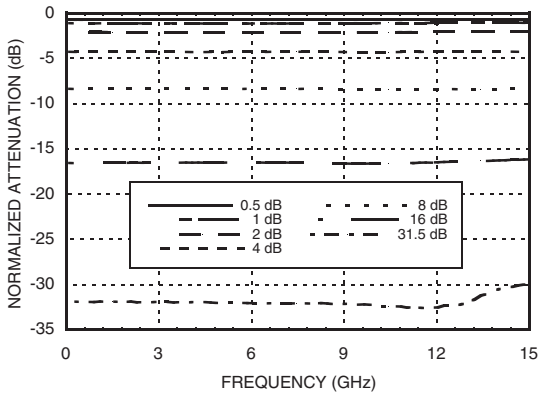
Insertion Loss



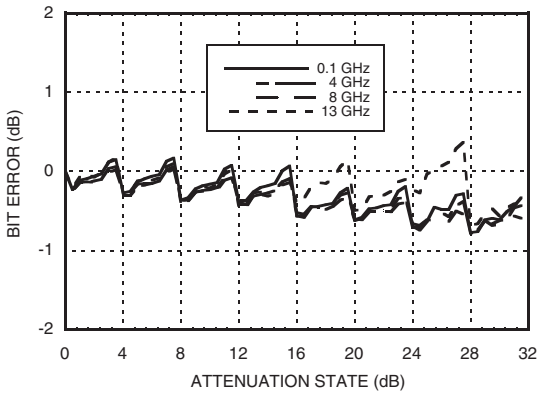
Return Loss RF1, RF2
(Only Major States are Shown)



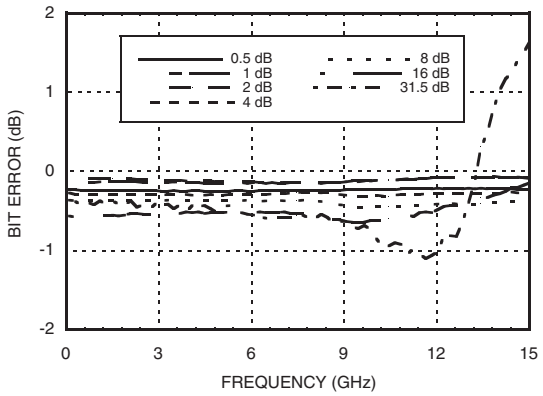
Normalized Attenuation
(Only Major States are Shown)



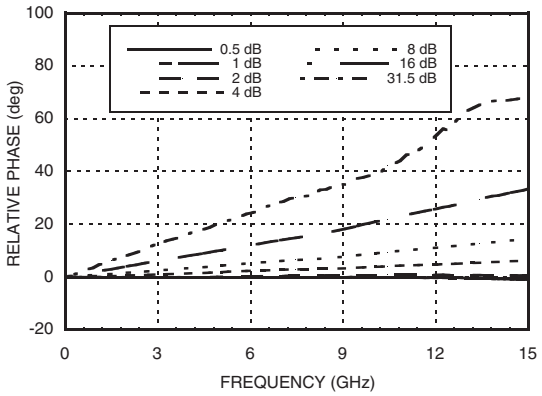
Bit Error vs. Attenuation State



Bit Error vs. Frequency
(Only Major States are Shown)



Relative Phase vs. Frequency
(Only Major States are Shown)



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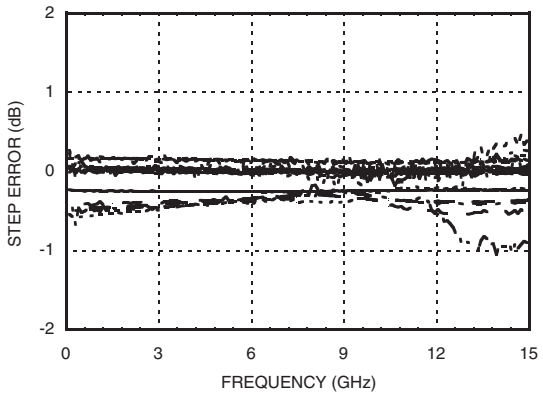
Worst Case Step Error Between Successive Attenuation States



Bias Voltage & Current

Vee Range= -5 Vdc ± 10%		
Vee (VDC)	Iee (Typ.) (mA)	Iee (Max.) (mA)
-5	2	5

Control Voltage

State	Bias Condition
Low	0 to -3V @ 35 µA Typ.
High	Vee to Vee +0.8V @ 5 µA Typ.

Truth Table

Control Voltage Input						Attenuation State RF1 - RF2
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	V6 0.5 dB	
Low	Low	Low	Low	Low	Low	Reference I.L.
Low	Low	Low	Low	Low	High	0.5 dB
Low	Low	Low	Low	High	Low	1 dB
Low	Low	Low	High	Low	Low	2 dB
Low	Low	High	Low	Low	Low	4 dB
Low	High	Low	Low	Low	Low	8 dB
High	Low	Low	Low	Low	Low	16 dB
High	High	High	High	High	High	31.5 dB

Any Combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

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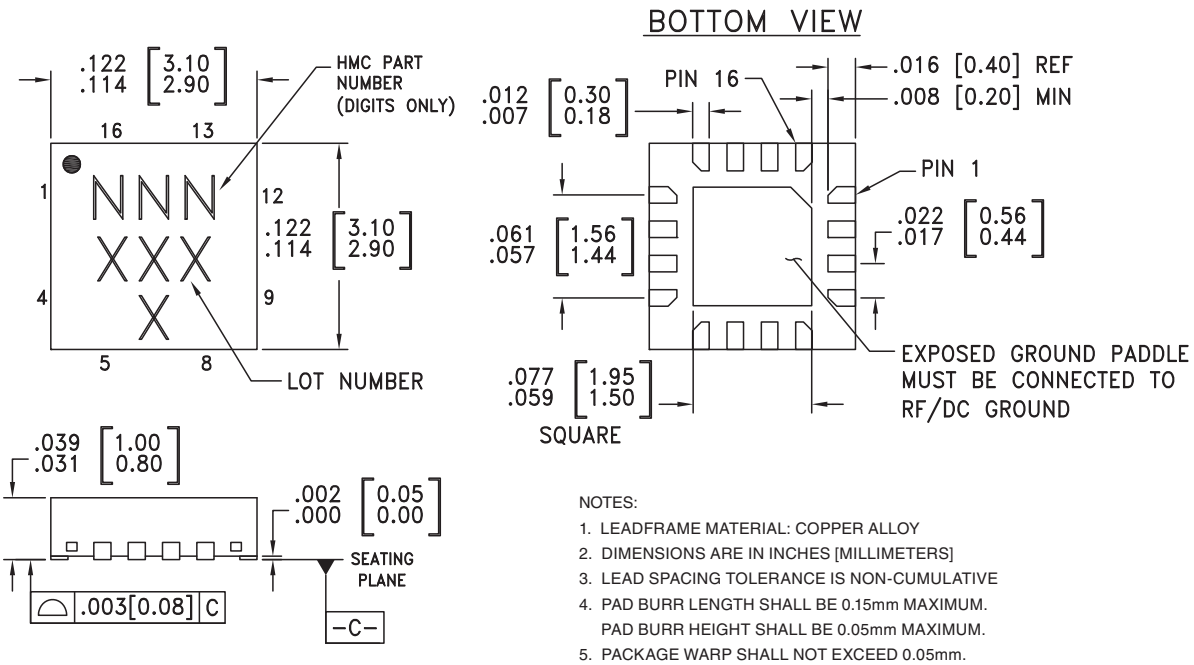
Absolute Maximum Ratings

Control Voltage (V1 to V6)	Vee - 0.5 Vdc
Bias Voltage (Vee)	-7 Vdc
Channel Temperature	150 °C
Thermal Resistance	330 °C/W
Storage Temperature	-65 to + 150 °C
Operating Temperature	-55 to +85 °C
RF Input Power (0.5 - 13 GHz)	+25 dBm

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

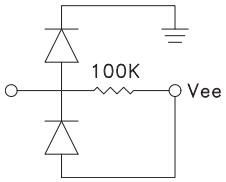
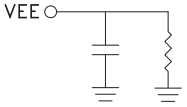
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

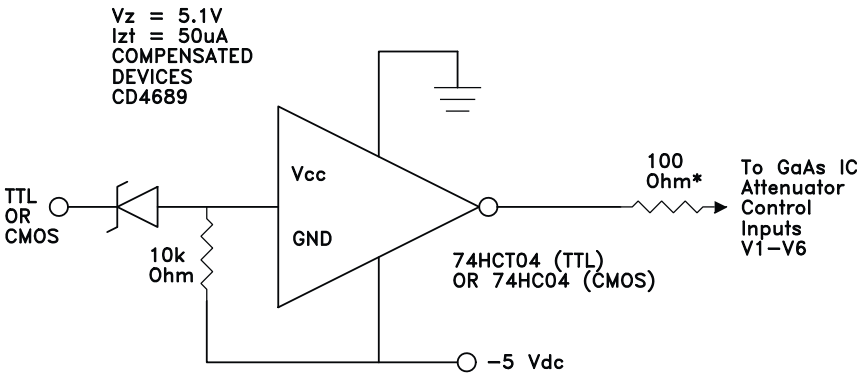
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC424LP3	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	424 XXXX
HMC424LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	424 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Description

Pad Number	Function	Description	Interface Schematic
1, 3, 10, 12	GND	Package bottom has an exposed metal paddle that must also be connected to RF ground	
2, 11	RFIN, RFOUT	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.	
4, 5, 6, 7, 8, 9	V6 - V1	See truth table and control voltage table.	
13, 14, 16	N/C	This pin should be connected to PCB RF ground to maximize performance	
15	VEE	Supply Voltage -5V ± 10%	

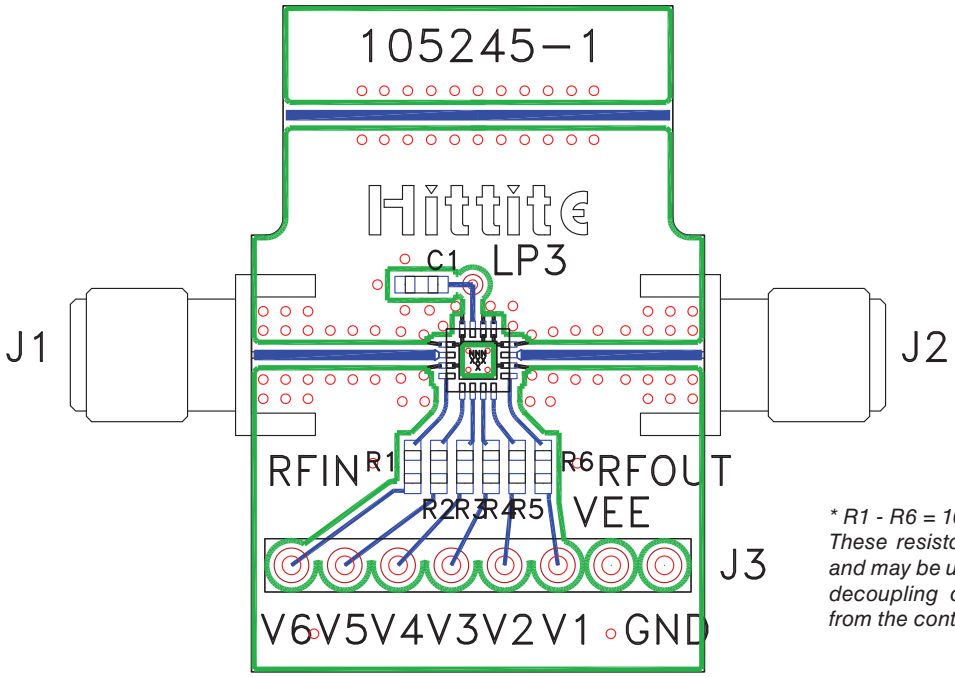
Suggested Driver Circuit *(One Circuit Required Per Bit Control Input)*



Simple driver using inexpensive standard logic ICs provides fast switching using minimum DC current.

** Recommended value to suppress unwanted RF signals at V1 - V6 control lines.*

Evaluation PCB



** R1 - R6 = 100 Ohm. These resistors are optional and may be used to enhance decoupling of the RF path from the control inputs.*

List of Materials for Evaluation PCB 105406 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	8 Pin DC Connector
C1	0.01 µF Capacitor, 0603 Pkg.
R1 - R6	100 Ohm Resistor, 0603 Pkg.
U1	HMC424LP3 / HMC424LP3E Digital Attenuator
PCB [2]	105245 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.