v03.0711

HMC570

GaAs MMIC I/Q DOWNCONVERTER 17 - 21 GHz

Typical Applications

The HMC570 is ideal for:

- Point-to-Point and Point-to-Multi-Point Radio
- Military Radar, EW & ELINT
- Satellite Communications

Features

10 dB Conversion Gain

Image Rejection: 17 dB

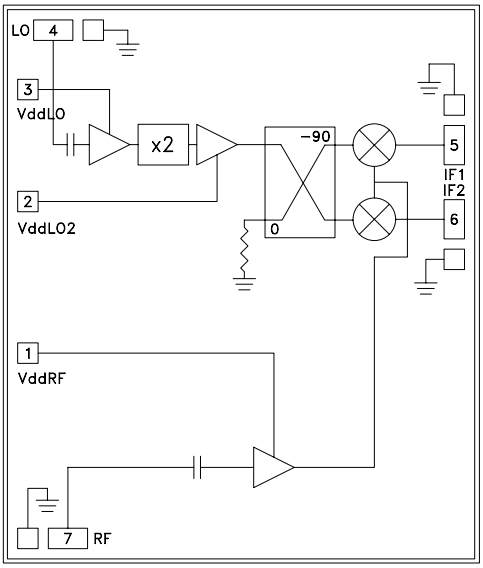
2 LO to RF Isolation: 35 dB

Noise Figure: 3 dB

Input IP3: +3 dBm

Die Size: 2.33 x 2.73 x 0.10 mm

Functional Diagram



General Description

The HMC570 is a compact GaAs MMIC I/Q downconverter chip which provides a small signal conversion gain of 10 dB with a noise figure of 3 dB and 17 dB of image rejection across the frequency band. The device utilizes an LNA followed by an image reject mixer which is driven by an active x2 multiplier. The image reject mixer eliminates the need for a filter following the LNA, and removes thermal noise at the image frequency. I and Q mixer outputs are provided and an external 90° hybrid is needed to select the required sideband. All data shown below is taken with the chip mounted in a 50 Ohm test fixture and includes the effects of 1 mil diameter x 20 mil length bond wires on each port. This product is a much smaller alternative to hybrid style image reject mixer downconverter assemblies.

Electrical Specifications, T_A = +25° C, IF = 100 MHz, LO = +4 dBm, Vdd = 3.5 Vdc*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF		17.7 - 19.7			17 - 21		GHz
Frequency Range, LO		7 - 12			7 - 12		GHz
Frequency Range, IF		DC - 3.5			DC - 3.5		GHz
Conversion Gain (As IRM)	9	10		9	12		dB
Noise Figure		3			4		dB
Image Rejection	14	17		14	22		dB
1 dB Compression (Input)	-7	-4		-10	-6		dBm
2 LO to RF Isolation	35	40		30	35		dB
2 LO to IF Isolation	28	30		25	30		dB
IP3 (Input)	-5	-2		-6	+3		dBm
Amplitude Balance		0.5			0.5		dB
Phase Balance		12			4		Deg
Total Supply Current		125	165		125	165	mA

*Data taken as IRM with external IF hybrid

Data Taken As IRM With External IF Hybrid

Conversion Gain vs. Temperature

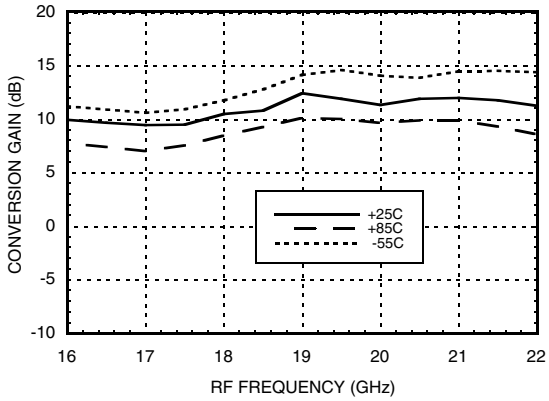
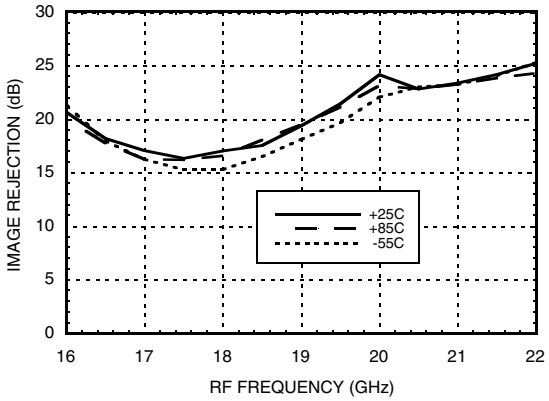
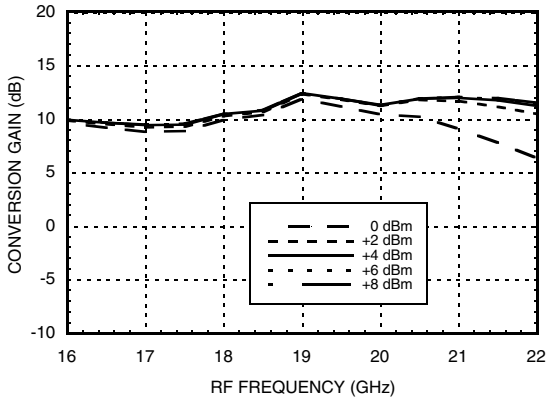


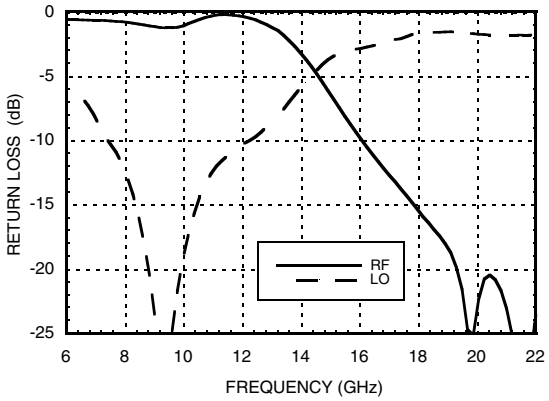
Image Rejection vs. Temperature



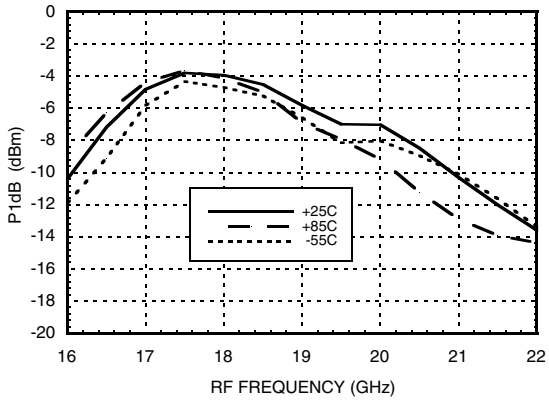
Conversion Gain vs. LO Drive



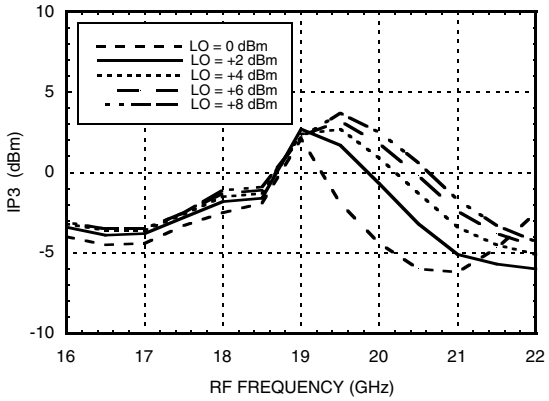
Return Loss



Input P1dB vs. Temperature

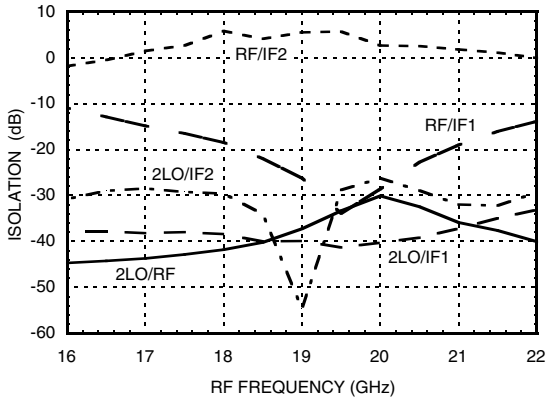


Input IP3 vs. LO Drive

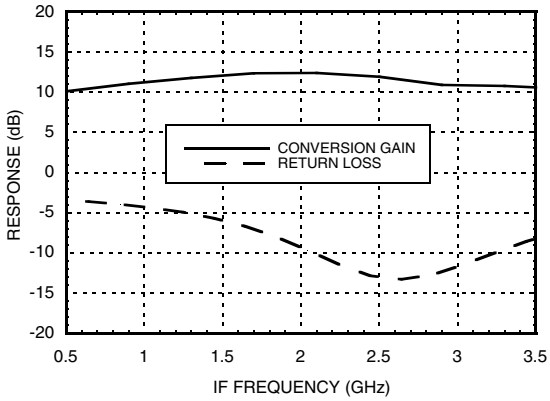


Quadrature Channel Data Taken Without IF Hybrid

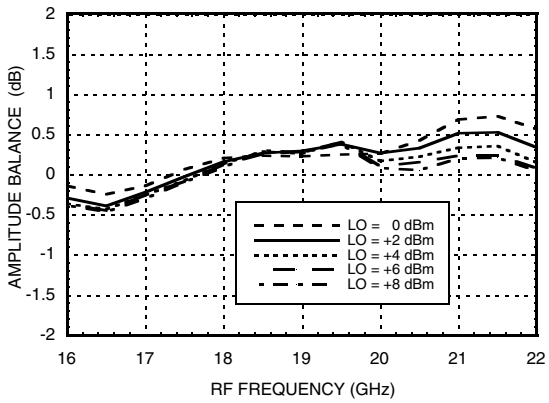
Isolations



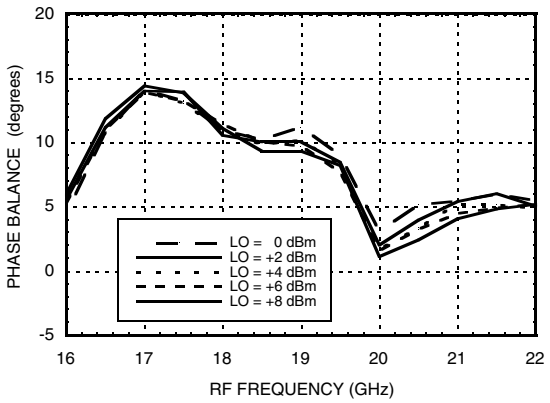
IF Bandwidth*



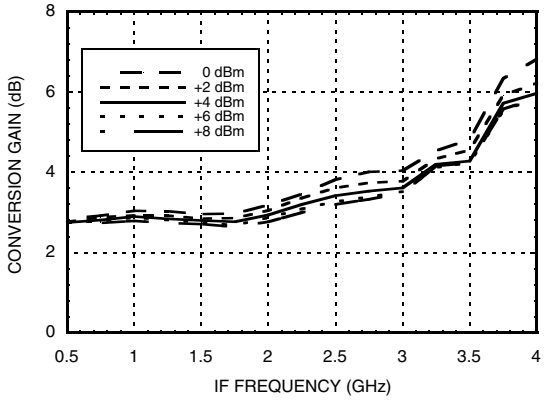
Amplitude Balance vs. LO Drive



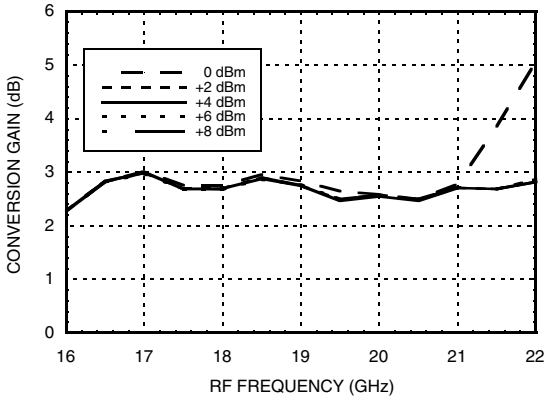
Phase Balance vs. LO Drive



Noise Figure vs. LO Drive, LO Frequency = 8.6 GHz



Noise Figure vs. LO Drive, IF Frequency = 100 MHz



** Conversion gain data taken with external IF hybrid, LO Frequency fixed at 8.6 GHz and RF varied*

MxN Spurious Outputs

	nLO				
mRF	0	1	2	3	4
0	xx	26	25	19	27
1	27	26	0	25	38
2	54	74	61	66	43
3	xx	xx	xx	79	76
4	xx	xx	xx	xx	xx

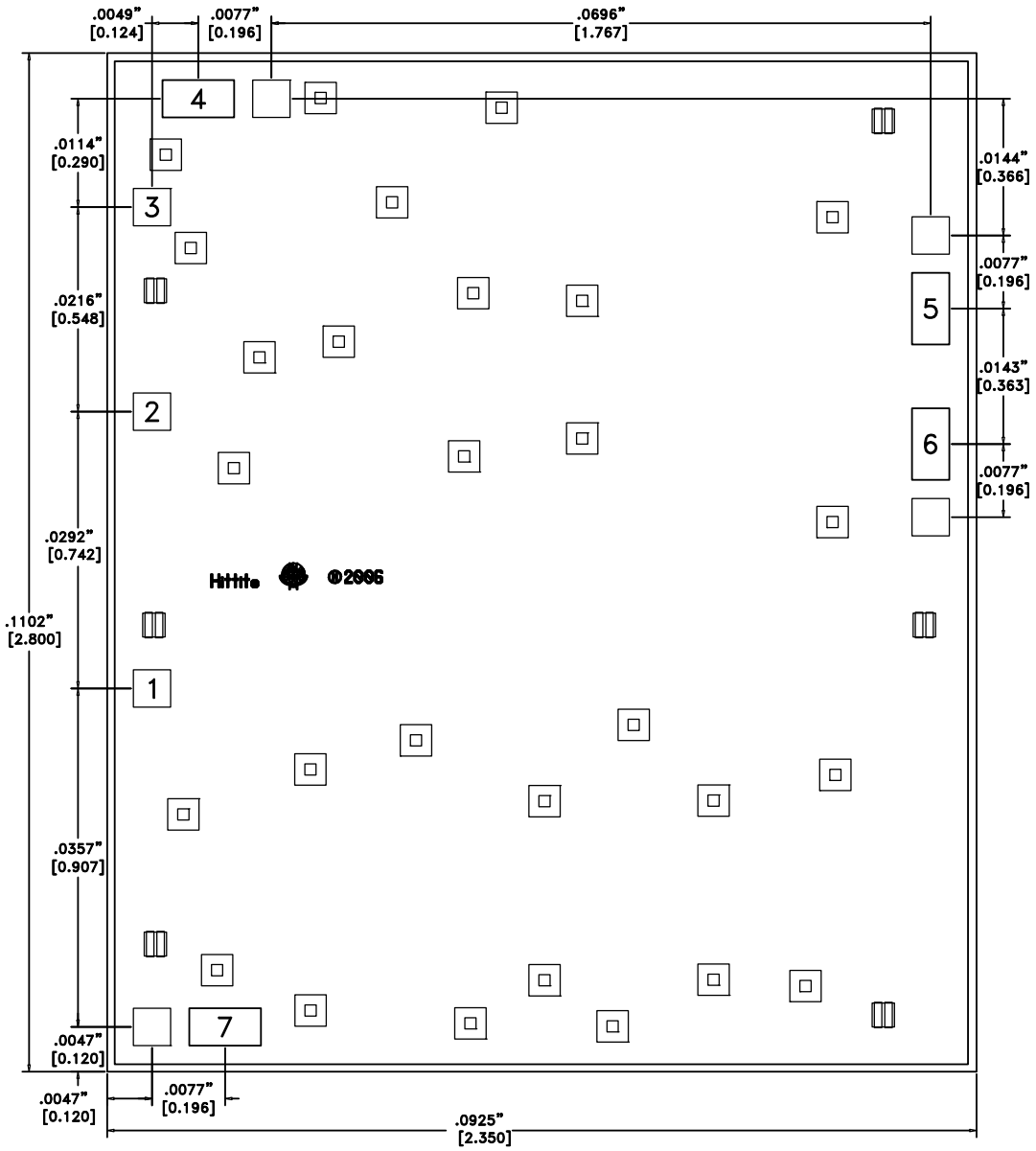
RF = 18 GHz @ -20 dBm
LO = 8.5 GHz @ +4 dBm
Data taken without IF hybrid
All values in dBc below IF power level (1RF -2LO = 1 GHz)

Absolute Maximum Ratings

RF	+2 dBm
LO Drive	+ 13 dBm
Vdd	5.5V
Channel Temperature	175°C
Continuous Pdiss (T=85°C) (derate 10.2 mW/°C above 85°C)	920 mW
Thermal Resistance (R_{TH}) (channel to package bottom)	98.3 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



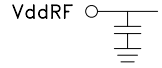
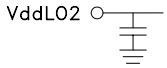
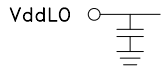
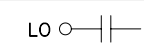
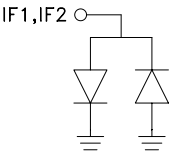
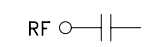
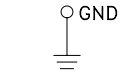
Die Packaging Information [1]

Standard	Alternate
GP-1 (Gel Pack)	[2]

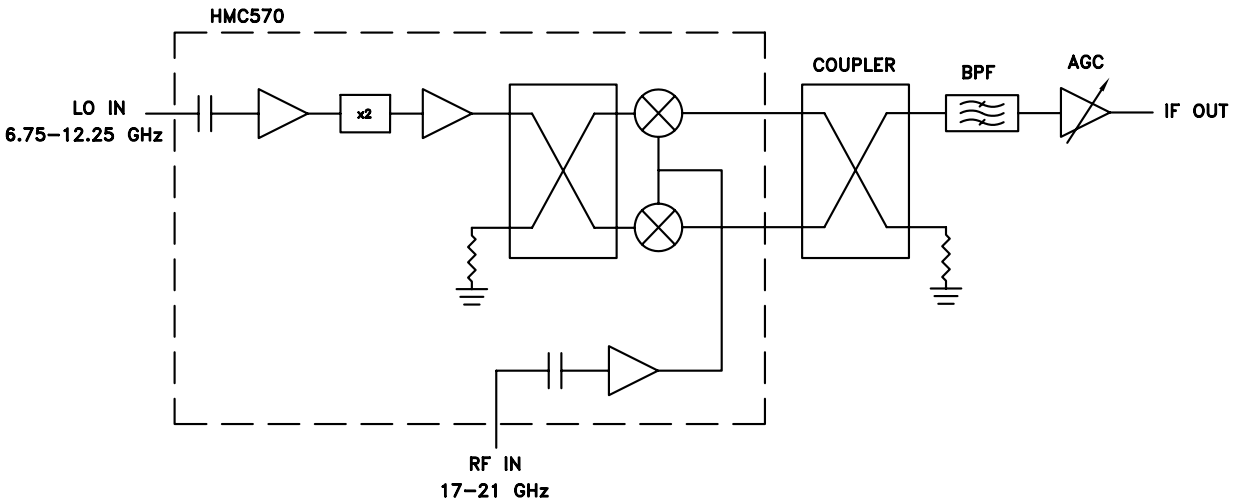
[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS 0.004"
3. BOND PAD METALIZATION: GOLD
4. BACKSIDE METALIZATION: GOLD
5. BACKSIDE METAL IS GROUND
6. OVERALL DIE SIZE ±0.002

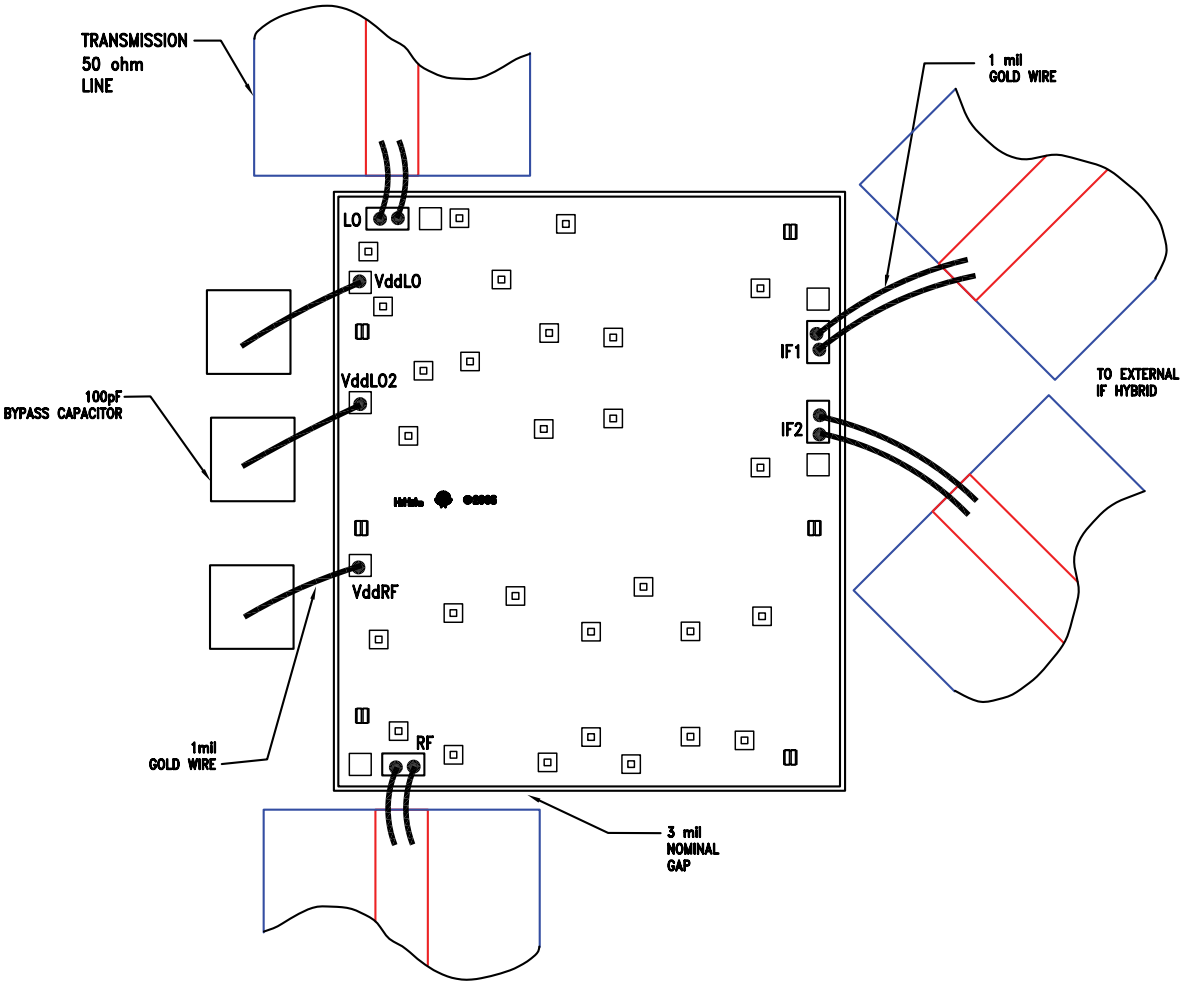
Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	VddRF	Power supply for RF LNA. External RF bypass capacitors are required.	
2	VddLO2	Power supply for second stage of LO amplifier. External RF bypass capacitors are required.	
3	VddLO	Power supply for first stage of LO amplifier. External RF bypass capacitors are required.	
4	LO	This pad is AC coupled and matched to 50 Ohms.	
5	IF1	This pad is DC coupled. For applications not requiring operation to DC, this port should be DC blocked externally using a series capacitor whose value has been chosen to pass the necessary frequency range. For operation to DC, this pad must not source /sink more than 3 mA of current or die non - function and possible die failure will result.	
6	IF2		
7	RF	This pad is AC coupled and matched to 50 Ohms.	
	GND	The backside of the die must be connected to RF/DC ground.	

Typical Application



Assembly Drawing



Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm (3 mils).

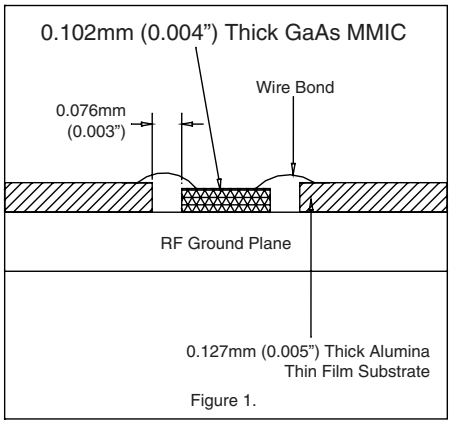


Figure 1.

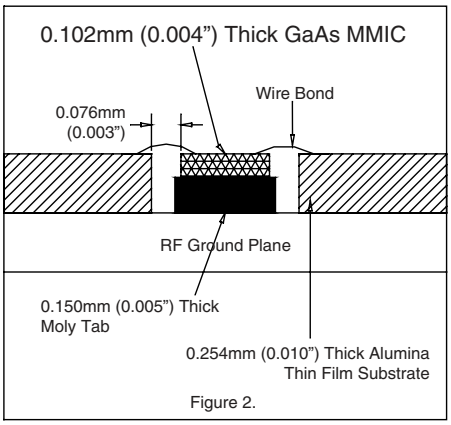


Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.
Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.
Static Sensitivity: Follow ESD precautions to protect against > ± 250V ESD strikes.
Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.
General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.
Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire is recommended. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).