Hittite MICROWAVE CORPORATION v00.0310

RoHS ✓ EARTH FRIENDLY

HMC905LP3E

6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Typical Applications

The HMC905LP3E is ideal for:

- LO Generation with Low Noise Floor
- Software Defined Radios
- Clock Generators
- Fast Switching Synthesizers
- Military Applications
- Test Equipment
- Sensors

Features

Low Noise Floor:
-164 dBc/Hz at 10 MHz Offset for N = 4

Programmable Frequency Divider, N = 1, 2, 3 or 4

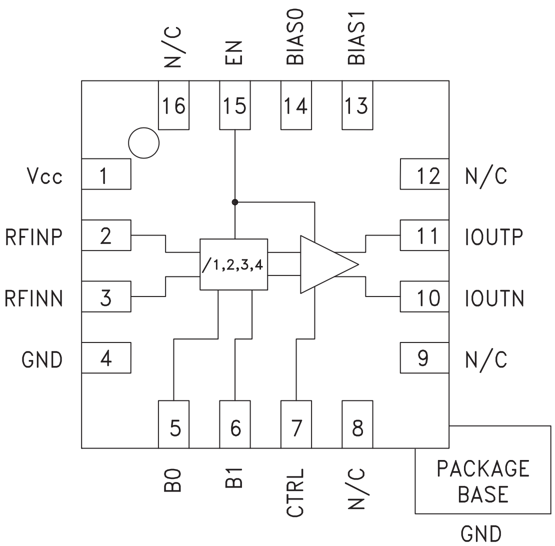
400 MHz to 6 GHz Input Frequency Range

Up to +6 dBm Output Power

Sleep Mode: Consumes <1 μA

16 Lead 3X3 mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC905LP3E is a SiGe BiCMOS low noise programmable frequency divider in a 3x3 mm leadless surface mount package. The circuit can be programmed to divide from N = 1 to N = 4 in the 400 MHz to 6 GHz input frequency range. The high level output power (up to 6 dBm single ended) with a very low SSB phase noise and 50% duty cycle makes this device ideal for low noise clock generation, LO generation and LO drive applications. Configurable bias and output power controls allow current consumption and output power control. The device incorporates a power down feature, good input to output isolation and fast start up time. The HMC905LP3E can be included into fast switching “ping-pong” applications.

Electrical Specifications, T_A = +25° C, Vcc = +3.3V, Z_O = 50Ω

Parameter	Conditions	Min.	Typ.	Max.	Units
RF Input Characteristics					
RF Input Frequency	Single-ended input	400		6000	MHz
RF Input Power	Single-ended input	0	6	10	dBm
Divider Output Characteristics					
Output Power (Single-ended Out)	-Typically, 50 ohms load resistors connected to Vcc - 1 bit programmable (CTRL digital signal) [1]	-2	3	6	dBm
SSB Phase Noise @ 10 kHz Offset	+6 dBm Input Power, 6 GHz input, Single-Ended Input and Output, Divide-by-4 [2]		-150		dBc/Hz
SSB Phase Noise @ 100 kHz Offset			-158		dBc/Hz
SSB Phase Noise @ 10 MHz Offset			-164		dBc/Hz
Start Up Time	EN bit from OFF to ON State (0V to Vcc)		200		ns
Power Down Time	EN bit from ON to OFF State (Vcc to 0V)		20		ns
Setting Time at Division Ratio Change	Delay from divide ratio change to output frequency change		25		ns

[1] See typical supply currents vs. BIAS0, BIAS1, CTRL bits table
[2] See Residual Phase Noise plot

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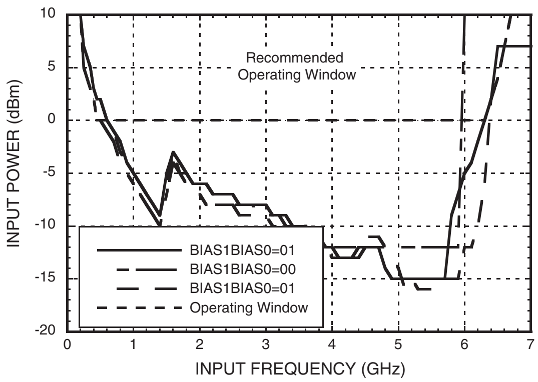
Electrical Specifications, T_A = +25° C, Vcc = +3.3V, Z_O = 50Ω *(Continued)*

Parameter	Conditions	Min.	Typ.	Max.	Units
Isolation SE Input to SE Output	EN bit OFF	-80		-30	dBc
Duty Cycle for Differential Mode			50		%
Logic Inputs					
VIH Input High Voltage		1.5		3.3	V
VIL Input Low Voltage		0		0.8	V
Power Supplies					
Vcc	Analog Supply (Low Noise LDO for good phase noise - HMC860LP3E)	3.15	3.3	3.45	V
Current Consumption	Total current vs. BIAS and CTRL bits [1]	82	100	125	mA
Sleep Current	EN = 0V		1		µA

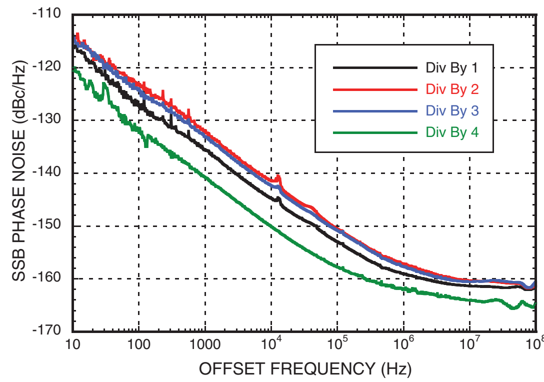
[1] The bias bits combination BIAS1 BIAS0 = 1 1 is not recommended

All data plots taken on Evaluation Board (schematic on page 10) single-ended with the unused output port 50 ohms terminated, Vcc = +3.3V, Ta=+25 °C, except stated otherwise

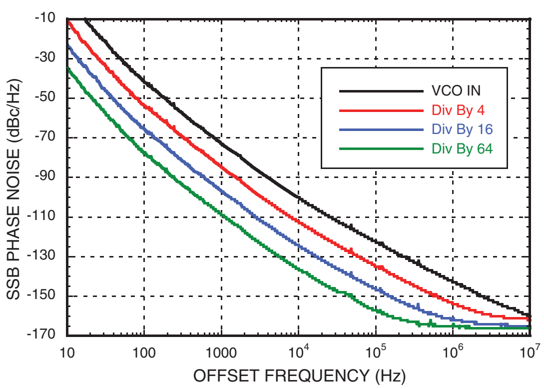
Input Sensitivity Window



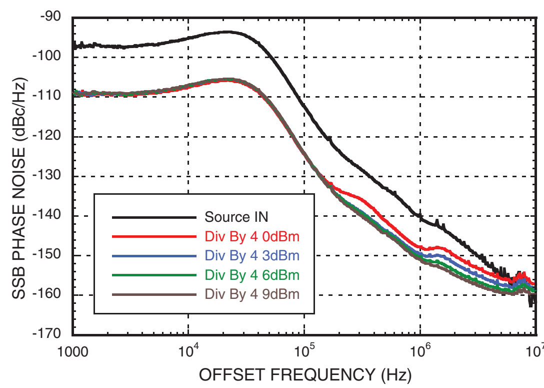
Residual Phase Noise Divide by 1, 2, 3 & 4 [2]



Phase Noise for 3 Cascaded HMC905LP3E from 6 GHz VCO



Output Phase Noise vs. Input Power Divide-by-4



[2] Fin = 6 GHz, Pin = 6 dBm, CTRL = 1, BIAS1 BIAS0 = 01

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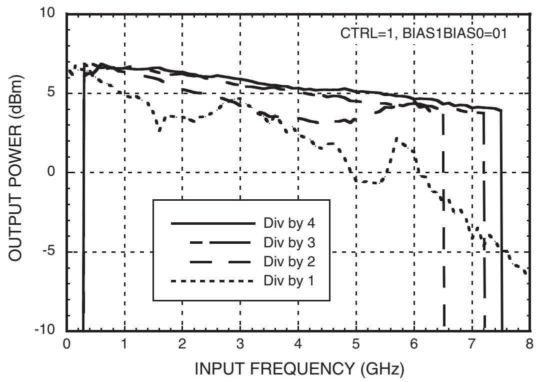
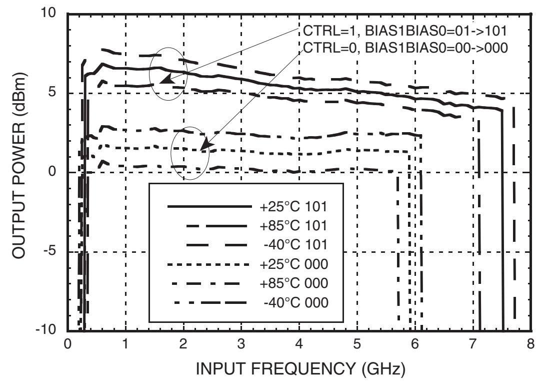
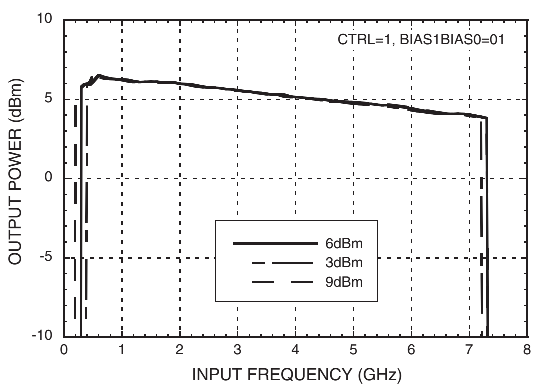
Pout vs. Division Ratio



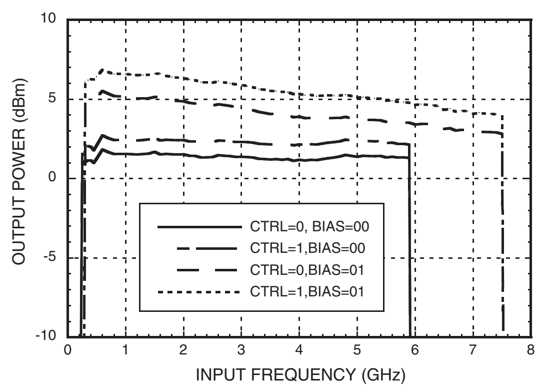
Output Power vs. Temperature Divide-by-4



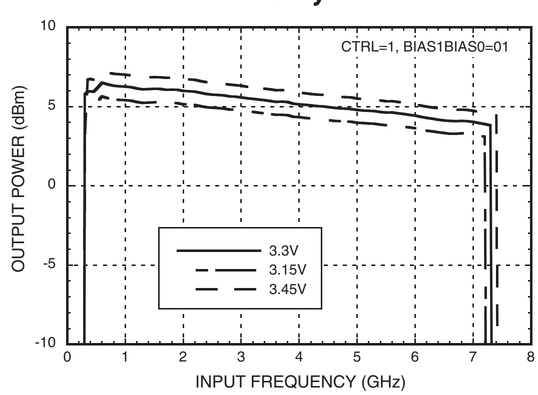
Output Power vs. Input Power Level Divide-by-4



Pout Divide-by-4 vs. CTRL & BIAS

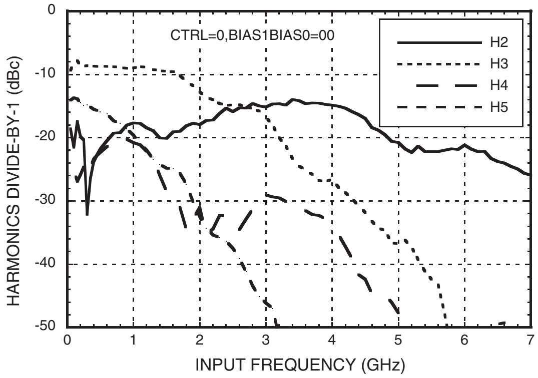


Output Power vs. Voltage Supply Divide-by-4

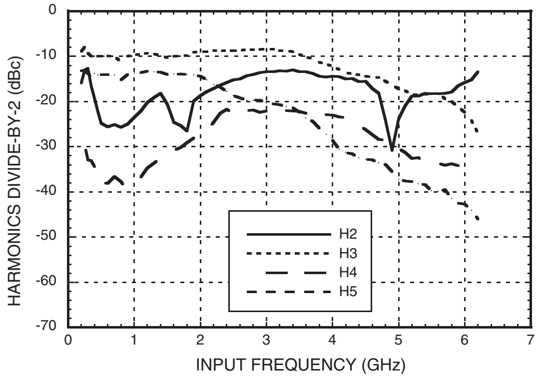


[1] CTRL = 0, BIAS1, BIAS1 BIAS0 = 00, Pin = 6 dBm

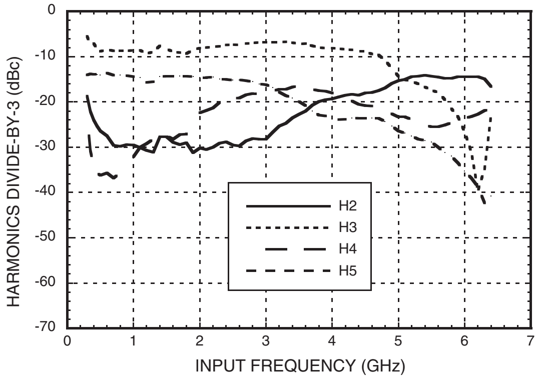
H2, H3, H4, H5 Harmonics, Divide-by-1 [1]



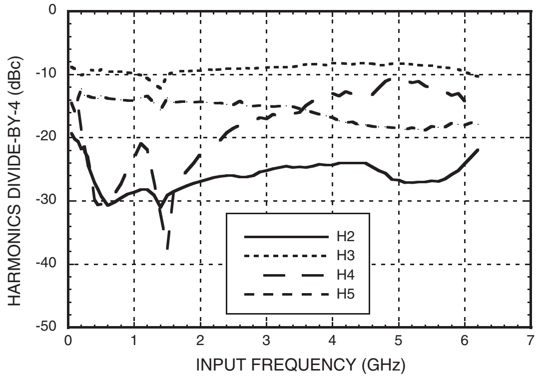
H2, H3, H4, H5 Harmonics, Divide-by-2 [1]



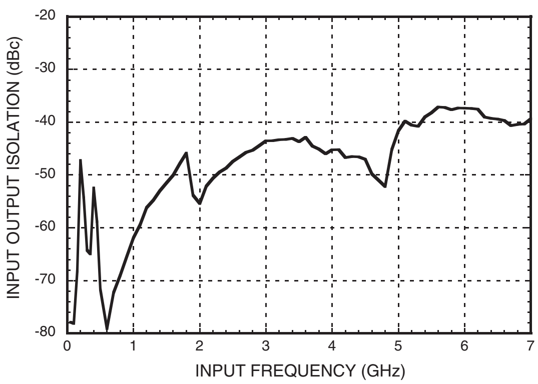
H2, H3, H4, H5 Harmonics, Divide-by-3 [1]



H2, H3, H4, H5 Harmonics, Divide-by-4 [1]



Input to Output Isolation



[1] CTRL = 0, BIAS1, BIAS1 BIAS0 = 00, Pin = 6 dBm

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Absolute Maximum Ratings

RF Input Power	12 dBm
Supply Voltage (Vcc)	3.6V
Control Inputs (B0, B1, CTRL, Bias0, EN)	3.6V
Junction Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 33 mW/ °C above 85 °C)	1.3 W
Thermal Resistance (Junction to ground paddle)	30 °C/W
Storage Temperature	-65 to +125 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Programming Truth Table for Frequency Division Ratios

B1	B0	Divide-by
0	0	1
0	1	2
1	0	3
1	1	4
0 = Logic Low 1 = Logic High		

Digital Control Input Voltages

State	B0, B1, CTRL, BIAS1, BIAS0, EN
Low	0 to 0.8V
High	1.5V to 3.3V

Typical Supply Current vs. EN, BIAS0, BIAS1 & CTRL Bits

EN	CTRL	BIAS1	BIAS0	3.3V Supply Typ. Current (mA)	Pout Typ. (dBm)	Noise Floor
1	0	0	0	84	1.5	Low
1	0	0	1	105	4.8	
1	0	1	0	98	3.9	
1	1	0	0	100	2.4	Better
1	1	0	1	120	6.3	Best
1	1	1	0	113	5.3	
0	x	x	x	0.001	-55	

Note: Currents for the divide-by-4 option, 2 GHz and 6 dBm input and 3.3V; for Vcc voltage supply from 3.15V to 3.45V, the HMC905LP3E total current is varying with a maximum of ~8% around typical values. With temperature, the total current is changing from +25°C to -40°C/+85°C with about ±3%.

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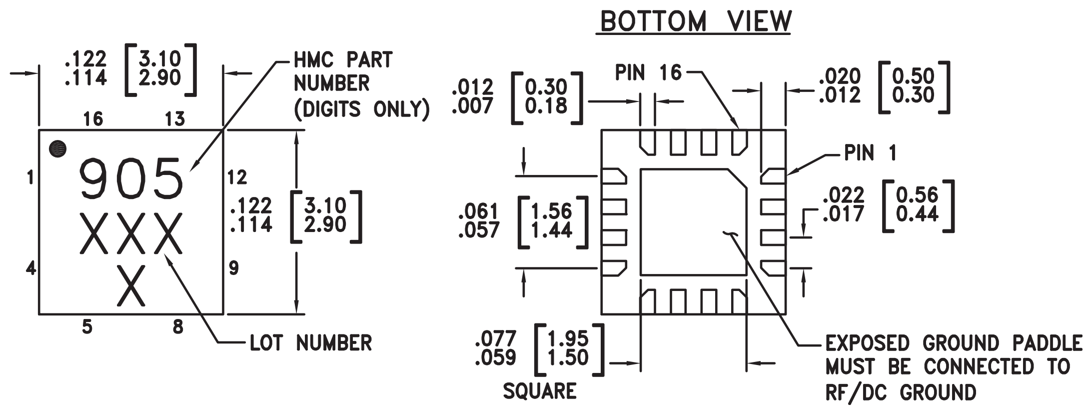
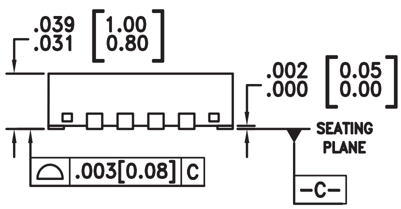
Outline Drawing





NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

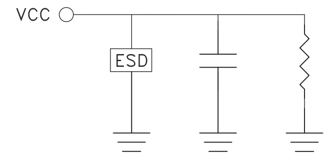
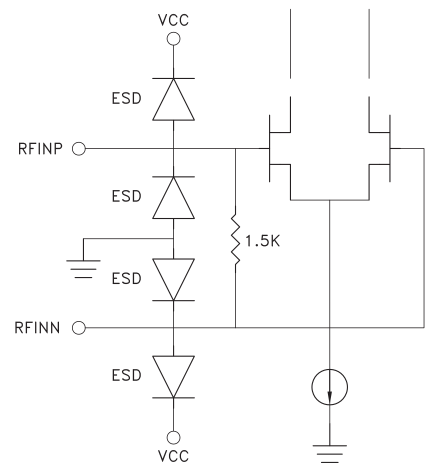
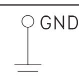
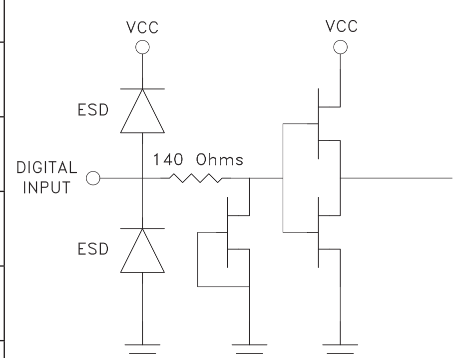
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC905LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	905 XXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

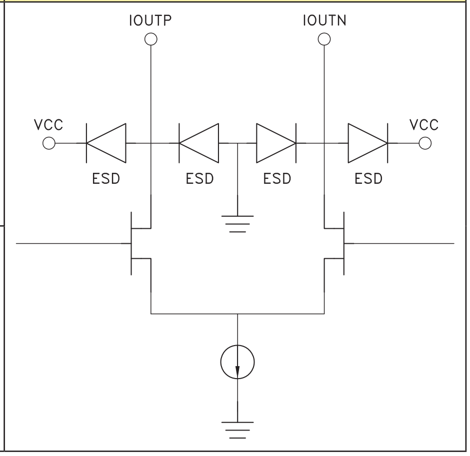
For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

Pin Description

Pin Number	Function	Description	Interface Schematic
1	Vcc	+3.3V Voltage Supply	
2	RFINP	RF Positive Input. Input is DC coupled, external DC blocks required.	
3	RFINN	RF Negative Input. Input is DC coupled, external DC blocks required.	
4	GND	This pin must be connected to RF/DC ground.	
5	B0	Division ratio (LSB) See programming truth table.	
6	B1	Division ratio (MSB) See programming truth table.	
7	CTRL	Divider Output Buffer Power Control	
13	BIAS1	Divider Core Bias Control	
14	BIAS0	Divider Core Bias Control	
15	EN	Chip Enable	
8, 9, 12, 16	N/C	No connection required. This pin may be connected to ground, without affecting performance.	

6 GHz LOW NOISE PROGRAMMABLE DIVIDER (N = 1 to 4)

Pin Description *(Continued)*

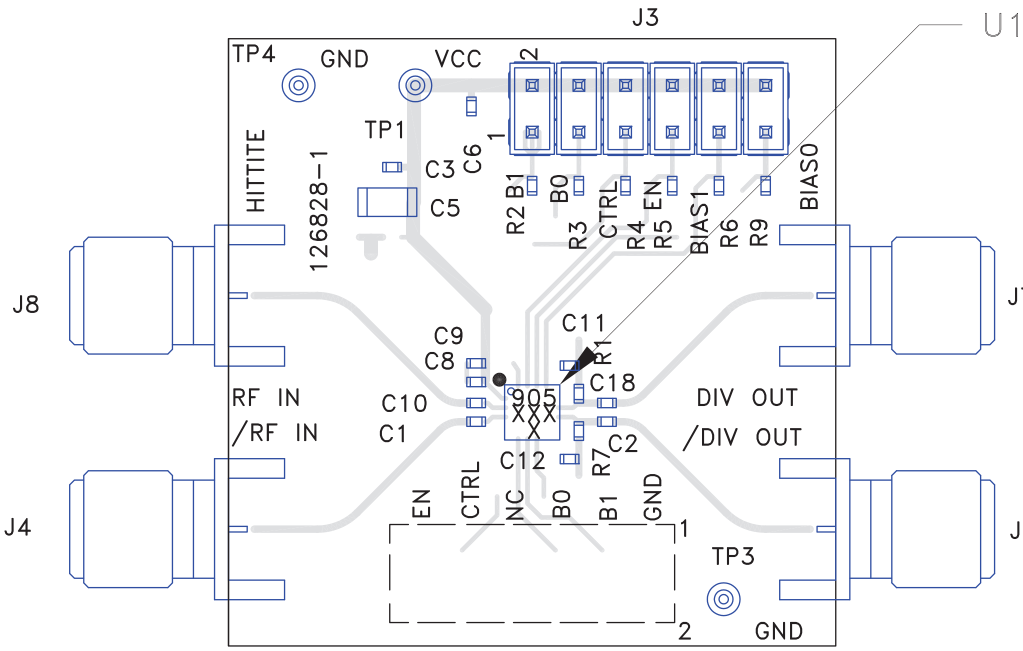
Pin Number	Function	Description	Interface Schematic
10	IOUTN	Divider Negative Output, Open Drain. Typically 50 Ohms connected to Vcc.	
11	IOUTP	Divider Positive Output, Open Drain. Typically 50 Ohms connected to Vcc.	

Application Note:

The HMC905LP3E is a high performance RF divider. Such dividers are high gain devices with internal feedback. The device will oscillate if used with AC coupled RF inputs and if no RF input is applied. Normally, if the RF input signal is removed the device should be disabled, or it should be placed in divide by 1 mode. The device is stable in divide by one mode with no RF input. The device will oscillate in divide 2, 3, or 4 modes with no RF input. In general, very small RF input levels will stop all oscillations. At the minimum rated RF input sensitivity level or higher, no oscillations or spurious signals exist and excellent low noise performance is achieved. For input frequency lower than 400 MHz, square wave input signal is recommended. For applications where the input frequency is bigger than ~5.5 GHz, it is recommended either to use differential drive, or to increase the divider core current (bias settings BIAS1BIAS0=01 or 10).

For single ended applications, apply the signal on the positive input RFinp and terminate the unused output with 50 ohms.

Evaluation PCB



List of Materials for Evaluation PCB 126830 [1]

Item	Description
J3	DC Connector
J1, J4, J7, J8	SMA SRI Connector
C1, C2, C10 - C12, C18	1nF Capacitor, 0402 Pkg
C3, C6, C9	100nF Capacitor, 0402 Pkg
C5	10uF Capacitor, 1206 Pkg
C8	10pF Capacitor, 0402 Pkg
R1, R7	51 Ohms, Resistor, 0402 Pkg
R2 - R6, R9	100 kOhms, Resistor, 0402 Pkg
TP1, TP3, TP4	PC Compact SMT
U1	HMC905LP3E Programmable Divider
PCB [2]	126828 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic