MAAD-009194-000100

Constant Phase Digital Attenuator
31.0 dB, 5-Bit, TTL Driver, DC-3.0 GHz

Rev. V2

Features

- Attenuation: 1 dB steps to 31 dB
- Minimal Phase Variation over Attenuation Range
- Low DC Power Consumption
- Hermetic Surface Mount Package
- Integral TTL Driver
- 50 Ω Nominal Impedance
- RoHS* Compliant and 260°C Reflow Compatible

Description

The MAAD-009194-000100 is a GaAs FET 5-bit digital attenuator with a 1 dB minimum step size and 31 dB total attenuation. The design has been optimized to minimize phase variation over the attenuation range. This attenuator and integral TTL driver is in a hermetically sealed ceramic 16-lead surface mount package.

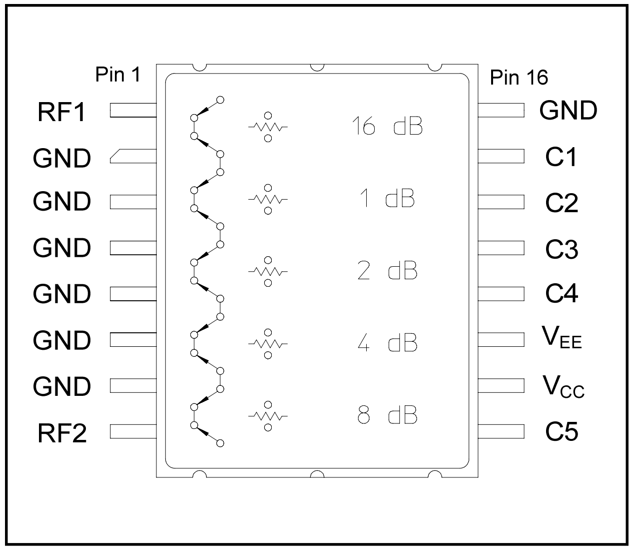
The MAAD-009194-000100 is ideally suited for use where accuracy, fast switching, very low power consumption and low intermodulation products are required. Typical applications include dynamic range setting in precision receiver circuits and other gain/leveling control circuits. Environmental screening is available. Contact the factory for information.

Ordering Information [1]

Part Number	Package
MAAD-009194 –000100	Bulk Packaging
MAAD-009194 -0001TB	Sample Test Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration[2]

Pin No.	Function	Pin No.	Function
1	RF1	9	C5
2	GND	10	V_{CC}
3	GND	11	V_{EE}
4	GND	12	C4
5	GND	13	C3
6	GND	14	C2
7	GND	15	C1
8	RF2	16	GND

2. The metal bottom of the case must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Electrical Specifications: $T_A = 25°C, Z_0 = 50\ \Omega, V_{CC} = +5.0V, V_{EE} = -5.0V$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Operating Power	—	dBm	—	—	+20
Reference Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 3.0 GHz	dB	—	—	4.5 5.0 5.3
Attenuation Accuracy[3]	Any Single Bit, DC - 3.0 GHz Any Combination of Bits, DC - 3.0 GHz	± (0.3 +3% of attenuation setting in dB) dB ± (0.3 +4% of attenuation setting in dB) dB			
Phase Accuracy Relative to Reference Loss State	Any Single Bit, DC - 2.0 GHz Any Single Bit, 2.0 - 3.0 GHz Any Combination of Bits, DC - 1.0 GHz Any Combination of Bits, 1.0 - 2.0 GHz Any Combination of Bits, 2.0 - 3.0 GHz	deg	± 3 ± 5 ± 4 ± 11 ± 18		
VSWR	DC - 3.0 GHz	Ratio	—	—	1.8:1
Trise, Tfall	10% to 90% RF, 90% to 10% RF	ns	See Table 1		
Ton, Toff	1.3 V Control to 90% RF, 1.3 V Control to 10% RF	ns	See Table 1		
1 dB Compression[4]	Reference State 0.05 GHz 0.5 - 3.0 GHz	dBm	—	>+26 >+26	—
Input IP3	For two-tone Input Power up to +5 dBm 0.05 GHz 0.5 - 3.0 GHz	dBm	—	+39 +41	—
Input IP2	For two-tone Input Power up to +5 dBm 0.05 GHz 0.5 - 3.0 GHz	dBm	—	+45 +68	—
V_{CC} V_{EE}	— —	V	4.5 -8.0	5.0 -5.0	5.5 -4.5
VIL VIH	LOW-level input voltage HIGH-level input voltage	V	0.0 2.0	0.0 5.0	0.8 5.0
I_{IN} (Input Leakage Current)	$V_{IN} = V_{CC}$ or GND	µA	-1	—	1
Icc (Quiescent Supply Current)	$V_{CNTRL} = V_{CC}$ or GND	µA	—	250	400
ΔIcc (Additional Supply Current Per TTL Input Pin)	V_{CC} = Max, $V_{CNTRL} = V_{CC} - 2.1$ V	mA	—	—	1.5
I_{EE}	V_{EE} min to max, V_{IN} = VIL or VIH	mA	-1.0	-0.2	—
Thermal Resistance θjc	—	°C/W	—	50	—

3. This attenuator is guaranteed monotonic.
4. 1 dB Compression was measured up to +26 dBm, which is the absolute maximum rating for this device.

Absolute Maximum Ratings [5,6]

Parameter	Absolute Maximum
Max Input Power DC - 3.0 GHz	+26 dBm
V_{CC}	$-0.5V \le V_{CC} \le +7.0V$
V_{EE}	$-8.5V \le V_{EE} \le +0.5V$
$V_{CC} - V_{EE}$	$-0.5V \le V_{CC} - V_{EE} \le 14.5V$
V_{IN} [7]	$-0.5V \le Vin \le V_{CC} + 0.5V$
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C

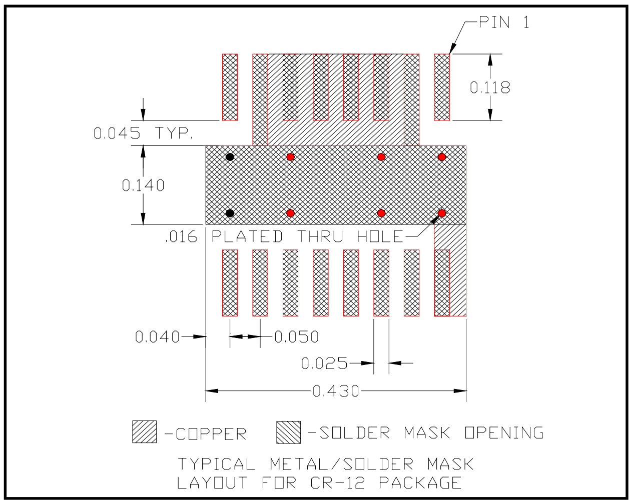
5. Exceeding any one or combination of these limits may cause permanent damage to this device.
6. M/A-COM Technology does not recommend sustained operation near these survivability limits.
7. Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Truth Table (Digital Attenuator)

Control Inputs					
C5	C4	C3	C2	C1	Attenuation
0	0	0	0	0	Reference
0	0	0	0	1	16 dB
0	0	0	1	0	1 dB
0	0	1	0	0	2 dB
0	1	0	0	0	4 dB
1	0	0	0	0	8 dB
1	1	1	1	1	31 dB

0 = TTL Low; 1 = TTL High

Recommended PCB Configuration



Typical Switching Speed (table 1)

Testing Condition	Ton	Trise	Units
Ref. State ↔ 1 dB	3.6	3.6	µs
Ref. State ↔ 2 dB	3.6	3.6	µs
Ref. State ↔ 4 dB	3.7	3.7	µs
Ref. State ↔ 8 dB	3.3	3.3	µs
Ref. State ↔ 16 dB	4.5	4.5	µs
Ref. State ↔ 31 dB	30.5	30.5	µs

Typical Input IP2 and IP3 [8]

Attenuation	IP2			IP3			Units
	50 MHz	500 MHz	2 GHz	50 MHz	500 MHz	2 GHz	
Reference State	50	68	70	39	43	42	dBm
1 dB	50	68	70	39	43	37	dBm
2 dB	50	68	70	39	43	37	dBm
4 dB	50	68	70	37	37	37	dBm
8 dB	50	68	70	37	37	37	dBm
16 dB	50	68	65	31	32	32	dBm
31 dB	50	50	50	31	30	29	dBm

8. IP2 and IP3 are measured with two-tone inputs F1 and F2 up to +5 dBm with 1 MHz spacing.

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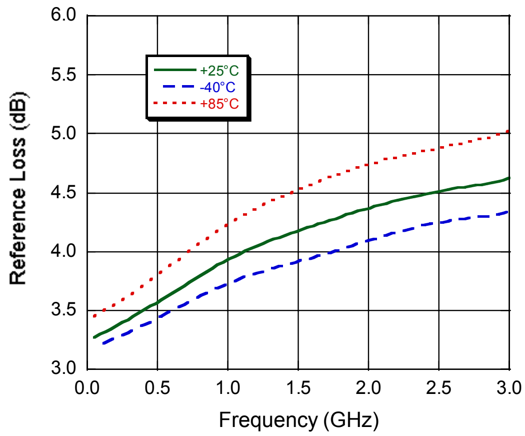
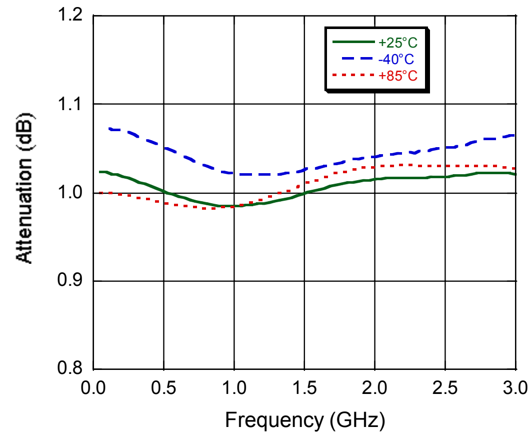
Typical Performance Curves

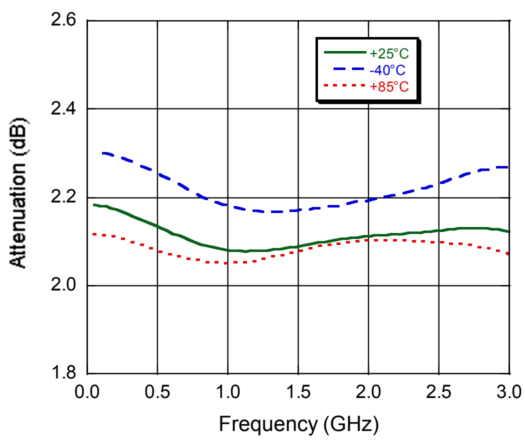
Reference Loss vs. Frequency



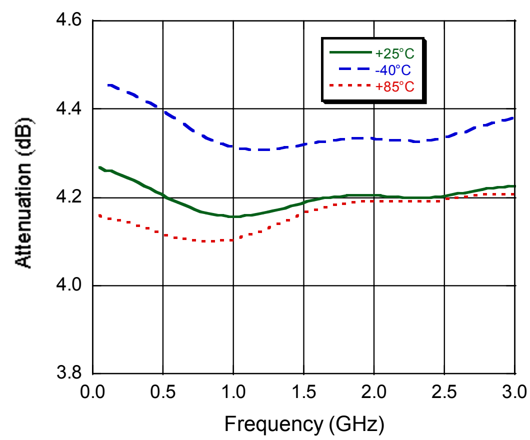
Attenuation - 1 dB Bit vs. Frequency



Attenuation - 2 dB Bit vs. Frequency



Attenuation - 4 dB Bit vs. Frequency



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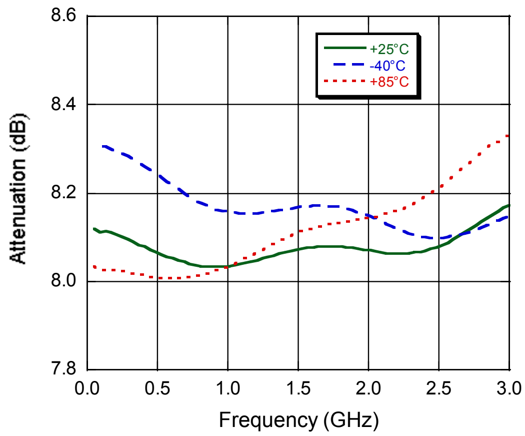
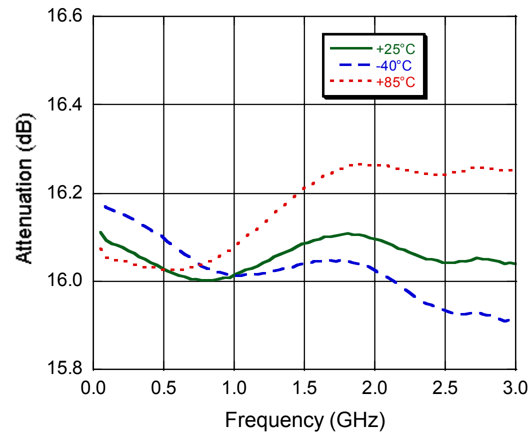
Typical Performance Curves

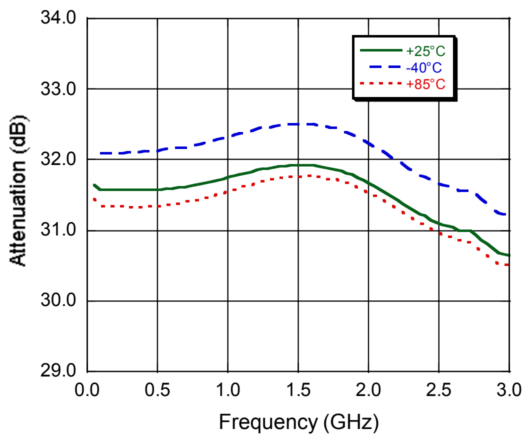
Attenuation - 8 dB Bit vs. Frequency



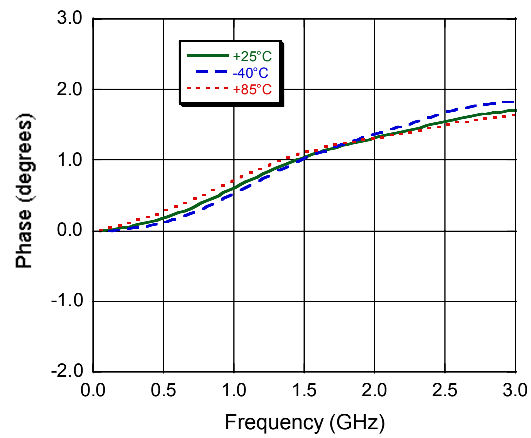
Attenuation - 16 dB Bit vs. Frequency



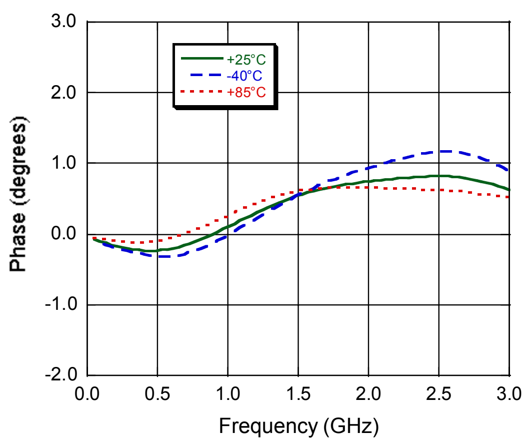
Attenuation - 31 dB Bit vs. Frequency



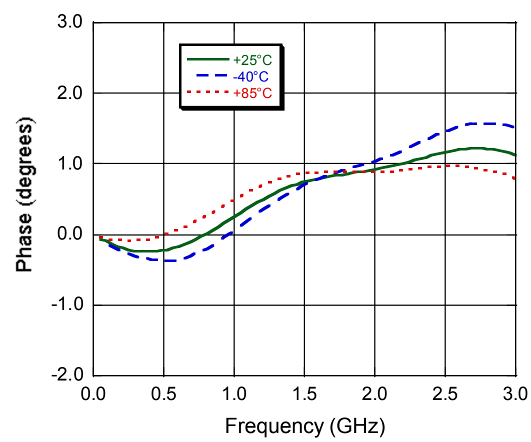
Phase - 1 dB Bit vs. Frequency
Relative to Reference Loss State



Phase - 2 dB Bit vs. Frequency
Relative to Reference Loss State

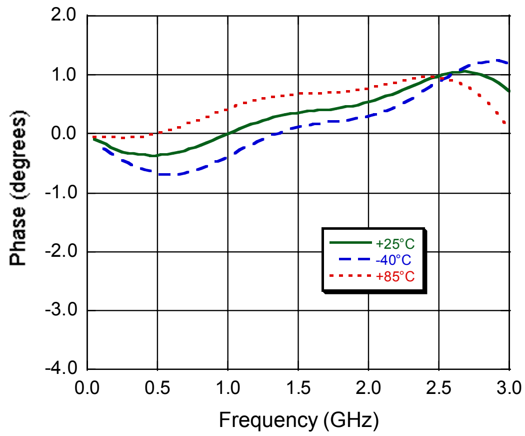


Phase - 4 dB Bit vs. Frequency
Relative to Reference Loss State

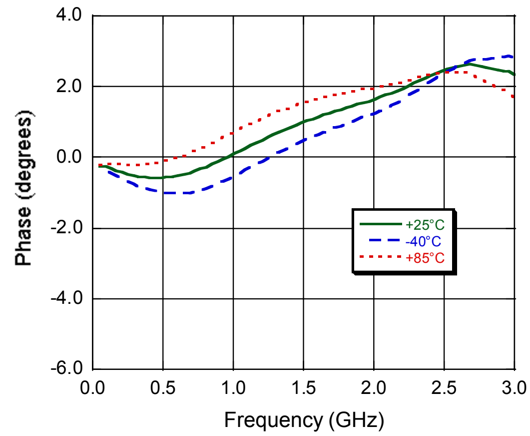


Typical Performance Curves

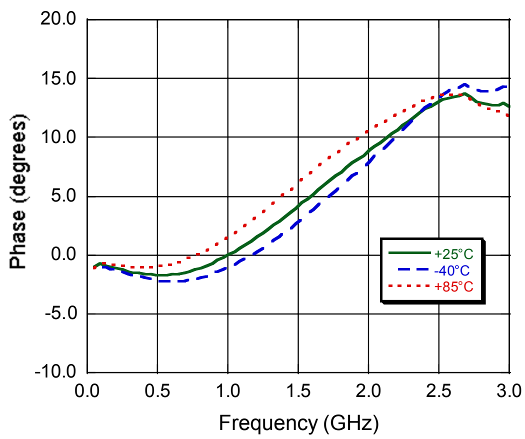
Phase - 8 dB Bit vs. Frequency
Relative to Reference Loss State



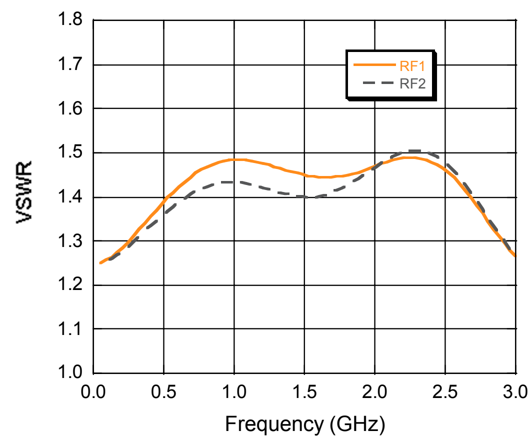
Phase - 16 dB Bit vs. Frequency
Relative to Reference Loss State



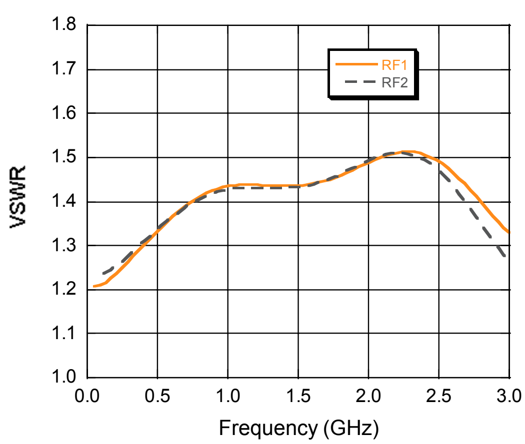
Phase - 31 dB Attenuation vs. Frequency
Relative to Reference Loss State



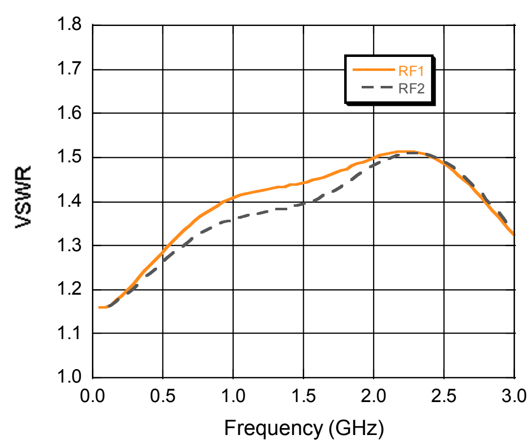
VSWR vs. Frequency
Relative to Reference Loss State



VSWR - 1 dB Bit vs. Frequency



VSWR - 2 dB Bit vs. Frequency



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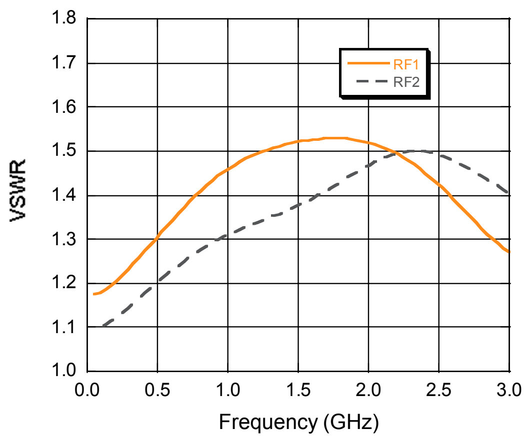
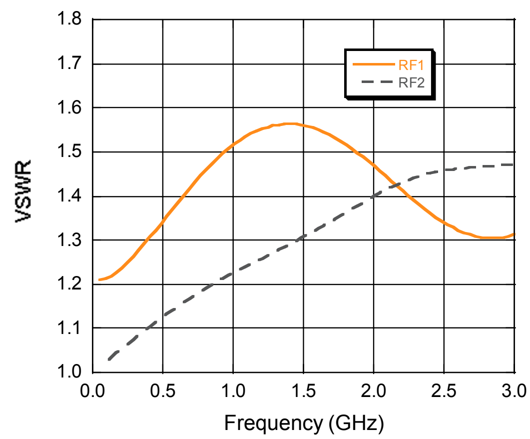
Typical Performance Curves

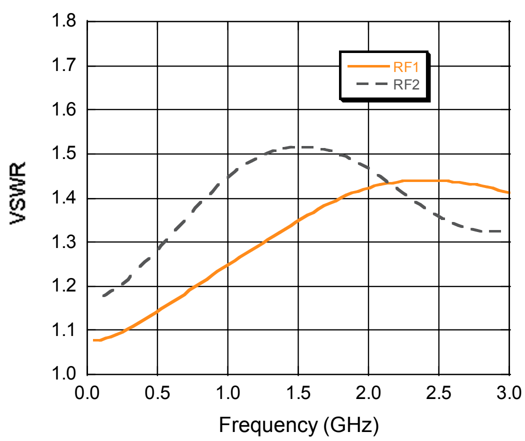
VSWR - 4 dB Bit vs. Frequency



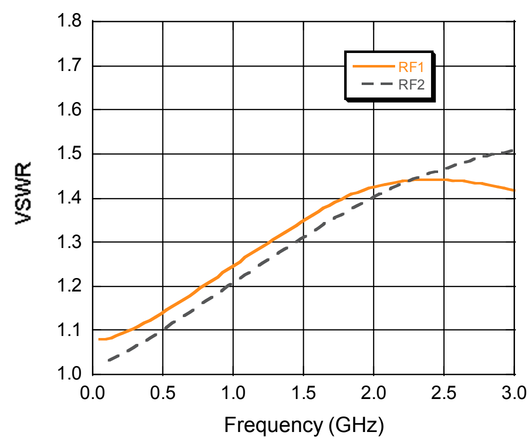
VSWR - 8 dB Bit vs. Frequency



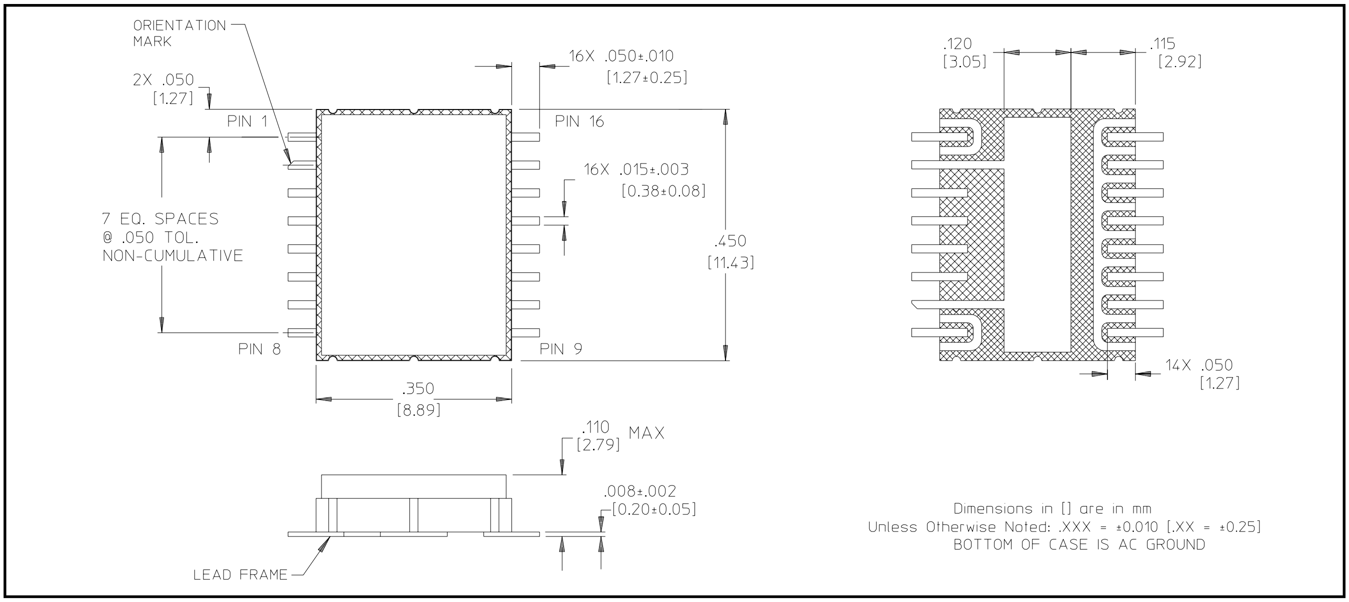
VSWR - 16 dB Bit vs. Frequency



VSWR - 31 dB Attenuation vs. Frequency



Lead-Free, CR-12 Ceramic Package†



† Reference Application Note M538 for lead-free solder reflow recommendations.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.