MADR-009443-000100

Quad Driver for GaAs FET or PIN Diode Switches and Attenuators

Rev. V1

Features

- High Voltage CMOS Technology
- Four Channel
- Positive Voltage Control
- CMOS device using TTL input levels
- Low Power Dissipation
- Low Cost 4x4 mm, 20-lead PQFN Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- 260°C Reflow Compatible

Description

The MADR-009443-000100 is a four channel driver used to translate TTL control inputs into gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to +2.0V (relative to GND) to optimize the intermodulation products of FET control devices at low frequencies. For driving PIN Diode circuits, the outputs are nominally switched between +5V & -5V. The actual driver output voltages will be lower when driving large currents due to the resistance of the output devices.

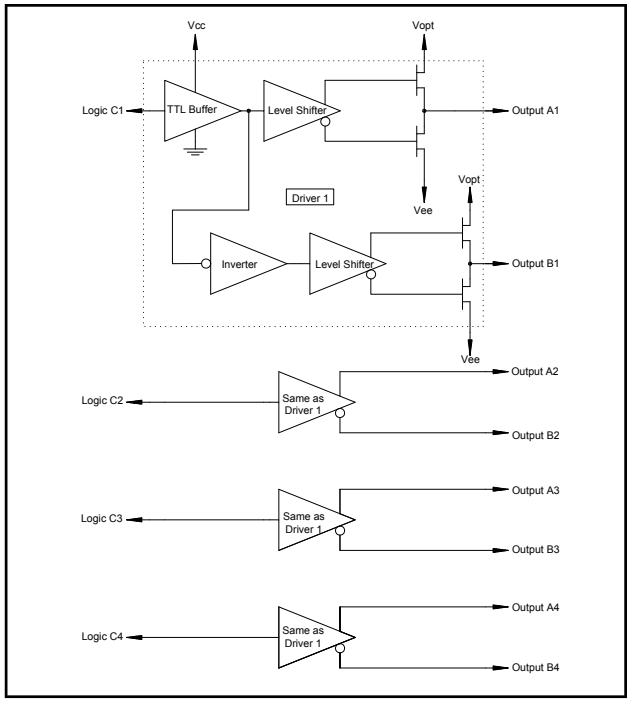
Ordering Information

Part Number	Package
MADR-009443-000100	Bulk Packaging
MADR-009443-0001TR	1000 piece reel
MADR-009190-000DIE	Die [1]

Note: Reference Application Note M513 for reel size information.

1. See the MADR-009190-000100 data sheet for the die outline
2. The exposed pad centered on the package bottom may be isolated or connected to ground.

Functional Schematic



Pin Configuration [2]

Pin No.	Function	Pin No.	Function
1	Ground	11	Output A4
2	NC	12	Output B4
3	NC	13	Vee
4	Output A1	14	NC
5	Output B1	15	Vcc
6	Output A2	16	C4
7	Output B2	17	C3
8	NC	18	C2
9	Output A3	19	C1
10	Output B3	20	Vopt

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Visit www.macomtech.com for additional data sheets and product information.

Guaranteed Operating Ranges (for driving FET or PIN devices) [3,4,7]

Symbol	Parameter	Unit	Min.	Typ.	Max.
V_{CC}	Positive DC Supply Voltage	V	4.5	5.0	5.5
V_{EE}	Negative DC Supply Voltage	V	-10.5	-5.0	-4.5
V_{OPT} [5]	Optional DC Output Supply Voltage	V	0	—	V_{CC}
V_{OPT} - V_{EE}	Negative Supply Voltage Range	V	4.5	Note 6	16.0
V_{CC} - V_{EE}	Positive to negative Supply Range	V	9.0	10.0	16.0
T_{OPER}	Operating Temperature	°C	-40	+25	+85
I_{OH}	DC Output Current - High	mA	-35	—	—
I_{OL}	DC Output Current - Low	mA	—	—	35
T_{rise}, T_{fall}	Maximum Input Rise or Fall Time	ns	—	—	500

3. Unused logic inputs must be tied to either GND or V_{CC}.
4. All voltages are relative to GND.
5. V_{OPT} is grounded in most cases when FETs are driven. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies, V_{OPT} can be increased to between 1.0 and 2.0V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current that is on the GaAs MMICs will increase when positive controls are applied.
6. When this driver is used to drive PIN diodes, V_{OPT} is often set to +5.0V, with V_{EE} set to -5.0V.
7. 0.01 uF decoupling capacitors are required on the power supply lines.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Truth Table

Input	Outputs	
Cn	An	Bn
Logic “0”	V_{EE}	V_{OPT}
Logic “1”	V_{OPT}	V_{EE}

DC Characteristics over Guaranteed Operating Range

Symbol	Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{IH}	Input High Voltage	Guaranteed High Input Voltage	V	2.0	—	—
V_{IL}	Input Low Voltage	Guaranteed Low Input Voltage	V	—	—	0.8
V_{OH}	Output High Voltage	I_{OH} = -0.5 mA	V	V_{OPT} - 0.1	—	—
V_{OL}	Output Low Voltage	I_{OL} = 0.5 mA	V	—	—	V_{EE} + 0.1
I_{IN}	Input Leakage Current (per Input)	V_{IN} = V_{CC} or GND, V_{EE} = min, V_{CC} = max, V_{OPT} = min or max	nA	-250	—	250
I_{OH}	DC Output Current—High (per Output)	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V	mA	-35	—	—
I_{OL}	DC Output Current—Low (per Output)	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V	mA	—	—	35
I_{OH_SPIKE}	Peak Spike Output Current (Rising Edge) (per Output)	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V, C_L = 25 pF	mA	—	35	—
I_{OL_SPIKE}	Peak Spike Output Current (Falling Edge) (per Output)	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V, C_L = 25 pF	mA	—	50	—
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5V, V_{CC} = 5.5V, V_{OPT} = 5.5V, No Output Load	µA	—	—	20
ΔI_{CC}	Additional Supply Current (per TTL Input pin)	V_{CC}= max, V_{IN} = V_{CC} -2.1V	mA	—	—	1.0
I_{EE}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5V, V_{CC} = 5.5V, V_{OPT} = 5.5V, No Output Load	µA	—	—	20
I_{OPT}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5V, V_{CC} = 5.5V, V_{OPT} = 5.5V, No Output Load	µA	—	—	20
R_{NFET}	Output Resistance NFET On (to V_{EE})	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V, V_{OUT} = -4.9V +25°C, Note 8	Ω	—	40	—
R_{PFET}	Output Resistance PFET On (to V_{OPT})	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V, V_{OUT} = 4.9V +25°C, Note 8	Ω	—	45	—

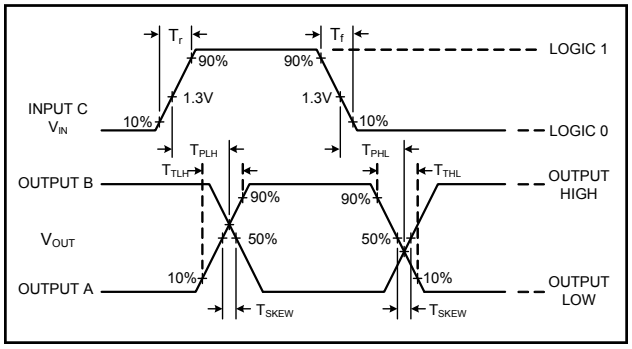
8. See plot of R_{NFET} and R_{PFET} for variations over temperature for 4.99k and 82 Ω loads (Note that this corresponds to 1 mA and 33 mA currents at 25°). Vout is approximate for 1 mA load.

AC Characteristics Over Guaranteed Operating Range (Driving FETs) [9]

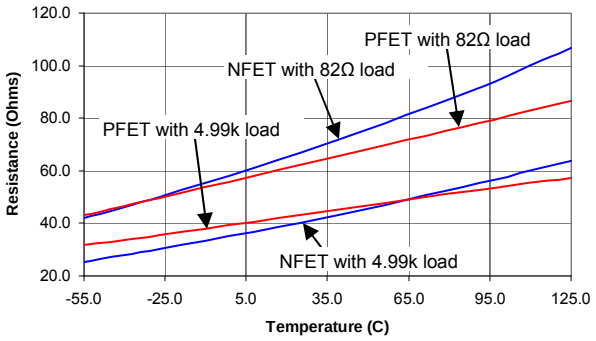
		Typical performance			
Symbol	**Parameter**	**-40°C**	**+85°C**	**+85°C**	**Unit**
T_{PLH}	Propagation Delay	20	22	25	ns
T_{PHL}	Propagation Delay	20	22	25	ns
T_{TLH}	Output Transition Time (Rising Edge)	5	5	8	ns
T_{THL}	Output Transition Time (Falling Edge)	4	5	6	ns
T_{skew}	Delay Skew	2	2	2	ns
PRF (max)	50% Duty Cycle	DC	—	10	MHz
C_{IN}	Input Capacitance	5	5	5	pF
C_{PDC}	Power Dissipation Capacitance [10]	50	50	50	pF
C_{PDE}	Power Dissipation Capacitance [10]	100	100	100	pF

9. V_{CC} = 4.5V, V_{OPT} - V_{EE} = min or max, V_{OPT} = 0V, C_L = 25 pF, Input Logic "0" = 0.0V, Input logic "1" = 3.0V, Trise, Tfall = 6 ns.
10. Total Power Dissipation is calculated by the following formula: PD = $V_{CC}^2 f C_{PDC} + V_{EE}^2 f C_{PDE}$.

Switching Waveforms—Driving FETs



Output Resistance vs. Temperature[11]



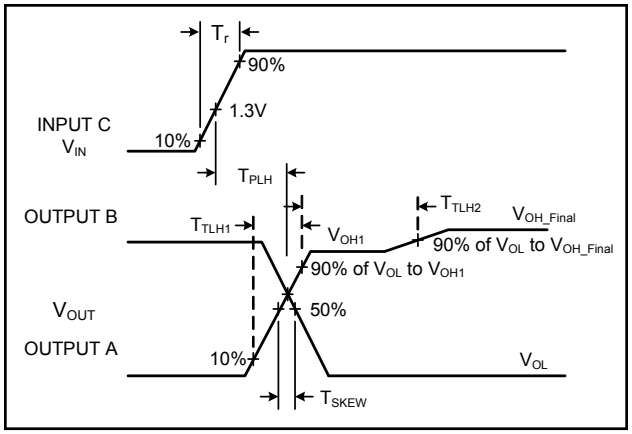
11. Output resistance were measured under the condition of V_{CC} = 5.0V, V_{OPT} = 5.0V, and V_{EE} = -5.0V, with load resistors from outputs to ground.

AC Characteristics Over Guaranteed Operating Range (Driving PIN Diodes) [12]

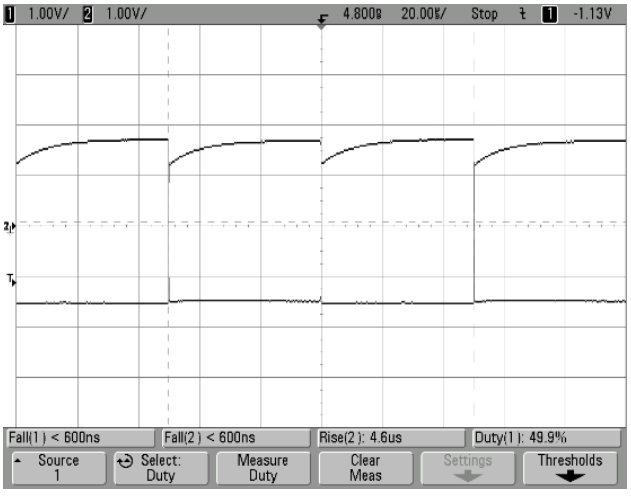
		Typical performance			
Symbol	**Parameter**	**-40°C**	**+85°C**	**+85°C**	**Unit**
T_{PLH}	Propagation Delay	20	22	25	ns
T_{PHL}	Propagation Delay	20	22	25	ns
T_{TLH1}	Output Transition Time (Rising Edge)	5	5	8	ns
T_{TLH2}	Output Setttling Time (Rising Edge)	2	5	6	µs
T_{THL}	Output Transition Time (Falling Edge)	4	4	5	ns
T_{skew}	Delay Skew	2.5	2.5	2.5	ns
PRF (max)	50% Duty Cycle	DC	—	10	MHz
C_{IN}	Input Capacitance	5	5	5	pF
C_{PDC}	Power Dissipation Capacitance [13]	45	45	45	pF
C_{PDE}	Power Dissipation Capacitance [13]	180	180	180	pF
C_{PDO}	Power Dissipation Capacitance [13]	135	135	135	pF

12. V_{CC} = 5.0V, V_{EE} = -5V, V_{OPT} = 5.0V, C_L = 25 pF, input LOGIC "1" = 3V, LOGIC "0" = 0V, Trise, Tfall = 6 ns
13. Total Power Dissipation is calculated by the following formula: PD = $V_{CC}^2 f C_{PDC} + V_{EE}^2 f C_{PDE} + V_{OPT}^2 f C_{PDO}$

Switching Waveforms—Driving PINs [14]



Switching Waveforms—Driving 35 mA load with 25 pF load capacitance



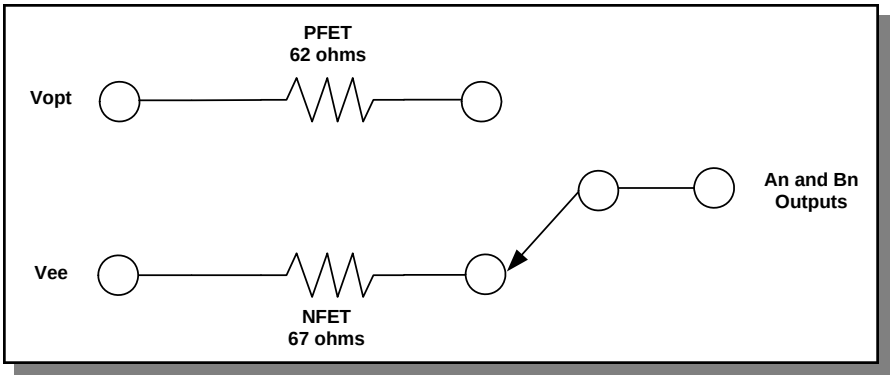
14. This effect is only apparent when driving high currents and only occurs on the rising edges. On the schematic in "Typical Application for a SPDT Switch" note that the rising edge turns on the shunt diodes. There will be a slight effect on isolation over time, but the insertion loss should not be affected.

Absolute Maximum Ratings[15]

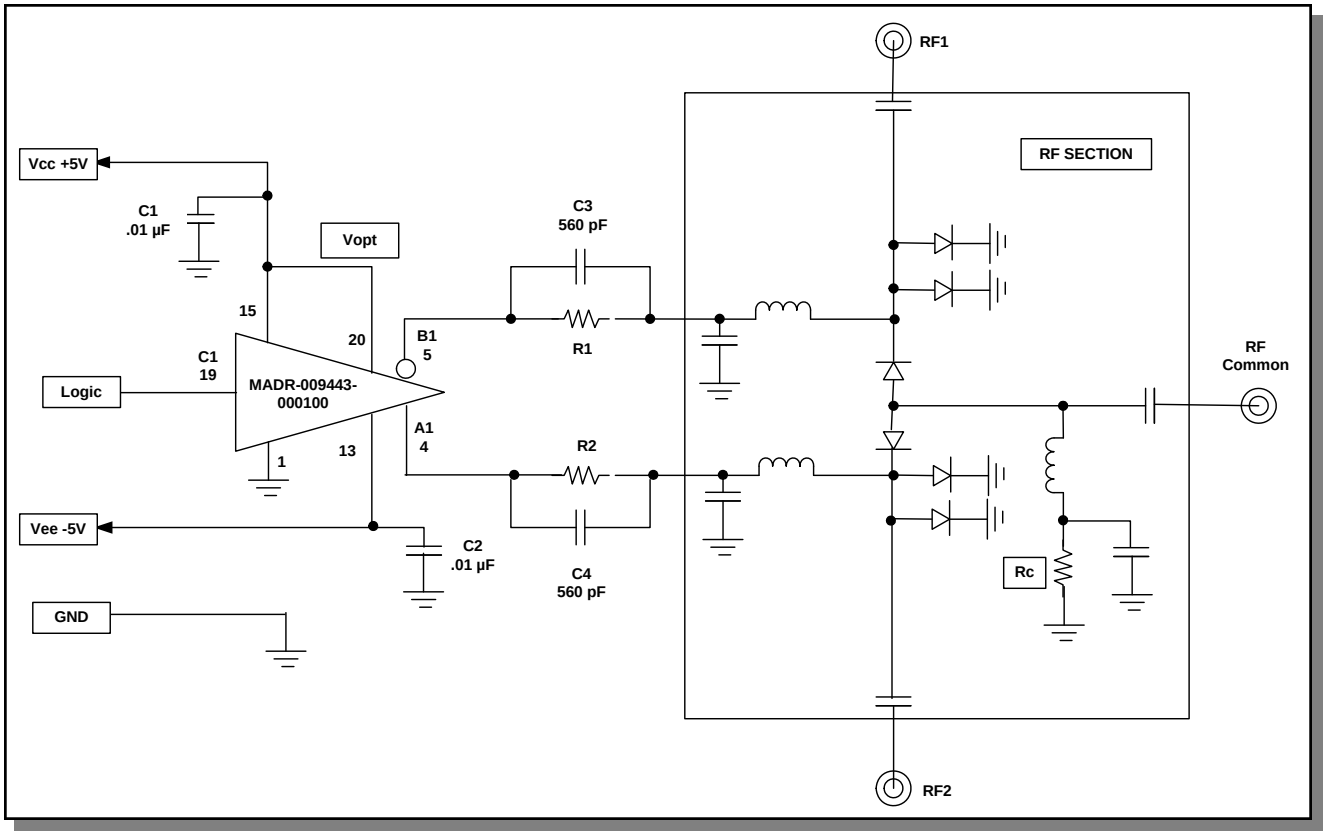
Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	-0.5	7.0	V
I_{CC}	Positive DC Supply Current (-0.5V ≤ V_{IN} ≤ 0.8V; 2.0V ≤ V_{IN} ≤ V_{CC} + 0.5V; V_{CC} - V_{IN} ≤ 7.0V)	—	20	mA
V_{EE}	Negative DC Supply Voltage	-11.0	0.5	V
I_{EE}	Negative DC Supply Current (per Output) [16]	-50	—	mA
V_{OPT}	Optional DC Output Supply Voltage	-0.5	V_{CC} +0.5	V
I_{OPT}	Optional DC Output Supply Current (per Output) [16]	—	50	V
V_{OPT} - V_{EE}	Output to Negative Supply Voltage Range	-0.5	18.0	V
V_{CC} - V_{EE}	Positive to Negative Supply Voltage Range	-0.5	18.0	V
V_{IN}	DC Input Voltage	-0.5 Note 17	V_{CC} +0.5	V
I_{IN}	DC Input Current	-25	25	mA
V_O	DC Output Voltage	V_{EE} – 0.5	V_{OPT} + 0.5	V
P_D[18]	Power Dissipation in Still Air	—	500	mW
T_{OPER}	Operating Temperature	-55	125	°C
T_{STG}	Storage Temperature	-65	150	°C
ESD	ESD Sensitivity	2.0	—	kV

15. All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.
16. The maximum I_{EE} and I_{OPT} are specified under the condition of V_{CC} = 5.5V, V_{EE} = -5.5V, V_{OPT} = 5.5V, and the total power dissipation is within 500 mW in still air.
17. If V_{CC} ≥ 6.5V, then the minimum for V_{IN} is V_{CC} - 7.0V.
18. Derate -7 mW/°C from 65°C to 85°C.

Equivalent Output Circuit for An and Bn Outputs (33 mA load at 25°)



Typical Application for a SPDT Switch [19,20]



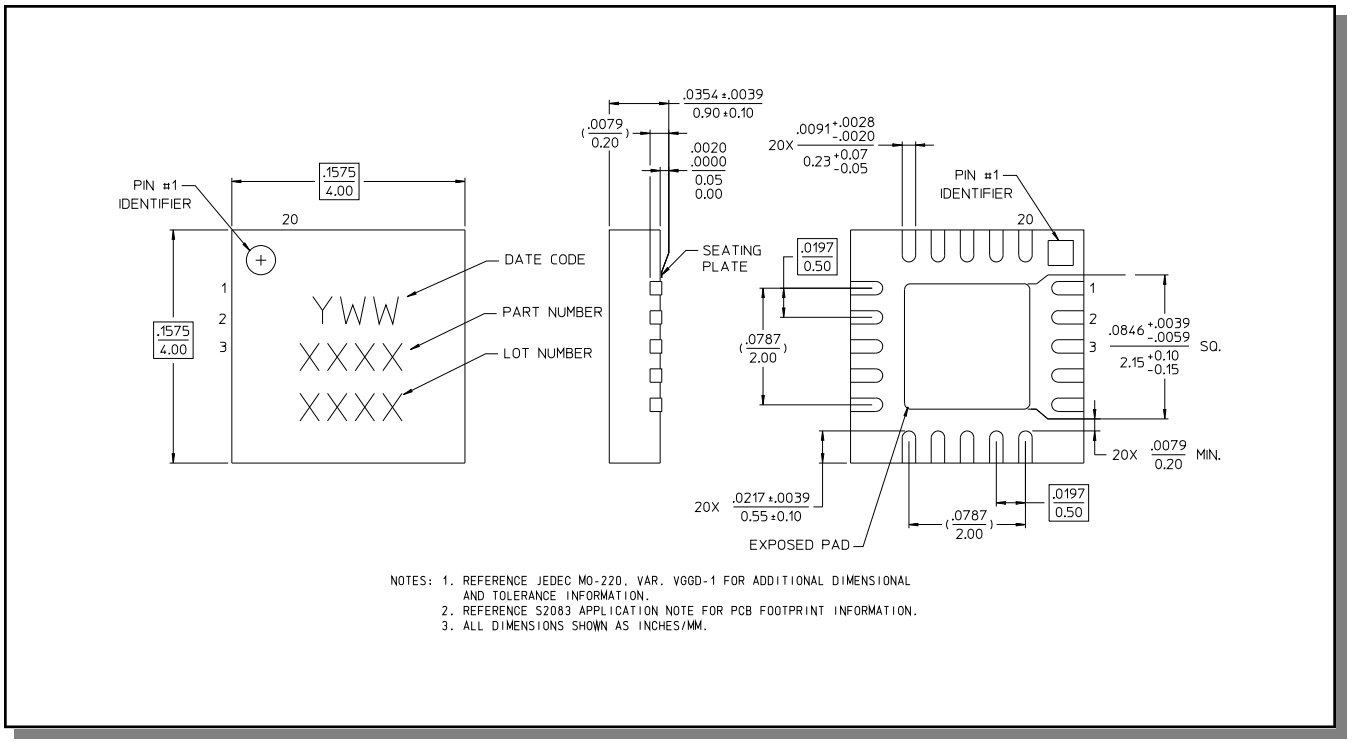
19. Note that the description of the above circuit is on the following page.
20. Only one section of MADR-009443-000100 is shown. The other three sections will have equivalent performance.

Description of Circuit

The MADR-009443-000100 provides four pairs of complementary outputs that are each capable of driving a maximum of ± 35 mA into a load. In addition, with proper capacitor selection (C3 & C4) used in parallel with the current setting resistor (R1 & R2), additional spiking current can be achieved.

To achieve the Non-Inverting and Inverting complementary voltages, each output is switched between two internal FETs. The FETs are connected to V_{OPT} for the positive output and V_{EE} for the negative output. V_{OPT} and V_{EE} are adjustable for various configurations and have the following limitations: V_{EE} can be no more negative than –10.5 volts; V_{OPT} can be no more positive than +7.0 volts AND V_{OPT} must always be less than or equal to V_{CC}. Increasing V_{OPT} beyond V_{CC} will prevent the device from switching states when commanded to by the logic input. The most common configuration is to drive V_{EE} at –5.0 volts with V_{CC} and V_{OPT} tied together at +5.0 volts.

Lead-Free, 4 x 4 mm, 20-lead PQFN†



NOTES: 1. REFERENCE JEDEC MO-220, VAR. VGGD-1 FOR ADDITIONAL DIMENSIONAL AND TOLERANCE INFORMATION.
2. REFERENCE S2083 APPLICATION NOTE FOR PCB FOOTPRINT INFORMATION.
3. ALL DIMENSIONS SHOWN AS INCHES/MM.

† Reference Application Note M538 for lead-free solder reflow recommendations.