MAPLST1617-030CF

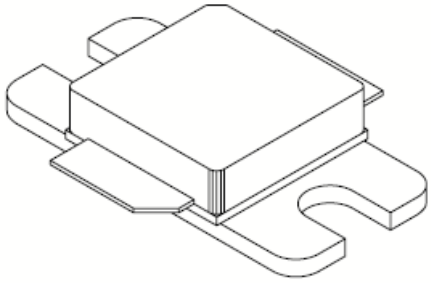
LDMOS RF Line Power FET Transistor
30 W , 1600-1700 MHz, 28V

Discontinued
(For Reference Only)

Designed for INMARSAT applications in the 1620-1670 MHz frequency band.

- Typical two tone performance (IMD=-30 dBc):
  Average output power: 15W
  Gain: 14dB (typ.)
  Efficiency: 38% (typ.)
- 10:1 VSWR ruggedness at 30W, 28V,1670MHz)

Product Image



MAPLST1617-030CF

MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Drain—Source Voltage	V_{DSS}	65	V_{dc}
Gate—Source Voltage	V_{GS}	20	V_{dc}
Total Power Dissipation @ T_C = 25 °C	P_D	97	W
Storage Temperature	T_{STG}	-40 to +150	°C
Junction Temperature	T_J	+200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.8	°C/W

NOTE—**CAUTION**—MOS devices are susceptible to damage from electrostatic charge. Precautions in handling and packaging MOS devices should be observed.

- **North America** Tel: 800.366.2266 / Fax: 978.366.2266
- **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

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Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS @ 25°C					
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 20 µAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0)	I_{DSS}	—	—	1	µAdc
Gate—Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0)	I_{GSS}	—	—	1	µAdc
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 1 mA)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 250 mA)	$V_{DS(Q)}$	2	—	4.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 A)	$V_{DS(on)}$	—	0.2	—	Vdc
Forward Transconductance (V_{GS} = 10 Vdc, I_D = 1 A)	Gm	—	1.2	—	S
DYNAMIC CHARACTERISTICS @ 25°C					
Input Capacitance (Including Input Matching Capacitor in Package) (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	90	—	pF
Output Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	32.5	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.5	—	pF
RF FUNCTIONAL TESTS @ 25°C (In M/A-COM Test Fixture)					
CW Gain (V_{DS} = 28 Vdc, P_{OUT} = 30 W (avg.), I_{DQ} = 250 mA, f0 = 1670 MHz)	G_{ps}	—	14	—	dB
CW Drain Efficiency (V_{DS} = 28 Vdc, P_{OUT} = 30 W (avg.), I_{DQ} = 250 mA, f0 = 1670 MHz)	EFF (η)	—	50	—	%
CW Input Return Loss (V_{DS} = 28 Vdc, P_{OUT} = 30 W (avg.), I_{DQ} = 250 mA, f0 = 1670 MHz)	IRL	—	-10	-9	dB
IMD (V_{DS} = 28 Vdc, P_{OUT} = 15 W (avg.) (30 W PEP), I_{DQ} = 250 mA, f0 = 1670 MHz, f1 = 1670.1 MHz)	IMD	—	-30	—	dBc
Output VSWR Tolerance (V_{DS} = 28 Vdc, P_{OUT} = 30 W (avg.), I_{DQ} = 250 mA, f0 = 1670 MHz)	Ψ	No Degradation In Output Power Before and After Test			

(1) Device specifications obtained on a Production Test Fixture.

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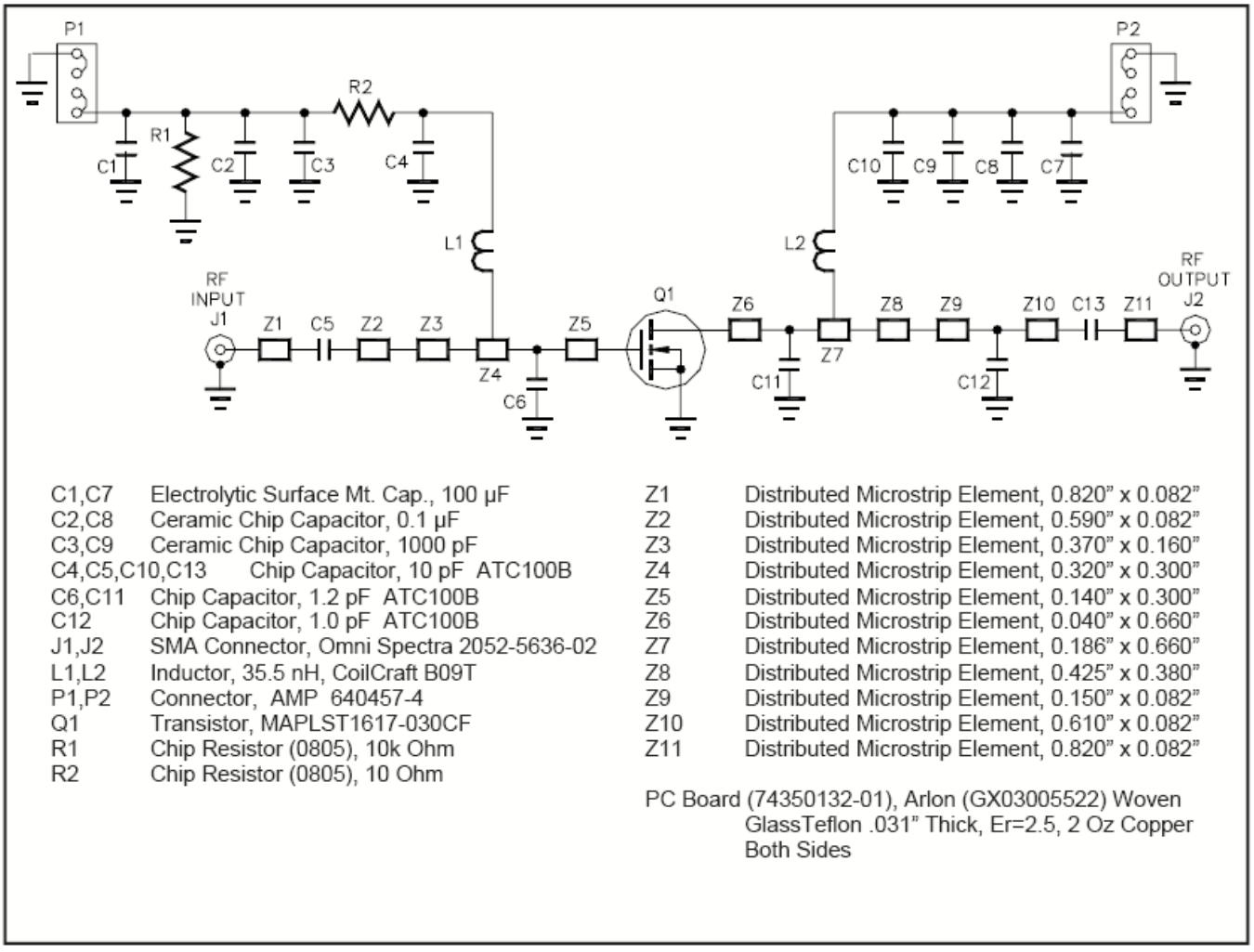


C1,C7	Electrolytic Surface Mt. Cap., 100 µF	Z1	Distributed Microstrip Element, 0.820" x 0.082"
C2,C8	Ceramic Chip Capacitor, 0.1 µF	Z2	Distributed Microstrip Element, 0.590" x 0.082"
C3,C9	Ceramic Chip Capacitor, 1000 pF	Z3	Distributed Microstrip Element, 0.370" x 0.160"
C4,C5,C10,C13	Chip Capacitor, 10 pF ATC100B	Z4	Distributed Microstrip Element, 0.320" x 0.300"
C6,C11	Chip Capacitor, 1.2 pF ATC100B	Z5	Distributed Microstrip Element, 0.140" x 0.300"
C12	Chip Capacitor, 1.0 pF ATC100B	Z6	Distributed Microstrip Element, 0.040" x 0.660"
J1,J2	SMA Connector, Omni Spectra 2052-5636-02	Z7	Distributed Microstrip Element, 0.186" x 0.660"
L1,L2	Inductor, 35.5 nH, CoilCraft B09T	Z8	Distributed Microstrip Element, 0.425" x 0.380"
P1,P2	Connector, AMP 640457-4	Z9	Distributed Microstrip Element, 0.150" x 0.082"
Q1	Transistor, MAPLST1617-030CF	Z10	Distributed Microstrip Element, 0.610" x 0.082"
R1	Chip Resistor (0805), 10k Ohm	Z11	Distributed Microstrip Element, 0.820" x 0.082"
R2	Chip Resistor (0805), 10 Ohm		

PC Board (74350132-01), Arlon (GX03005522) Woven GlassTeflon .031" Thick, Er=2.5, 2 Oz Copper Both Sides

FIGURE 1. 1620—1670 MHZ TEST FIXTURE SCHEMATIC

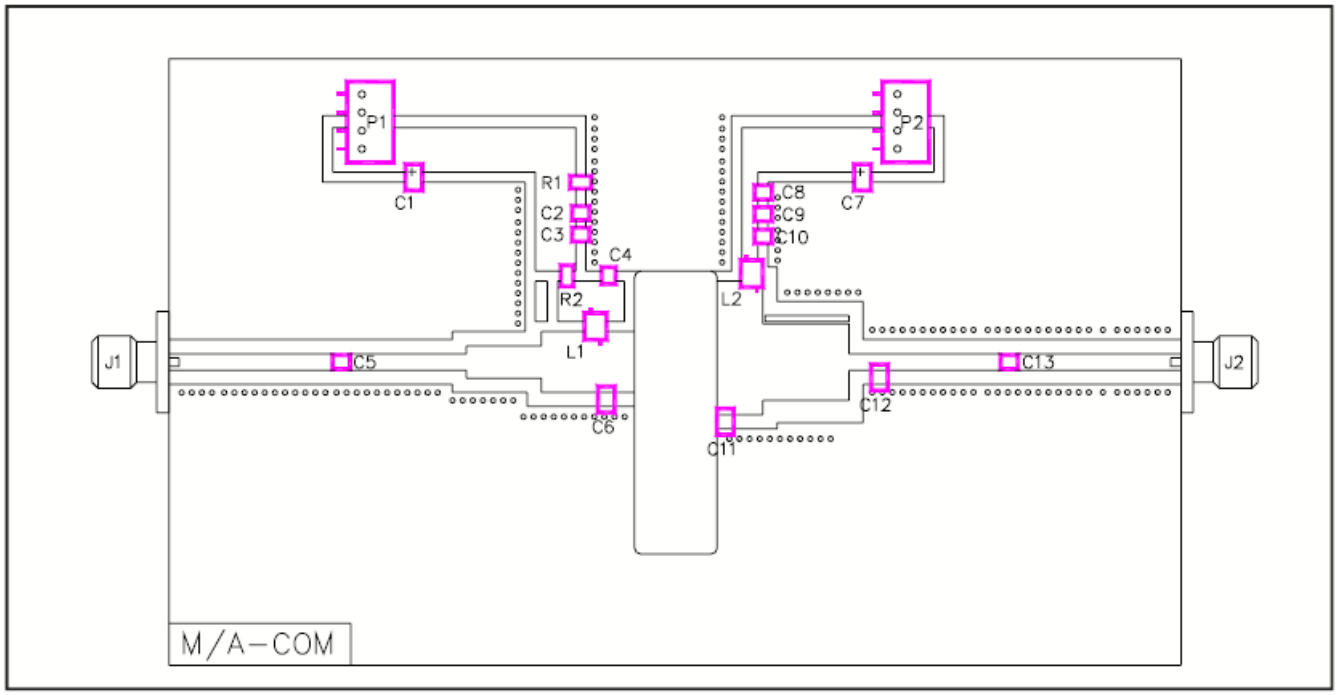
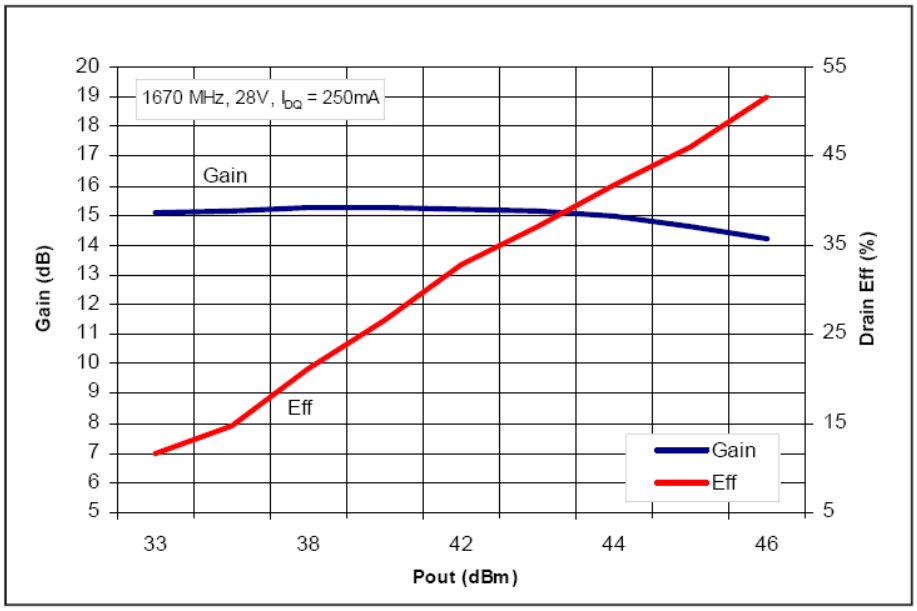
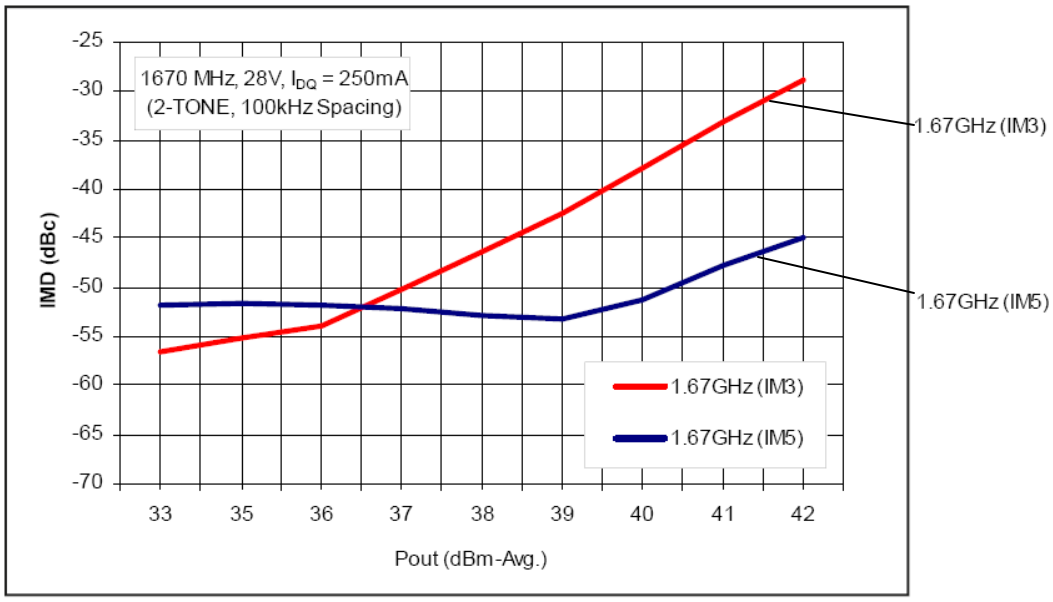


FIGURE 2. 1620—1670 MHZ TEST FIXTURE COMPONENT LAYOUT

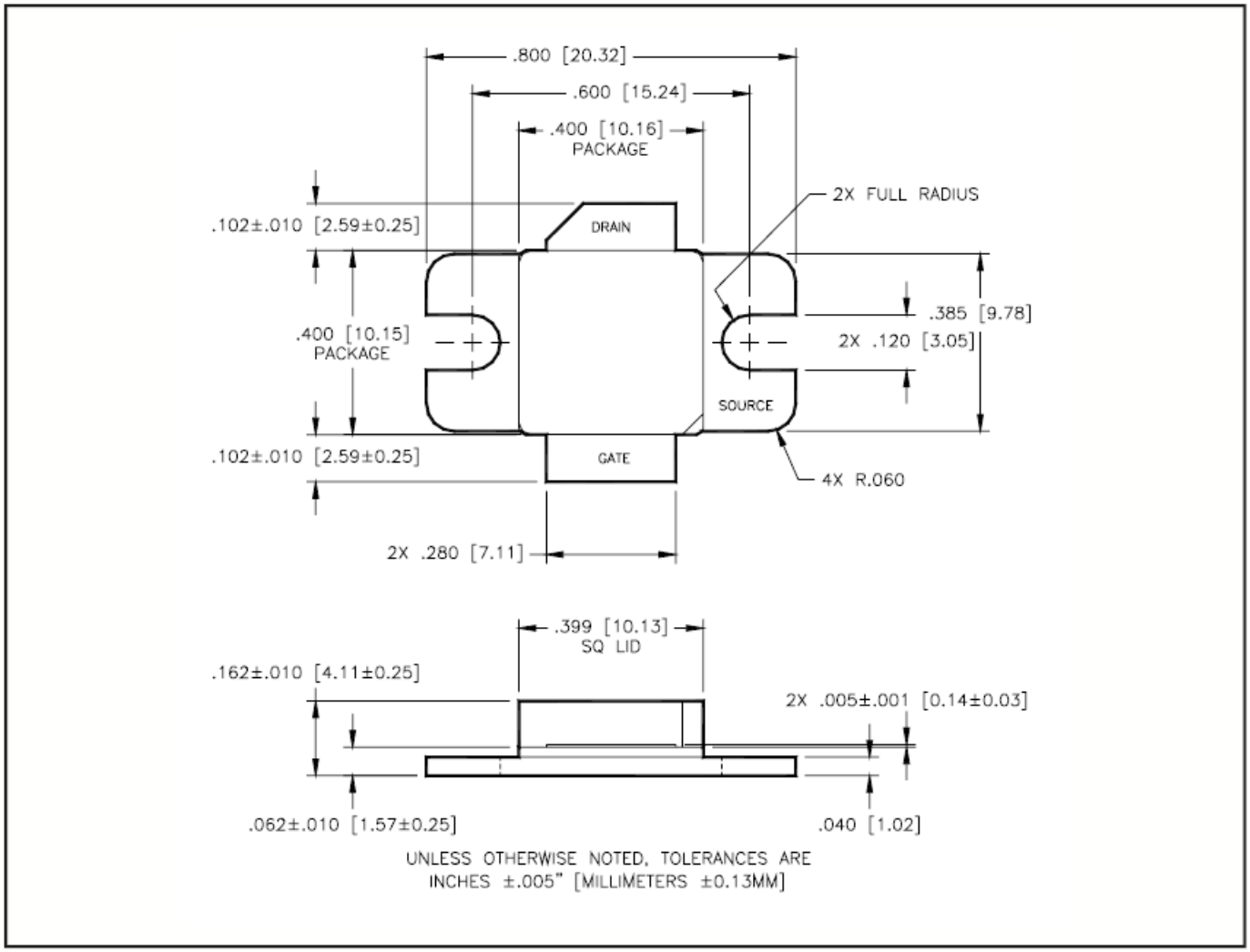


GRAPH 1. CW: GAIN AND EFFICIENCY VS. OUTPUT POWER



GRAPH 2. TWO TONE: INTERMODULATION DISTORTION VS. OUTPUT POWER

PACKAGE DIMENSIONS



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