

XB1008-QT

Buffer Amplifier 10.0-21.0 GHz

Rev. V1
MimiX Broadband

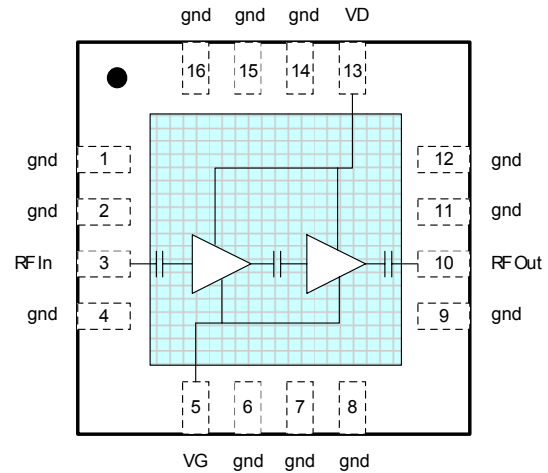
Features

- Excellent Transmit LO/Output Buffer Stage
- 3x3mm, QFN
- 17.0 dB Small Signal Gain
- +20.0 dBm Psat
- +32 dBm Output IP3
- 4.5 dB Noise Figure
- Variable Gain with Adjustable Bias
- 100% RF, DC and Output Power Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's two stage 10.0-21.0 GHz GaAs MMIC buffer amplifier has a small signal gain of 17.0 dB with a +18.0 dBm P1dB output compression point. The device also provides variable gain regulation with adjustable bias. The device is ideally suited as an LO or RF buffer stage with broadband performance at a very low cost. The device comes in an RoHS compliant 3x3mm QFN surface mount package offering excellent RF and thermal properties. This device is well suited for Microwave and Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Functional Block Diagram



Pin Configuration

Pin No.	Function	Pin No.	Function
1-2	Ground	10	RF Output
3	RF Input	11-12	Ground
4	Ground	13	Drain Bias
5	Gate Bias	14-16	Ground
6-9	Ground		

Ordering Information

Part Number	Package
XB1008-QT-0G00	bulk quantity
XB1008-QT-0G0T	tape and reel
XB1008-QT-EV1	evaluation module

Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3 VDC
Supply Current (Id1)	180 mA
Gate Bias Voltage (Vg)	0 V
Input Power (Pin)	+20.0 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to +85 °C
Channel Temperature (Tch)	150 °C
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL1

Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

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Electrical Specifications: 10-21 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)	dB	-	12.0	-
Output Return Loss (S22)	dB	-	12.0	-
Small Signal Gain (S21)	dB	-	17.0	-
Gain Flatness (ΔS_{21})	dB	-	+/-2.0	
Reverse isolation (S12)	dB	-	65.0	-
Noise Figure	dB	-	4.5	
Output Power for 1dB Compression Point (P1dB)	dBm	-	+18.0	-
Saturated Output Power (Psat)	dBm	-	+20.0	-
Output Third Order Intercept	dBm	-	+32.0	-
Drain Bias Voltage (Vd)	VDC	-	+4.0	+4.0
Gate Bias Voltage (Vg)	VDC	-1.0	-0.23	-0.1
Supply Current (Id) (Vd=4.0 V, Vg2=-0.5 V Typical)	mA	-	100	130

ADVANCED: Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.

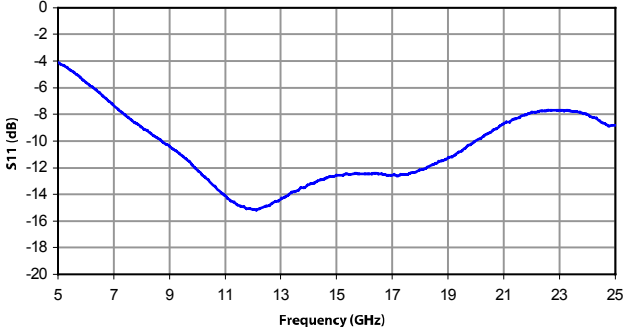
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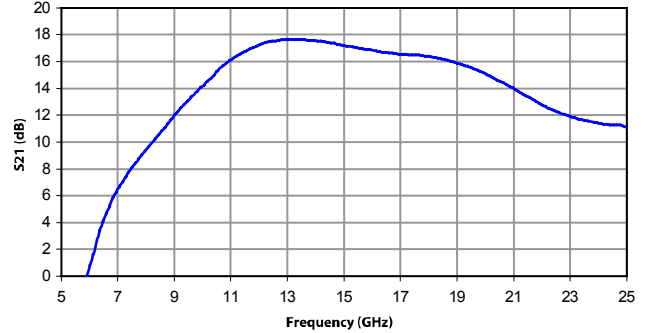
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Typical Performance Curves

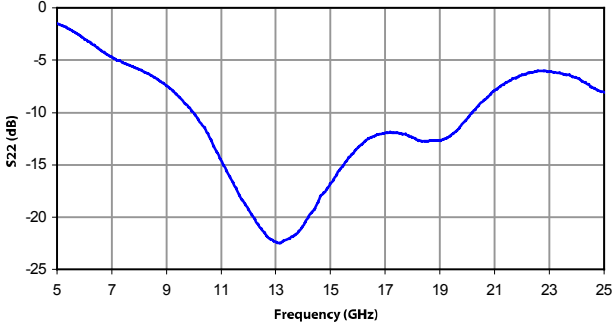
XB1008-QT, Vd = 4V, Id = 100 mA: Input Return Loss vs Frequency



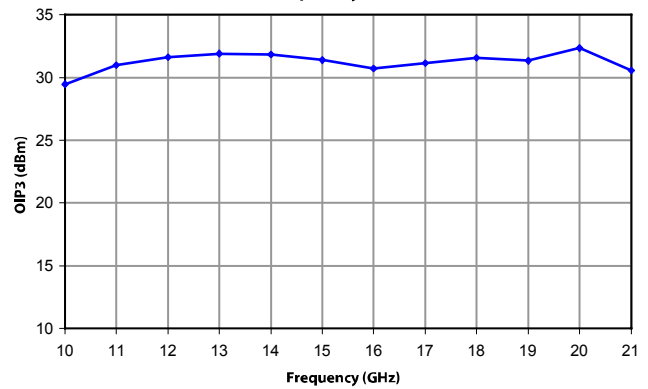
XB1008-QT, Vd = 4V, Id = 100 mA: Small Signal Gain vs Frequency



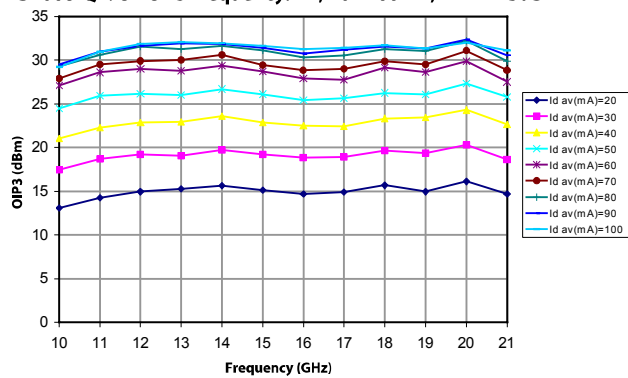
XB1008-QT, Vd = 4V, Id = 100 mA: Output Return Loss vs Frequency



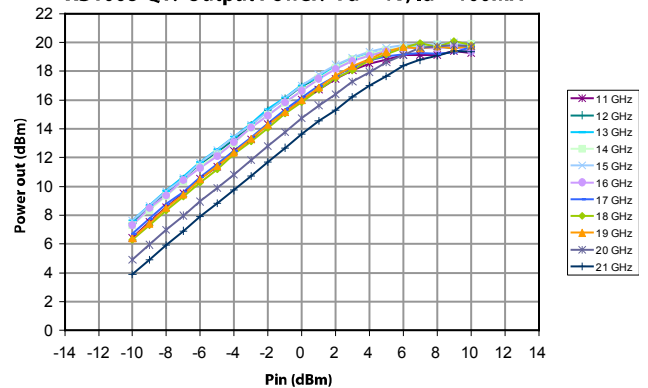
XB1008-QT: OIP3 vs Frequency. 4V, 90 mA, Pin = -15dBm



XB1008-QT: OIP3 vs Frequency. 4V, 20 - 100mA, Pin = -15dBm

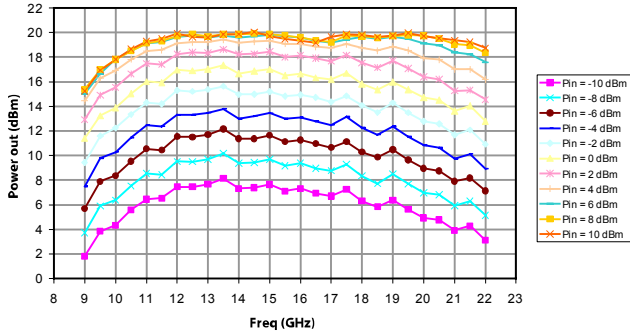


XB1008-QT: Output Power. Vd = 4V, Id = 100mA



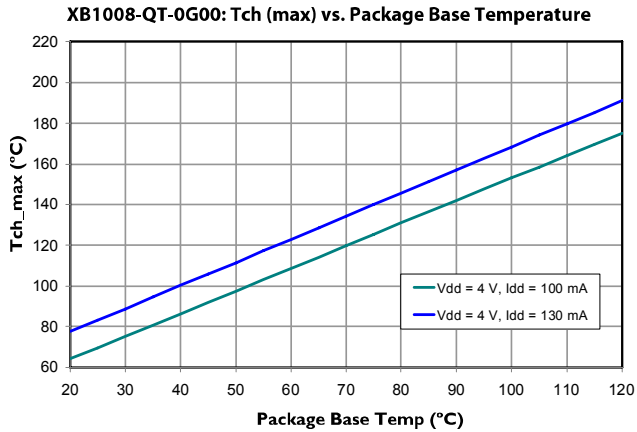
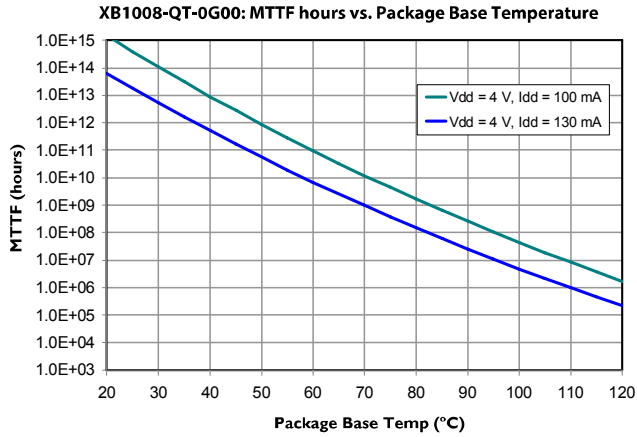
Typical Performance Curves (cont.)

XB1008-QT: Power out vs Frequency. $V_d = 4V$ and $I_d = 100mA$



MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.



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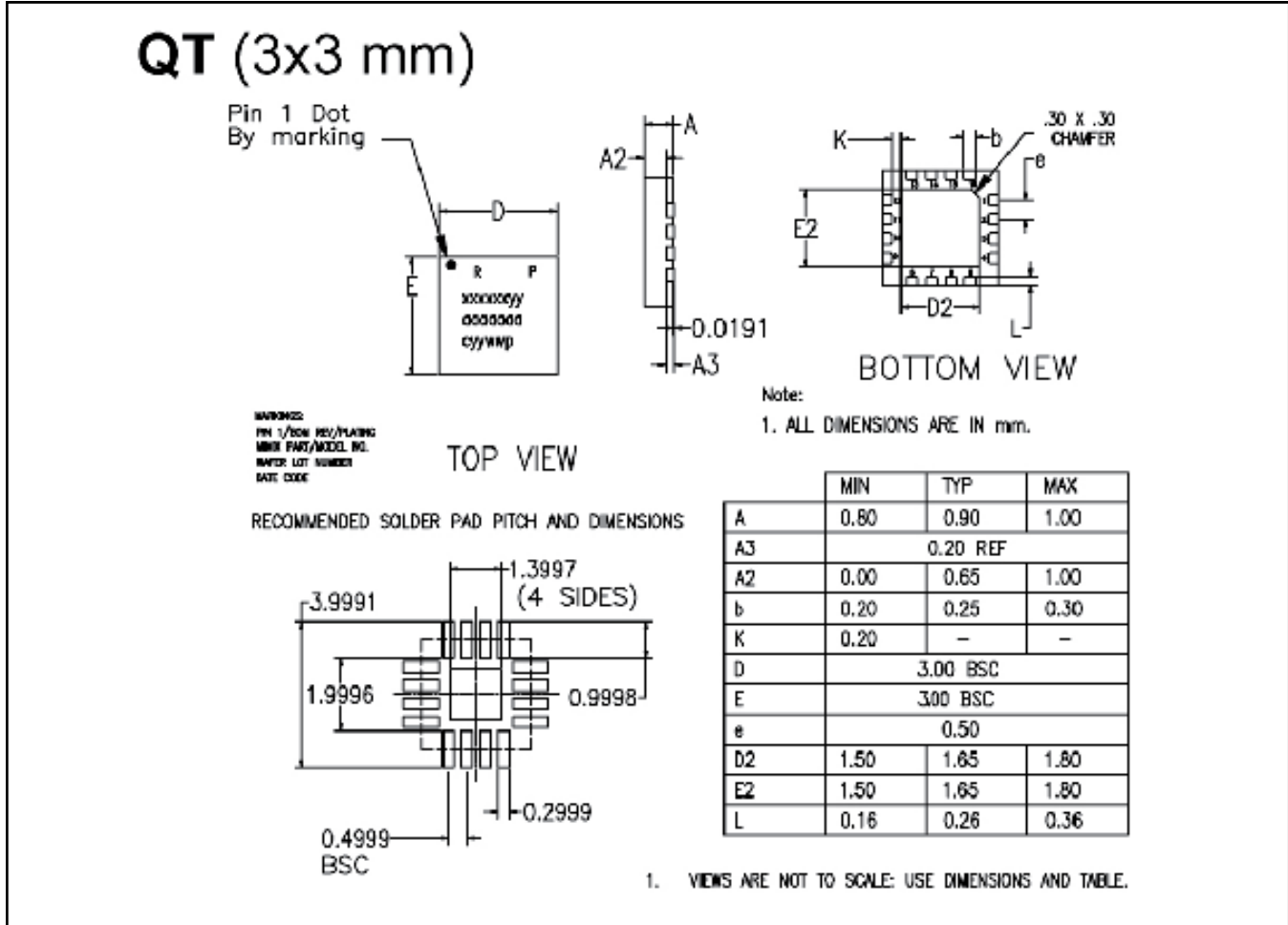


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App Note [1] Biasing - The device provides variable gain with adjustable bias regulation. For optimum linearity performance, it is recommended to bias this device at $V_d=4V$ with $I_d=90\text{ mA}$. It is also recommended to use active biasing to control the drain currents because this gives the most reproducible results over temperature or RF level variations. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is $-0.5V$. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

Lead-Free Package Dimensions/Layout



Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.