XD1001-BD

Distributed Amplifier
18-50 GHz

Rev. V1
Mimix Broadband

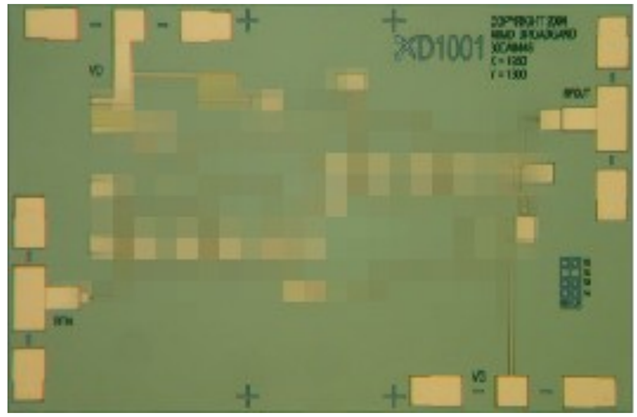
Features

- Ultra Wide Band Driver Amplifier
- Fiber Optic Modulator Driver
- 17.0 dB Small Signal Gain
- 5.0 dB Noise Figure
- 30 dB Gain Control
- +15.0 dBm P1dB Compression Point
- 100% On-Wafer RF, DC and Output Power Testing
- 100% Visual Inspection to MIL-STD-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's 18.0-50.0 GHz GaAs MMIC distributed amplifier has a small signal gain of 17.0 dB with a noise figure of 5.0 dB across the band. The device also includes 30.0 dB gain control and a +15 dBm P1dB compression point. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for microwave, millimeter-wave and wideband military applications.

Chip Device Layout



Absolute Maximum Ratings

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	220 mA
Gate Bias Voltage (Vg)	+0.3 V
Input Power (Pin)	+15 dBm
Storage Temperature (Tstg)	-65 ºC to +165 ºC
Operating Temperature (Ta)	-55 ºC to +85 ºC
Channel Temperature (Tch)[1]	+175 ºC

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

Ordering Information

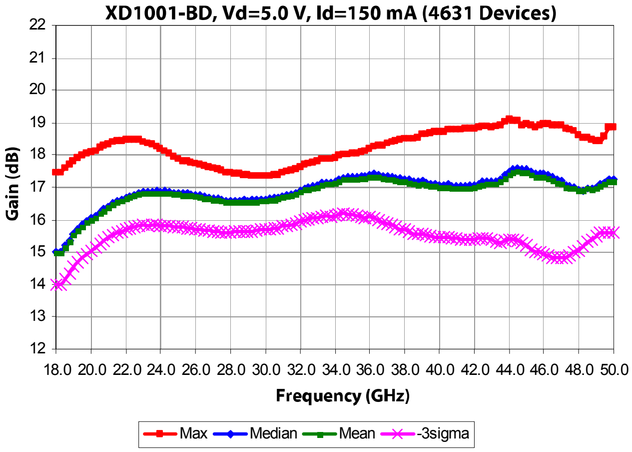
Part Number	Package
XD1001-BD-000V	"V" - vacuum release gel paks
XD1001-BD-EV1	evaluation module

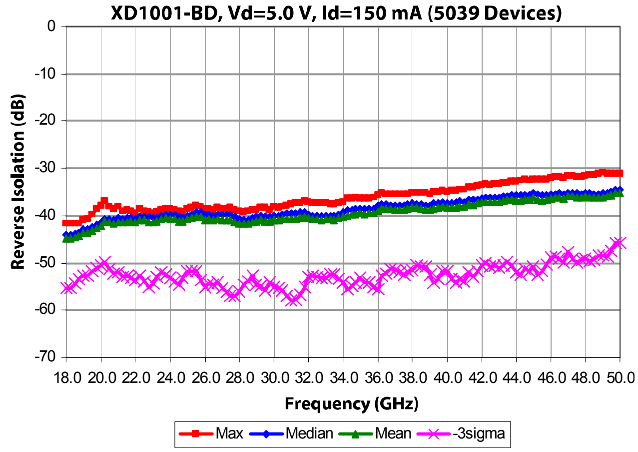
Electrical Specifications: 18-50 GHz (Ambient Temperature T = 25°C)

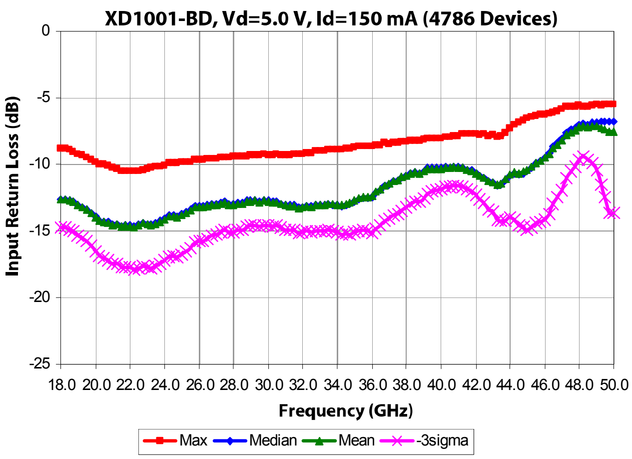
Parameter	Units	Min.	Typ.	Max.
Input Return Loss (S11)[2]	dB	5.0	10.0	-
Output Return Loss (S22)[2]	dB	6.0	11.0	-
Small Signal Gain (S21)[2]	dB	13.0	17.0	-
Gain Flatness (ΔS21)	dB	-	+/-1.0	-
Gain Control	dB	-	30.0	-
Reverse Isolation (S12)[2]	dB	30.0	40.0	-
Noise Figure (NF)	dB	-	5.0	-
Output Power for 1dB Compression Point (P1dB)[1]	dBm	-	+15.0	-
Output Third Order Intercept Point (OIP3)[1]	dBm	-	+24.0	-
Drain Bias Voltage (Vd)	VDC	-	+5.0	+5.5
Gain Control Bias (Vg)	VDC	-2.0	0.0	+0.1
Supply Current (Id) (Vd=5.0 V, Vg=-0.0 V Typical)	mA	-	160	190

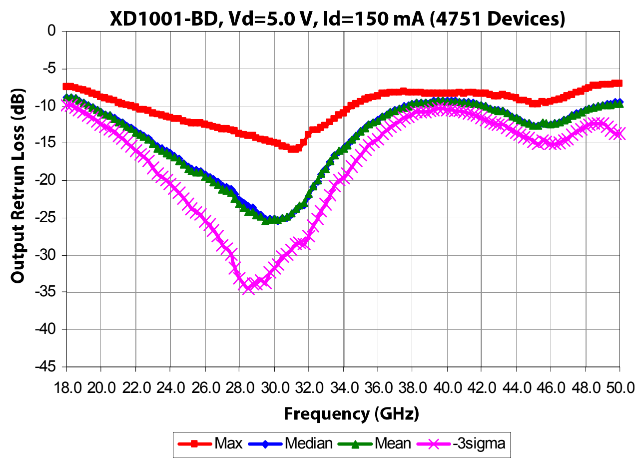
1. Measured using constant current.
2. Unless otherwise indicated Min/Max over 18.0-50.0 GHz and biased at Vd=5 V, Id=160 mA

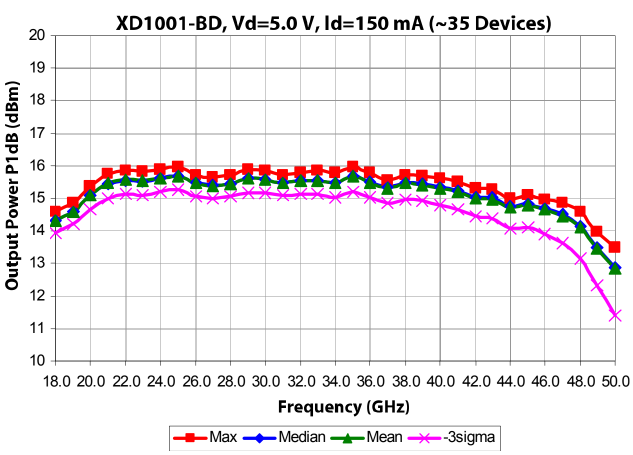
Typical Performance Curves (On-Wafer[1])

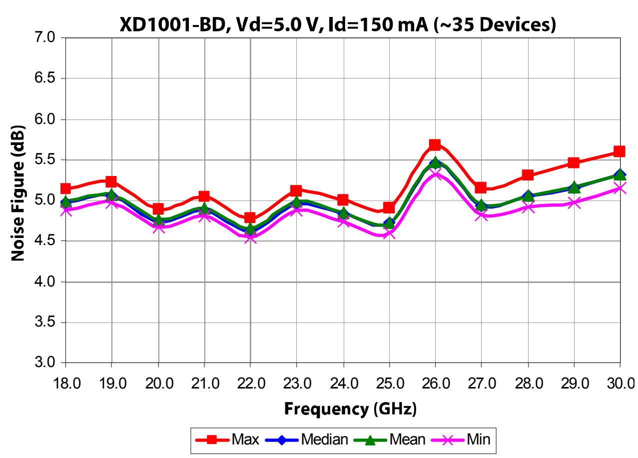






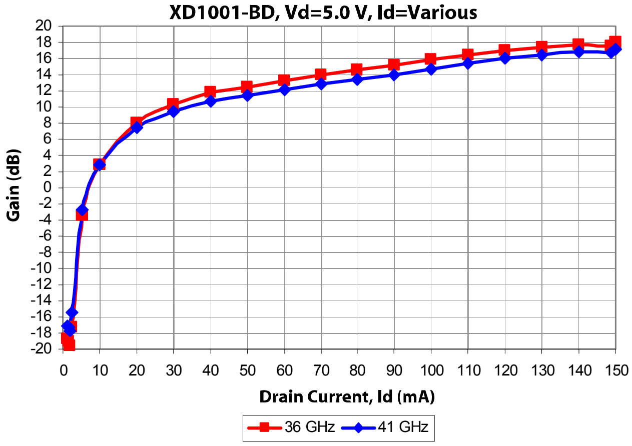


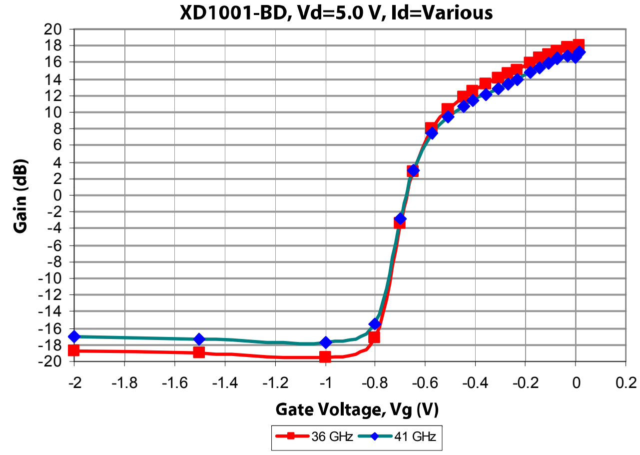


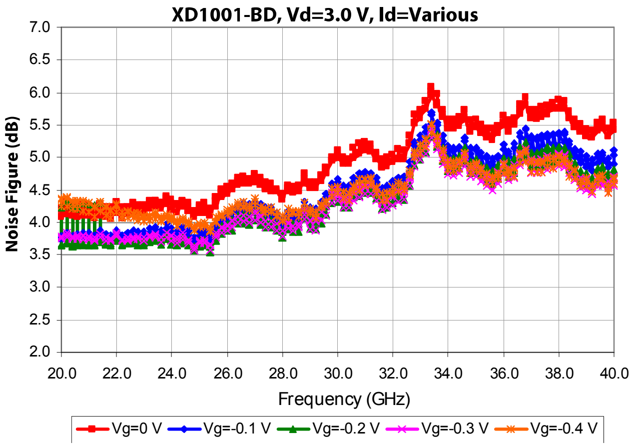


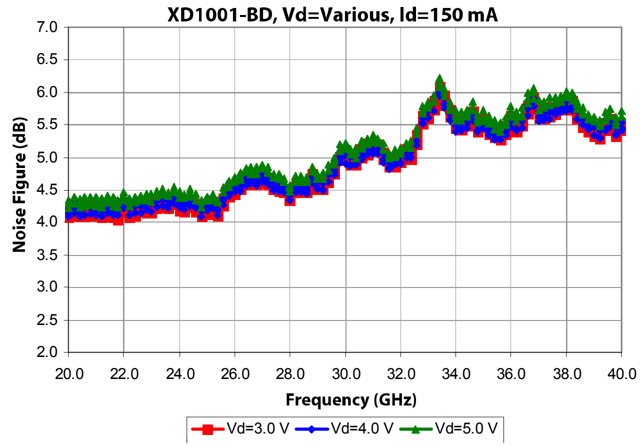
Note [1] Measurements – On-Wafer data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM Tech T-pad transition is recommended. For additional information see the M/A-COM Tech "T-Pad Transition" application note.

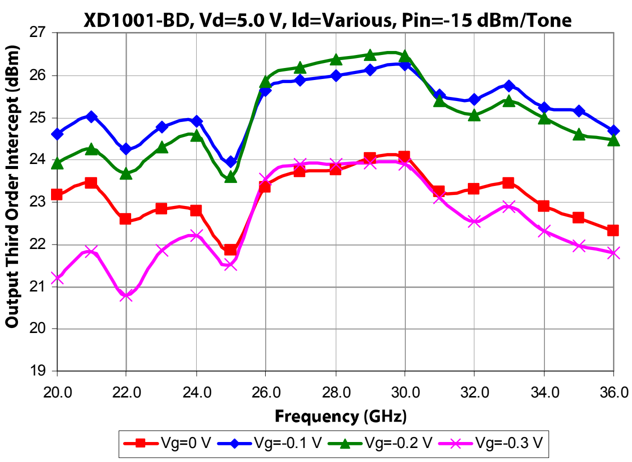
Typical Performance Curves (On-Wafer[1]) (cont.)











Note [1] Measurements – On-Wafer data has been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge. For optimum performance M/A-COM Tech T-pad transition is recommended. For additional information see the M/A-COM Tech "T-Pad Transition" application note.

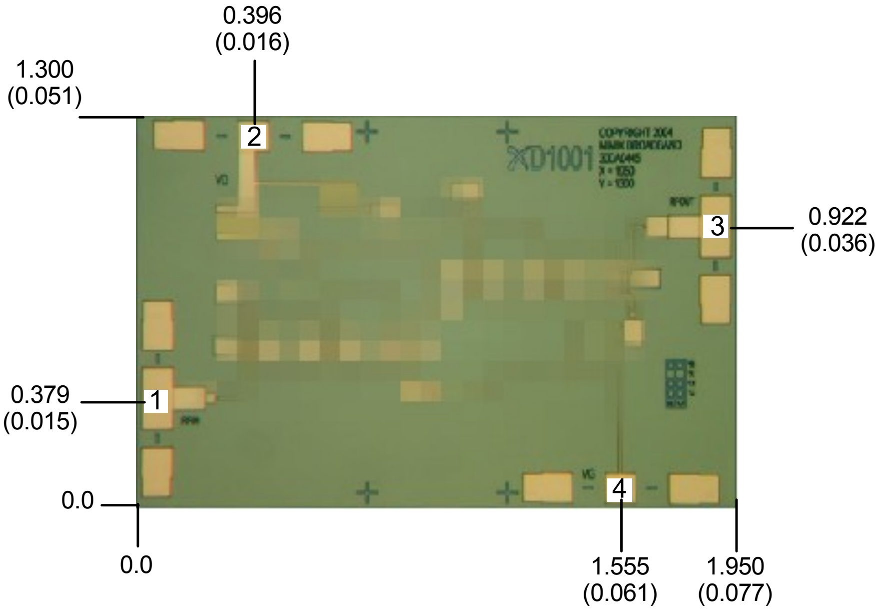
S-Parameters (On-Wafer[1])

Typcial S-Parameter Data for XD1001-BD
Vd=5.0 V, Id=149 mA

Frequency (GHz)	S11 (Mag)	S11 (Ang)	S21 (Mag)	S21 (Ang)	S12 (Mag)	S12 (Ang)	S22 (Mag)	S22 (Ang)
14.0	0.339	-105.95	4.484	-64.44	0.0024	151.71	0.566	42.43
15.0	0.318	-109.42	4.959	-81.25	0.0029	146.08	0.536	29.71
16.0	0.296	-113.59	5.454	-98.28	0.0036	142.13	0.504	16.92
17.0	0.277	-118.09	5.957	-115.37	0.0043	129.03	0.469	3.70
18.0	0.263	-122.98	6.452	-132.70	0.0050	119.05	0.427	-9.98
19.0	0.248	-128.13	6.886	-150.61	0.0056	106.79	0.379	-24.20
20.0	0.227	-130.91	7.221	-168.63	0.0065	94.16	0.325	-38.39
21.0	0.219	-133.08	7.502	173.62	0.0068	78.94	0.271	-53.12
22.0	0.218	-136.80	7.627	155.96	0.0073	65.41	0.218	-66.82
23.0	0.222	-139.91	7.672	138.78	0.0077	50.14	0.170	-79.26
24.0	0.225	-143.34	7.656	122.19	0.0075	37.52	0.129	-89.38
25.0	0.233	-150.18	7.596	106.11	0.0079	18.78	0.096	-98.45
26.0	0.242	-157.65	7.519	90.71	0.0074	5.49	0.070	-103.92
27.0	0.250	-164.41	7.465	75.62	0.0078	-6.83	0.059	-103.19
28.0	0.249	-172.29	7.404	60.84	0.0078	-24.58	0.055	-99.36
29.0	0.248	-178.25	7.394	46.58	0.0077	-41.51	0.060	-99.54
30.0	0.249	177.08	7.445	32.02	0.0071	-55.57	0.083	-106.68
31.0	0.252	171.40	7.507	17.23	0.0073	-69.66	0.108	-120.07
32.0	0.252	168.86	7.606	2.06	0.0075	-85.07	0.141	-130.95
33.0	0.251	169.12	7.695	-13.87	0.0079	-104.67	0.178	-143.90
34.0	0.268	165.08	7.704	-29.86	0.0075	-121.74	0.211	-159.27
35.0	0.291	161.35	7.655	-45.93	0.0079	-135.09	0.243	-172.40
36.0	0.307	159.48	7.542	-62.26	0.0079	-152.32	0.275	174.70
37.0	0.331	156.28	7.423	-78.77	0.0088	-165.75	0.305	163.36
38.0	0.370	150.02	7.168	-94.50	0.0083	172.51	0.334	151.74
39.0	0.384	144.92	6.983	-109.65	0.0090	160.60	0.351	139.42
40.0	0.380	139.70	6.920	-125.06	0.0080	145.41	0.352	129.53
41.0	0.390	136.35	6.827	-140.84	0.0087	134.33	0.352	121.51
42.0	0.399	132.68	6.827	-156.36	0.0090	119.70	0.345	112.70
43.0	0.407	128.89	6.929	-172.64	0.0091	106.25	0.331	106.19
44.0	0.417	126.10	7.019	169.64	0.0093	91.50	0.325	100.85
45.0	0.407	124.13	6.992	150.34	0.0094	78.26	0.313	94.96
46.0	0.402	124.74	6.884	131.08	0.0097	58.70	0.302	93.66
47.0	0.436	122.89	6.794	112.53	0.0099	33.85	0.306	88.79
48.0	0.438	121.54	6.696	92.46	0.0095	21.18	0.285	82.69
49.0	0.426	118.51	6.662	70.96	0.0098	-2.17	0.278	78.04
50.0	0.412	114.78	7.002	45.72	0.0101	-25.75	0.258	68.40

Note [1] S-Parameters – On-Wafer S-Parameters have been taken using bias conditions as shown. Measurements are referenced 150 um in from RF In/Out pad edge.

Mechanical Drawing

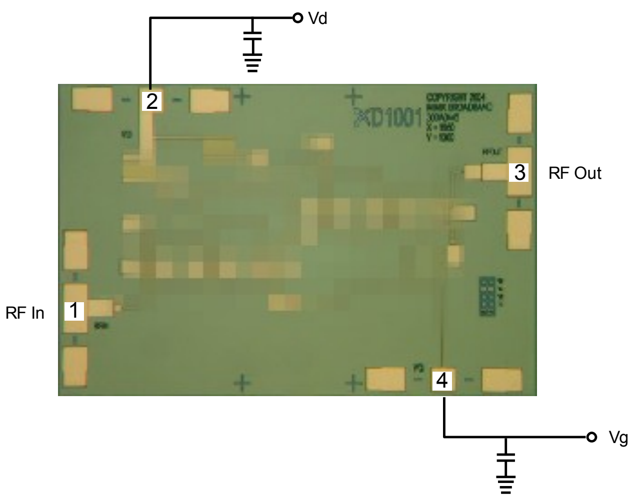


(Note: Engineering designator is 30DA0445)

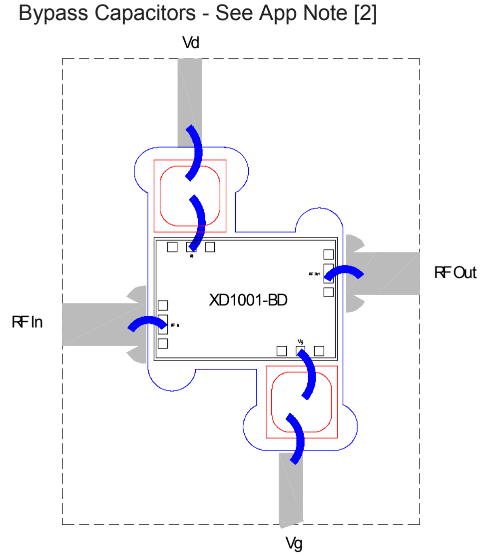
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 1.572 mg.

Bond Pad #1 (RF In)	Bond Pad #3 (RF Out)
Bond Pad #2 (Vd)	Bond Pad #4 (Vg)

Bias Arrangement

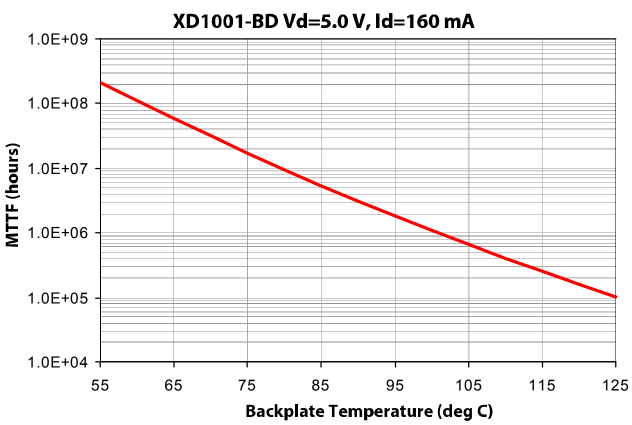


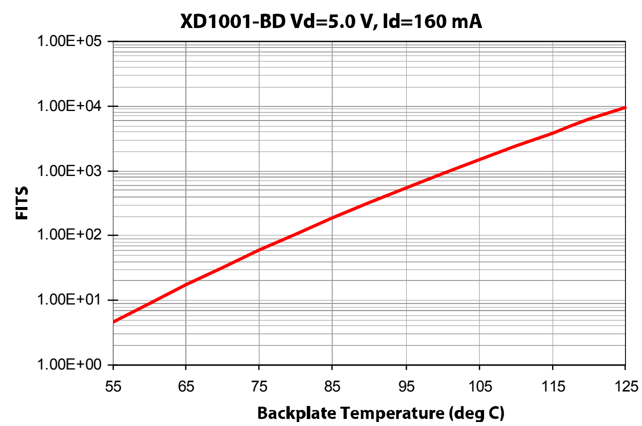
Bypass Capacitors - See App Note [2]

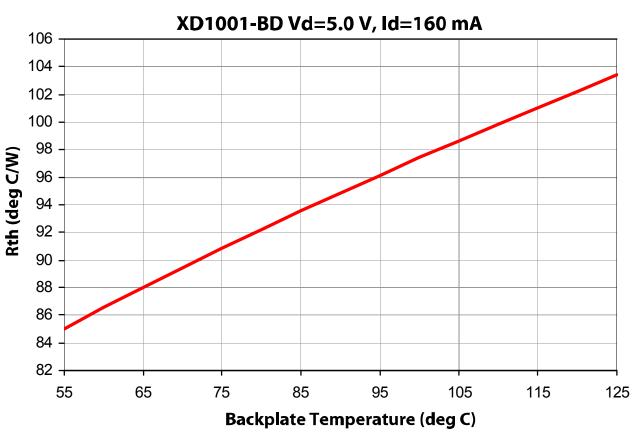


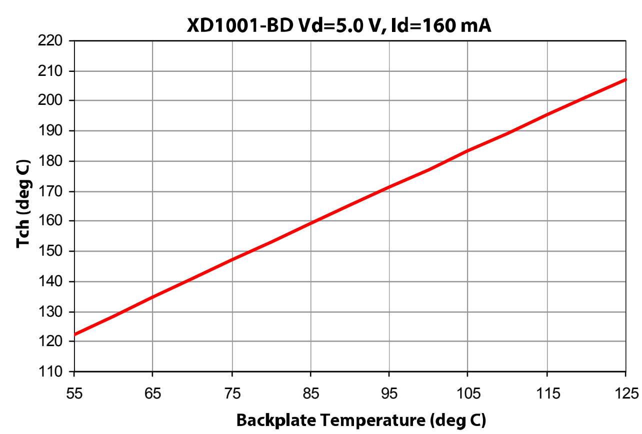
MTTF

These numbers were calculated based upon accelerated life test information received from the fabricating foundry and extensive thermal modeling/finite element analysis done at M/A-COM Tech. The values shown here are only to be used as a guideline against the end application requirements and only represent reliability information under one bias condition. Ultimately bias conditions and resulting power dissipation along with the practical aspects, i.e. thermal material stack-up, attach method of die placement are the key parts in determining overall reliability for a specific application, see previous pages. If the data shown below does not meet your reliability requirements or if the bias conditions are not within your operating limits please contact technical sales for additional information.









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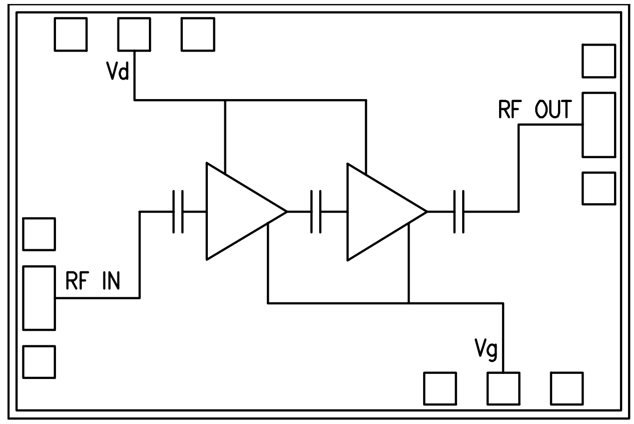
- **India** Tel: +91.80.43537383
- **China** Tel: +86.21.2407.1588

Visit www.macomtech.com for additional data sheets and product information.



App Note [1] Biasing - As shown in the bonding diagram, this device is operated with a single drain and a gain control voltage. Maximum gain bias is nominally Vd=5.0V, Vg=0V, Id=160mA. Gain can be adjusted by changing Vg. It is recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is 0.0V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement - Each DC pad (Vd and Vg) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.