XX1001-BD

Doubler and Power Amplifier 18.0-21.0/36.0-42.0 GHz

Rev. V1

Mimix Broadband

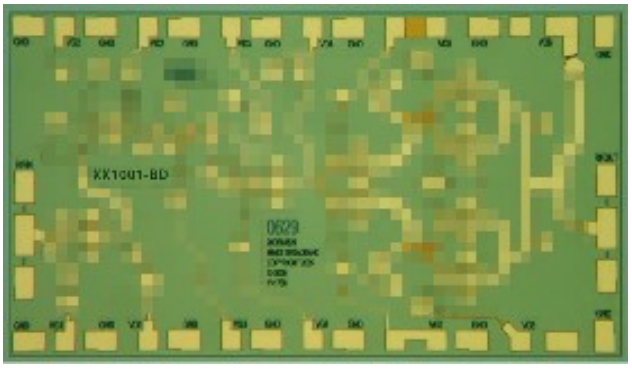
Features

- Integrated Doubler and Power Amplifier
- Excellent Saturated Output Stage
- +26.0 dBm Output Power
- 50.0 dBc Fundamental Suppression
- 100% On-Wafer RF, DC & Output Power Testing
- 100% Commercial-Level Visual Inspection Using Mil-Std-883 Method 2010
- RoHS* Compliant and 260°C Reflow Compatible

Description

M/A-COM Tech's 18.0-21.0/36.0-42.0 GHz GaAs MMIC doubler integrates a doubler and 4-stage power amplifier. The device provides better than +26.0 dBm output power and has excellent fundamental rejection. This MMIC uses M/A-COM Tech's GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Chip Device Layout



Absolute Maximum Ratings[1]

Parameter	Absolute Max.
Supply Voltage (Vd)	+6.0 VDC
Supply Current (Id)	800 mA
Gate Bias Voltage (Vg)	+0.3 VDC
Input Power (RF Pin)	TBD
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Ta)	-55 °C to MTTF Table[1]
Channel Temperature (Tch)	MTTF Table[1]

(1) Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

Ordering Information

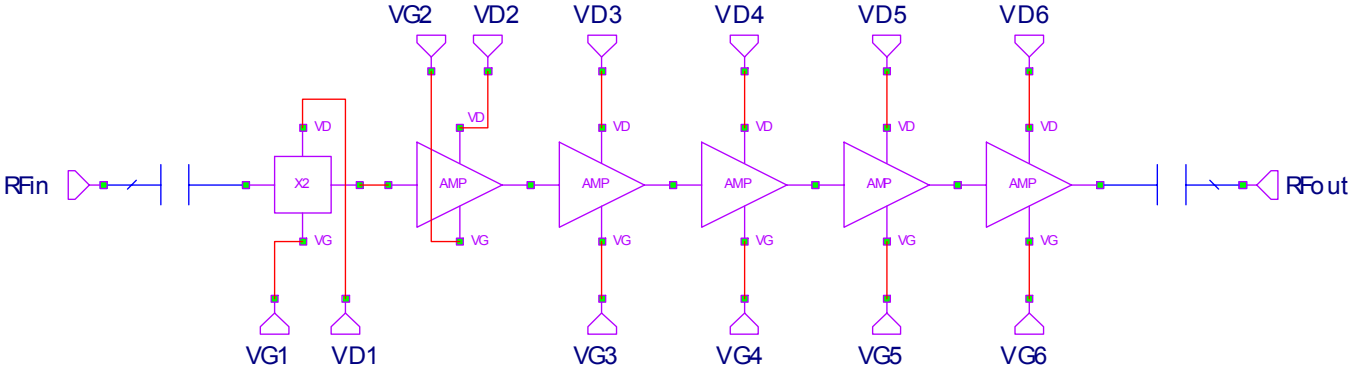
Part Number	Package
XX1001-BD-000V	vacuum release gel paks
XX1001-BD-EV1	evaluation board

• **North America** Tel: 800.366.2266 • **Europe** Tel: +353.21.244.6400
• **India** Tel: +91.80.43537383 • **China** Tel: +86.21.2407.1588
Visit www.macomtech.com for additional data sheets and product information.

Electrical Specifications: 18-21 GHz (fin) (Ambient Temperature T = 25°C)

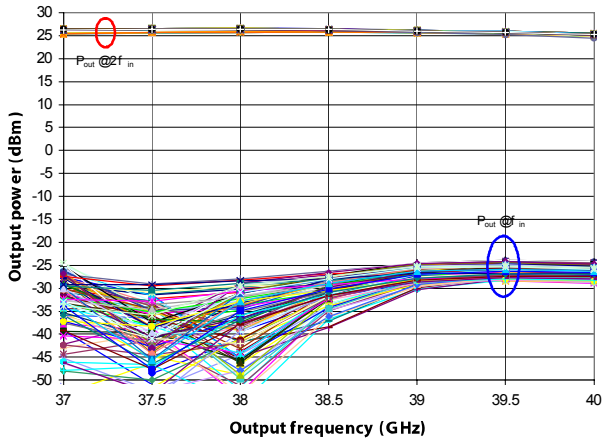
Parameter	Units	Min.	Typ.	Max.
Output Frequency Range (fout)	GHz	36.0	-	42.0
Input Return Loss (S11)	dB	-	TBD	-
Output Return Loss (S22)	dB	-	12.0	-
Fundamental Rejection	dBc	-	50.0	-
RF Input Power (RF Pin)	dBm	-	0.0	-
Output Power at 0.0 dBm Pin (Pout)	dBm	-	+26.0	-
Drain Supply Voltage (Vd1) Doubler	V	-	2.5	3.0
Drain Supply Voltage (Vd2) Buffer Amplifier	V	-	3.0	4.0
Drain Supply Voltage (Vd3,4,5,6) Power Amplifier	V	-	4.5	5.5
Gate Supply Voltage (Vg1) Doubler	V	-	-1.2	-
Drain Supply Current (Id1) Doubler	mA	-	<1.0	-
Drain Supply Current (Id2) Buffer Amplifier	mA	-	20	25
Drain Supply Current (Id3,4,5,6) (Vg=-0.7V Typical) Power Amplifier	mA	-	530	600

Block Diagram & Schematics

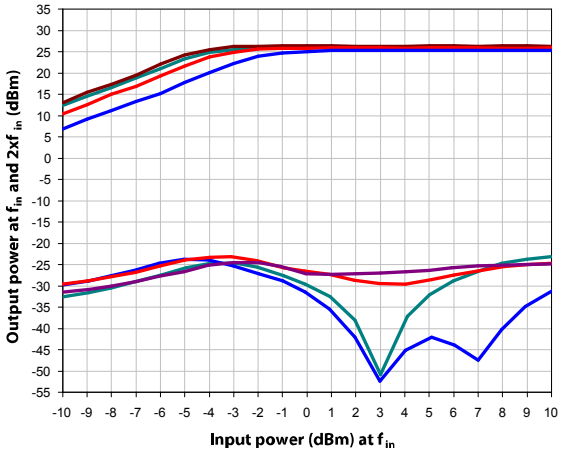


Typical Performance Curves

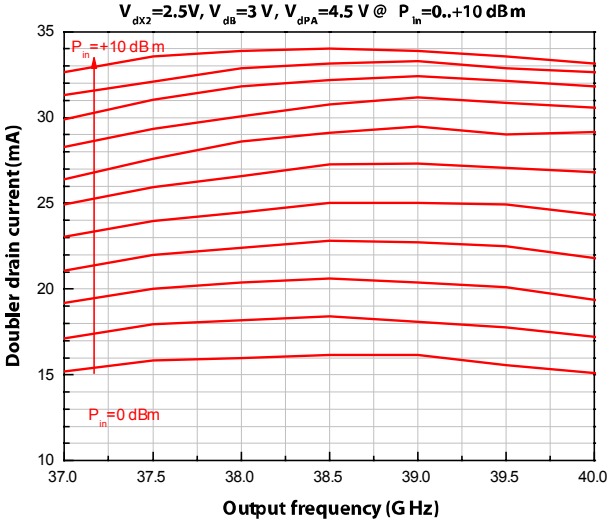
VdX2=2.5 V, VdB=3 V, Vd PA=4.5 V, P in= +2..+9 dBm



V_{dx2}=2.5 V, V_{dbuff}=3 V I_{db}=30 mA, V_{dPA}=4.5 V I_{dPA}=520 mA



V_{dX2}=2.5V, V_{dB}=3 V, V_{dPA}=4.5 V @ P_{In}=0..+10 dBm



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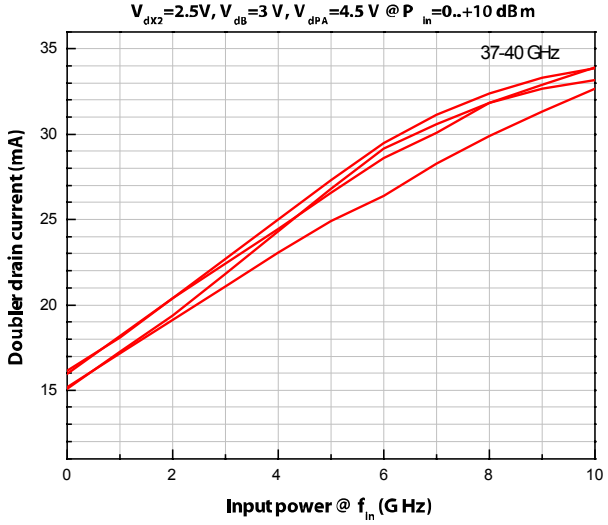

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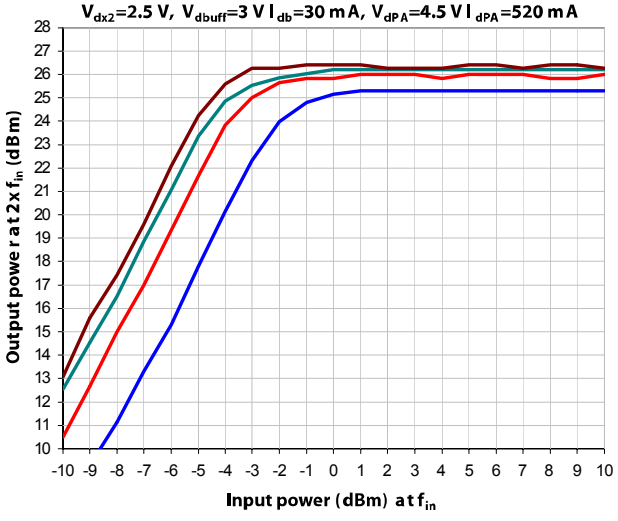

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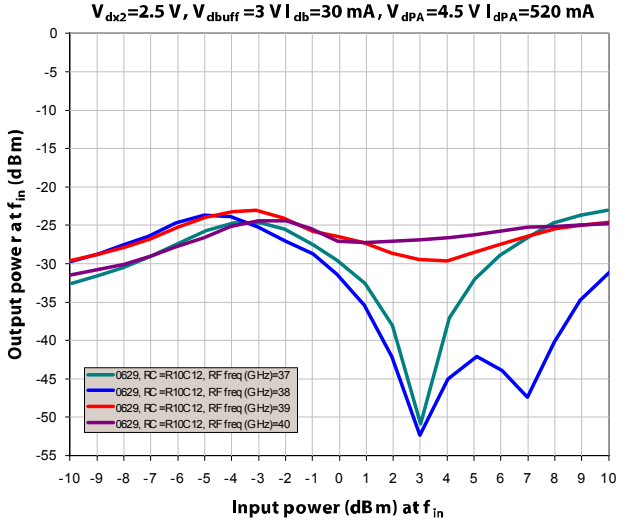
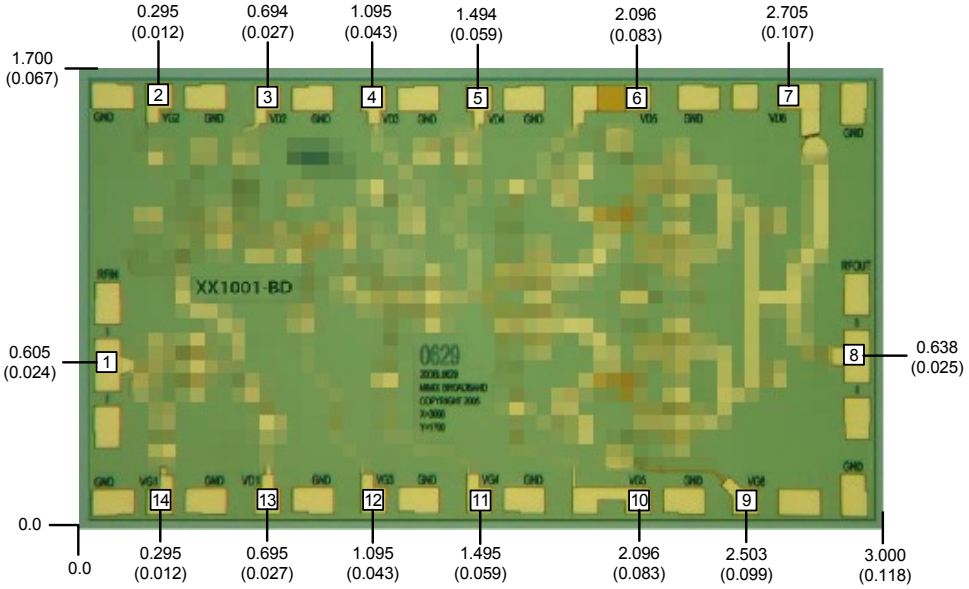


Mechanical Drawing

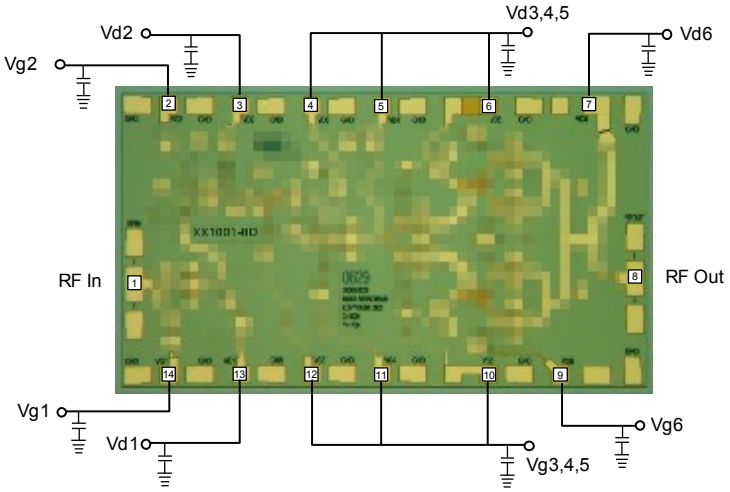


(Note: Engineering designator is 20DBL0629)

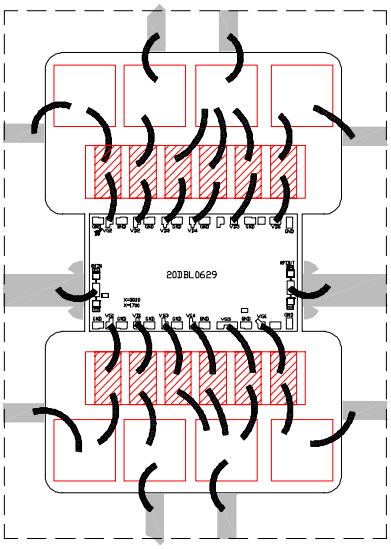
Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.
Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold
All DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF Bond Pads are 0.100 x 0.200 (0.004 x 0.008)
Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 3.987 mg.

Bond Pad #1 (RF In)	Bond Pad #5 (Vd4)	Bond Pad #9 (Vg6)	Bond Pad #13 (Vd1)
Bond Pad #2 (Vg2)	Bond Pad #6 (Vd5)	Bond Pad #10 (Vg5)	Bond Pad #14 (Vg1)
Bond Pad #3 (Vd2)	Bond Pad #7 (Vd6)	Bond Pad #11 Vg4)	
Bond Pad #4 (Vd3)	Bond Pad #8 (RF Out)	Bond Pad #12 (Vg3)	

Bias Arrangement

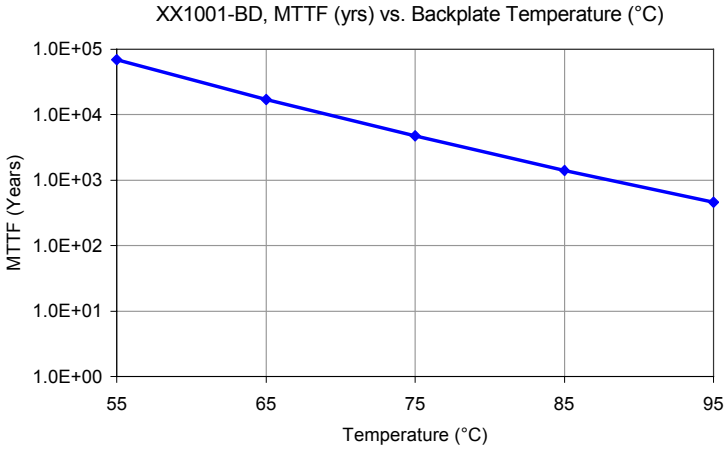


Bypass Capacitors - See App Note [2]



MTTF

MTTF is calculated from accelerated life-time data of single devices and assumes an isothermal back-plate.



App Note [1] Biasing - It is recommended to separately bias each amplifier stage Vd1 through Vd6 at Vd1=2.5V, Vd2=3.0V, Vd(3,4,5,6)=4.5V with Id1<1mA, Id2=20mA, Id3=40mA, Id4=70mA, Id5=150mA, Id6=270mA. Separate biasing is recommended if the amplifier is to be used at high levels of saturation, where gate rectification will alter the effective gate control voltage. As shown in the bonding diagram, it is possible to parallel stages Vd(3,4,5) with Id(3,4,5)=260mA while maintaining satisfactory performance. For non-critical applications it is possible to parallel stages Vd(3,4,5,6) together and adjust the common gate voltage Vg(3,4,5,6) for total drain current Id(total)=530mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.7V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Bias Arrangement -
For Parallel Stage Bias (Recommended for general applications) -- The same as Individual Stage Bias but all the drain pad DC bypass capacitors (~100-200 pF) can be combined. Additional DC bypass capacitance (~0.01 uF) is also recommended to all DC or combination (if gate or drains are tied together) of DC bias pads. Vd(3,4,5,6) or Vg(3,4,5,6) have been tied together but can be left open.

For Individual Stage Bias (Recommended for saturated applications) -- Each DC pad (Vd1,2,3,4,5,6 and Vg1,2,3,4,5,6) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. Additional DC bypass capacitance (~0.01 uF) is also recommended.

Lead-Free Package Dimensions/Layout

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.