PS12013-A

INTEGRATED FUNCTIONS AND FEATURES

- 3-Phase IGBT inverter bridge configured by the latest 3rd. generation IGBT and diode technologies.
- Circuit for dynamic braking of motor regenerative energy.
- Inverter output current capability Io (Note 1) :

Type Name	100% load	150% over load
PS12013-A	1.8A (rms)	2.7A (rms), 1min

(Note 1) : The inverter output current is assumed to be sinusoidal and the peak current value of each of the above loading cases is defined as : $Iop = Io \times \sqrt{2}$

## INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS:

- For P-Side IGBTs : Drive circuit, High-speed photo-couplers, Short circuit protection (SC), Bootstrap circuit supply scheme (Single drive power supply) and Under-voltage protection (UV).
- For N-Side IGBTs : Drive circuit, Short-circuit protection (SC), Control supply Under voltage and Over voltage protection (OV/UV), System Over temperature protection (OT), Fault output signaling circuit (Fo), and Current-Limit warning signal output (CL).
- For Brake circuit IGBT : Drive circuit.
- Warning and Fault signaling :
    - FO1 : Short circuit protection for lower-leg IGBTs and Input interlocking against spurious arm shoot-through.
    - FO2 : N-side control supply abnormality locking (OV/UV)
    - FO3 : System over-temperature protection (OT).
    - CL : Warning for inverter current overload condition
- For system feedback control : Analogue signal feedback reproducing actual inverter output phase current (3φ).
- Input Interface : 5V CMOS/TTL compatible, Schmitt trigger input, and Arm-Shoot-Through interlock protection.

APPLICATION

Acoustic noise-less 0.4kW/AC400V Class 3 Phase inverter and other motor control applications.
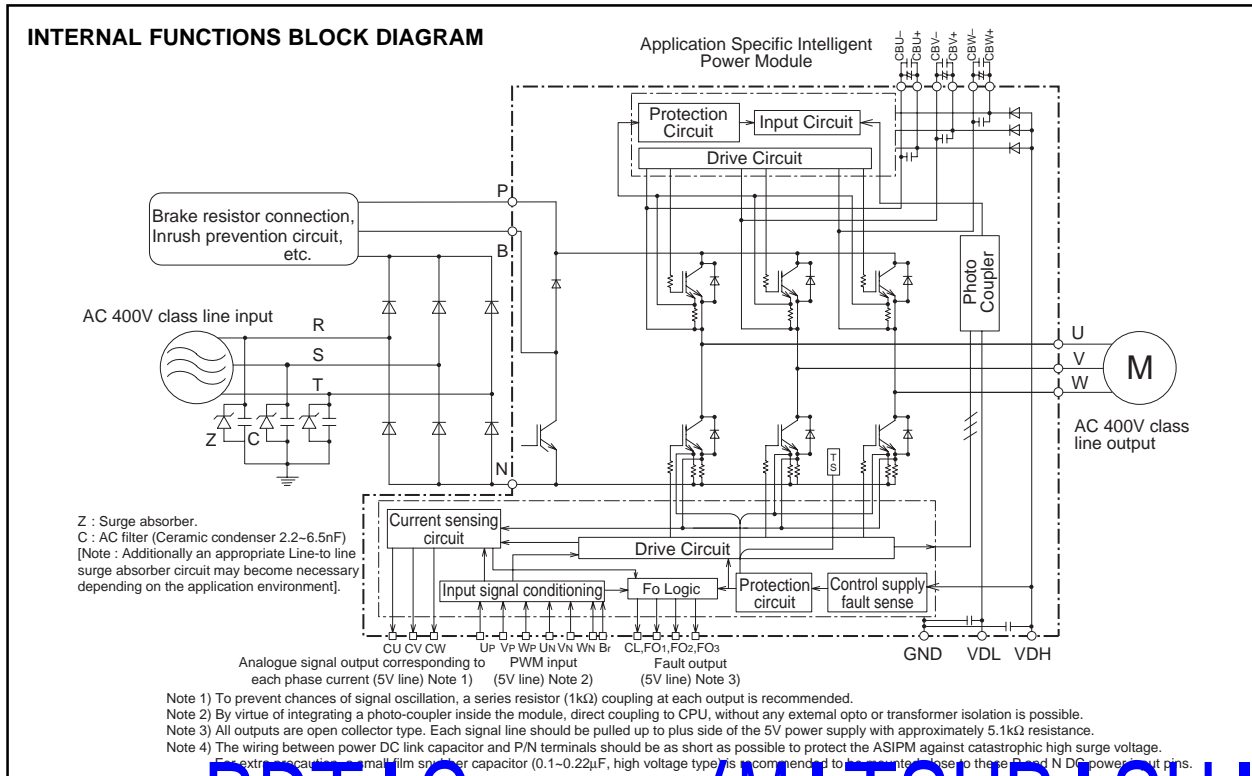
PACKAGE OUTLINES
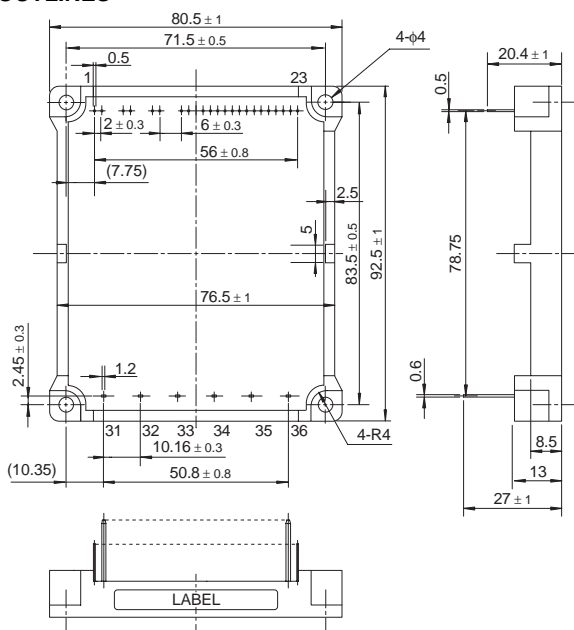
Terminals Assignment:

1	CBU+	31	P
2	CBU–	32	B
3	CBV+	33	N
4	CBV–	34	U
5	CBW+	35	V
6	CBW–	36	W
7	GND		
8	VDL		
9	VDH		
10	CL		
11	FO1		
12	FO2		
13	FO3		
14	CU		
15	CV		
16	CW		
17	UP		
18	VP		
19	WP		
20	UN		
21	VN		
22	WN		
23	Br		

(Fig. 1)

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INTERNAL FUNCTIONS BLOCK DIAGRAM

Note 1) To prevent chances of signal oscillation, a series resistor (1kΩ) coupling at each output is recommended.
Note 2) By virtue of integrating a photo-coupler inside the module, direct coupling to CPU, without any external opto or transformer isolation is possible.
Note 3) All outputs are open collector type. Each signal line should be pulled up to plus side of the 5V power supply with approximately 5.1kΩ resistance.
Note 4) The wiring between power DC link capacitor and P/N terminals should be as short as possible to protect the ASIPM against catastrophic high surge voltage.
For extra precaution, a small film snubber capacitor (0.1~0.22μF, high voltage type) is recommended to be mounted close to these P and N DC power input pins.

(Fig. 2)

MAXIMUM RATINGS (Tj = 25°C)
INVERTER PART (Including Brake Part)

Symbol	Item	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-N	900	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-N, Surge-value	1000	V
V_P or V_N	Each output IGBT collector-emitter static voltage	Applied between P-U, V, W, Br or U, V, W, Br-N	1200	V
$V_{P(S)}$ or $V_{N(S)}$	Each output IGBT collector-emitter surge voltage	Applied between P-U, V, W, Br or U, V, W, Br-N	1200	V
$\pm I_C(\pm I_{cp})$	Each output IGBT collector current	$T_C = 25°C$	±5 (±10)	A
$I_C(I_{cp})$	Brake IGBT collector current	Note : "( )" means Ic peak value	5 (10)	A
$I_F(I_{FP})$	Brake diode anode current		5 (10)	A

CONTROL PART

Symbol	Item	Condition	Ratings	Unit
V_{DH}, V_{DB}	Supply voltage	Applied between V_{DH}-GND, C_{BU+}-C_{BU-}, C_{BV+}-C_{BV-}, C_{BW+}-C_{BW-}	20	V
V_{DL}	Supply voltage	Applied between V_{DL}-GND	7	V
V_{CIN}	Input signal voltage	Applied between $U_P \cdot V_P \cdot W_P \cdot U_N \cdot V_N \cdot W_N \cdot B_r$-GND	$-0.5 \sim V_{DL}+0.5$	V
V_{FO}	Fault output supply voltage	Applied between $F_{O1} \cdot F_{O2} \cdot F_{O3}$-GND	$-0.5 \sim 7$	V
I_{FO}	Fault output current	Sink current of $F_{O1} \cdot F_{O2} \cdot F_{O3}$	15	mA
V_{CL}	Current-limit warning output voltage	Applied between CL-GND	$-0.5 \sim 7$	V
I_{CL}	CL output current	Sink current of CL	15	mA
I_{CO}	Analogue-current-signal output current	Sink current of $CU \cdot CV \cdot CW$	±1	mA

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FLAT-BASE TYPE
INSULATED TYPE

TOTAL SYSTEM

Symbol	Item	Condition		Ratings	Unit
Tj	Junction temperature		(Note 2)	−20 ~ +125	°C
Tstg	Storage temperature	—		−40 ~ +125	°C
TC	Module case operating temperature		(Fig. 3)	−20 ~ +100	°C
VISO	Isolation voltage	60 Hz sinusoidal AC for 1 minute, between all terminals and base plate.		2500	Vrms
—	Mounting torque	Mounting screw: M3.5		0.78 ~ 1.27	N·m

Note 2) : The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the ASIPM to ensure safe operation. However, these power elements can endure instantaneous junction temperature as high as 150°C. To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is to be provided before use.

CASE TEMPERATURE MEASUREMENT POINT (3mm from the base surface)
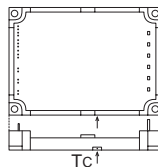
(Fig. 3)

THERMAL RESISTANCE

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
Rth(jc)Q		Inverter IGBT (1/6)	—	—	3.0	°C/W
Rth(jc)F	Junction to case Thermal Resistance	Inverter FWDi (1/6)	—	—	7.3	°C/W
Rth(jc)QB		Brake IGBT	—	—	3.0	°C/W
Rth(jc)FB		Brake FWDi	—	—	7.3	°C/W
Rth(c-f)	Contact Thermal Resistance	Case to fin, thermal grease applied (1 Module)	—	—	0.040	°C/W

ELECTRICAL CHARACTERISTICS (Tj = 25°C, VDH = 15V , VDB = 15V, VDL = 5V unless otherwise noted)

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
VCE(sat)	Collector-emitter saturation voltage	VDL = 5V, VDH = VDB = 15V Input = ON, Tj = 25°C, Ic = 5A	—	—	3.6	V
VEC	FWDi forward voltage	Tj = 25°C, Ic = −5A, Input = OFF	—	—	3.5	V
VCE(sat)Br	Brake IGBT Collector-emitter saturation voltage	VDL = 5V, VDH = 15V Input = ON, Tj = 25°C, Ic = 5A	—	—	3.6	V
VFBr	Brake diode forward voltage	Tj = 25°C, IF = 5A, Input = OFF	—	—	3.5	V
ton		1/2 Bridge inductive, Input = ON	0.3	1.2	2.0	μs
tc(on)	Switching times	VCC = 600V, Ic = 5A, Tj = 125°C	—	0.5	1.4	μs
toff		VDL = 5V, VDH = 15V, VDB = 15V	—	2.2	4.0	μs
tc(off)		Note : ton, toff include delay time of the internal control circuit.	—	0.9	1.6	μs
trr	FWD reverse recovery time		—	0.2	—	μs
	Short circuit endurance (Output, Arm, and Load, Short Circuit Modes)	VCC ≤ 800V, Input = ON (One-Shot) Tj = 125°C start 13.5V ≤ VDH = VDB = ≤ 16.5V	• No destruction • FO output by protection operation			
	Switching SOA	VCC ≤ 800V, Tj ≤ 125°C, Ic < IOL(CL) operation level, Input = ON, 13.5V ≤ VDH = VDB = ≤ 16.5V	• No destruction • No protecting operation • No FO output			
IDH	VDH Circuit Current	VDL = 5V, VDH = 15V, VCIN = 5V	—	—	150	mA
IDL	VDL Circuit Current	VDL = 5V, VDH = 15V, VCIN = 5V	—	—	50	mA
Vth(on)	Input on threshold voltage		0.8	1.4	2.0	V
Vth(off)	Input off threshold voltage		2.5	3.0	4.0	V
Ri	Input pull-up resistor	Integrated between input terminal-VDH	—	150	—	kΩ

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ELECTRICAL CHARACTERISTICS (Tj = 25°C, VDH = 15V, VDB = 15V, VDL = 5V unless otherwise noted)

Symbol	Item		Condition		Ratings			Unit
					Min.	Typ.	Max.	
fPWM	PWM input frequency		TC ≤ 100°C, Tj ≤ 125°C		2	—	15	kHz
txx	Allowable input on-pulse width		VDH = 15V, VDL = 5V, TC = −20°C ~ +100°C Note 3)		2	—	500	µs
tdead	Allowable input signal dead time for blocking arm shoot-through		Relates to corresponding inputs (Except brake part) TC = −20°C ~ +100°C		4.0	—	—	µs
tint	Input inter-lock sensing		Relates to corresponding inputs (Except brake part)		—	65	100	ns
VCO	Analogue signal linearity with output current		Ic = 0A	VDH = 15V	1.87	2.27	2.57	V
VC+(200%)			Ic = IOP(200%)	VDL = 5V	0.77	1.17	1.47	V
VC−(200%)			Ic = −IOP(200%)	TC = −20 ~ 100°C (Fig.4)	2.97	3.37	3.67	V
|∆VCO|	Offset change area vs temperature		VDH = 15V, VDL = 5V, TC = −20 ~ 100°C		—	15	—	mV
VC+	Analogue signal output voltage limit		Ic > IOP(200%), VDH = 15V,		—	—	0.7	V
VC−			VDL = 5V (Fig. 4)		4.0	—	—	V
∆VC(200%)	Analogue signal overall linear variation		|VCO-VC±(200%)|		—	1.1	—	V
rCH	Analogue signal data hold accuracy		Correspond to max. 500µs data hold period only, Ic = IOP(200%) (Fig. 5)		−5	—	5	%
td(read)	Analogue signal reading time		After input signal trigger point (Fig. 8)		—	3	—	µs
ICL(H)	Signal output current of CL operation	Idle	Open collector onput		—	—	1	µA
ICL(L)		Active			—	1	—	mA
±IOL	CL warning operation level		VDL = 5V, VDH = 15V, TC = −20 ~ 100°C (Note 4)		4.84	5.85	7.38	A
SC	Short circuit current trip level		Tj = 25°C (Fig. 7), (Note 5)		8.2	14.4	20.9	A
OT	Over tenperature protection	Trip level	VDL = 5V, VDH = 15V		100	110	120	°C
OTr		Reset level			—	90	—	°C
UVDB	Supply circuit under and over voltage protection	Trip level	TC = −20°C ~ +100°C Tj ≤ 125°C		10.0	11.0	12.0	V
UVDBr		Reset level			10.5	11.5	12.5	V
UVDH		Trip level			11.05	12.00	12.75	V
UVDHr		Reset level			11.55	12.50	13.25	V
OVDH		Trip level			18.00	19.20	20.15	V
OVDHr		Reset level			16.50	17.50	18.65	V
tdv		Filter time			—	10	—	µs
IFO(H)	Fault output current	Idle	Open collector output		—	—	1	µA
IFO(L)		Active			—	1	—	mA

(Note 3) : (a) Allowable minimum input on-pulse width : This item applies to P-side circuit only.
    (b) Allowable maximum input on-pulse width : This item applies to both P-side and N-side circuits excluding the brake circuit.
(Note4) : CL output : The "current limit warning (CL) operation circuit outputs warning signal whenever the arm current exceeds this limit. The circuit is reset automatically by the next input signal and thus, it operates on a pulse-by-pulse scheme.
(Note5) : The short circuit protection works instantaneously when a high short circuit current flows through an internal IGBT rising up momentarily. The protection function is, thus meant primarily to protect the ASIPM against short circuit distraction. Therefore, this function is not recommended to be used for any system load current regulation or any over load control as this might, cause a failure due to excessive temperature rise. Instead, the analogue current output feature or the over load warning feature (CL) should be appropriately used for such current regulation or over load control operation. In other words, the PWM signals to the ASIPM should be shut down, in principle, and not to be restarted before the junction temperature would recover to normal, as soon as a fault is feed back from its FO1 pin of the ASIPM indicating a short circuit situation.

RECOMMENDED CONDITIONS

Symbol	Item	Condition	Ratings			Unit
			Min.	Typ.	Max.	
VCC	Supply voltage	Applied between P-N	—	600	800	V
VDH, VDB	Control supply voltage	Applied between VDH-GND, CBU+-CBU−, CBV+-CBV−, CBW+-CBW−	13.5	15.0	16.5	V
VDL	Control supply voltage	Applied between VDL-GND	4.8	5.0	5.2	V
∆VDH, ∆VDB, ∆VDL	Supply voltage ripple		−1	—	+1	V/µs
VCIN(on)	Input ON voltage		—	—	0.3	V
VCIN(off)	Input OFF voltage		4.8	—	—	V
fPWM	PWM Input frequency	Using application circuit	2	10	15	kHz
tdead	Arm shoot-through blocking time	Using application circuit	4.0	—	—	µs

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Fig. 4 OUTPUT CURRENT ANALOGUE SIGNALING LINEARITY

Real load current peak value.(%)($I_C = I_0 \times \sqrt{2}$)
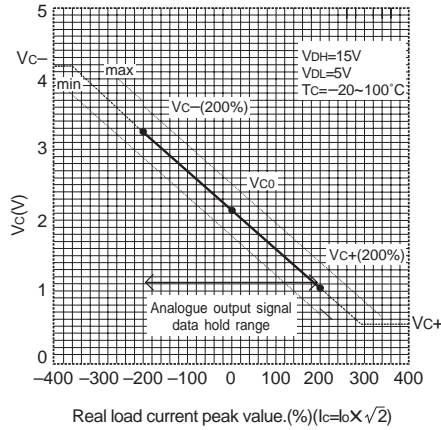
Fig. 5 OUTPUT CURRENT ANALOGUE SIGNALING "DATA HOLD" DEFINITION

$$r_{CH} = \frac{V_{CH}(505\mu s) - V_{CH}(5\mu s)}{V_{CH}(5\mu s)}$$
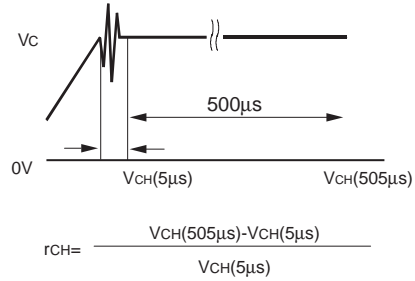
Note ; Ringing happens around the point where the signal output voltage changes state from "analogue" to "data hold" due to test circuit arrangement and instrumentational trouble. Therefore, the rate of change is measured at a 5 μs delayed point.

Fig. 6 INPUT INTERLOCK OPERATION TIMING CHART
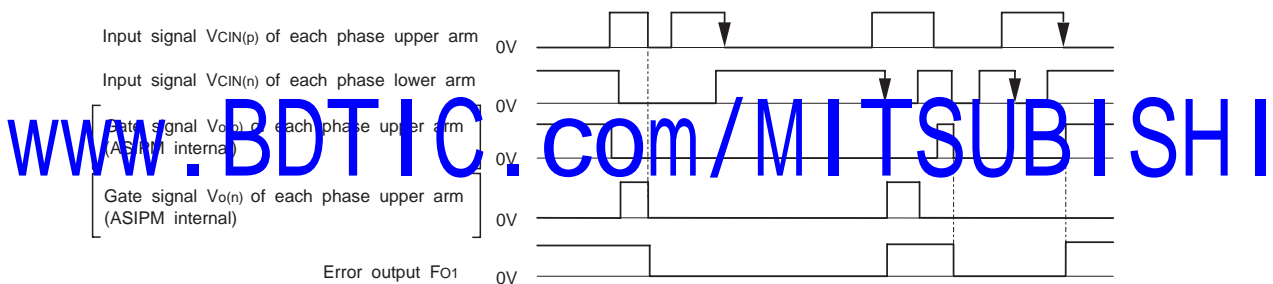
Note : Input interlock protection circuit ; It is operated when the input signals for any upper-arm / lower-arm pair of a phase are simultaneously in "LOW" level.

By this interlocking, both upper and lower IGBTs of this mal-triggered phase are cut off, and "F_O" signal is outputted. After an "input interlock" operation the circuit is latched. The "F_O" is reset by the high-to-low going edge of either an upper-leg, or a lower-leg input, whichever comes in later.

Fig. 7 TIMING CHART AND SHORT CIRCUIT PROTECTION OPERATION
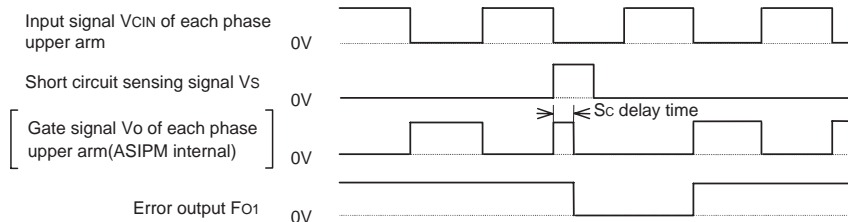
Note : Short circuit protection operation. The protection operates with "F_O" flag and reset on a pulse-by-pulse scheme. The protection by gate shutdown is given only to the IGBT that senses an overload (excluding the IGBT for the "Brake").

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Fig. 8 INVERTER OUTPUT ANALOGUE CURRENT SENSING AND SIGNALING TIMING CHART.
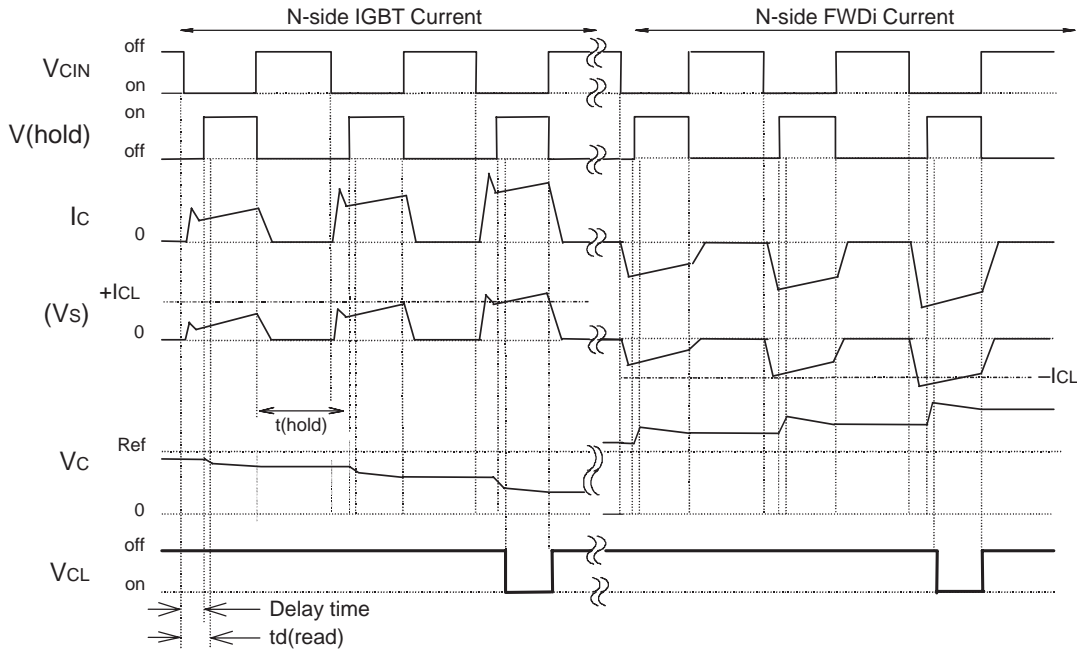
Fig. 9 START-UP SEQUENCE

Normally at start-up, Fo and CL output signals will be pulled-up High to V_{DL} voltage (OFF level); however, F_{O1} output may fall to Low (ON) level at the instant of the first ON input pulse to an N-Side IGBT. This can happen particularly when the boot-strap capacitor is of large size. F_{O1} resetting sequence (together with the boot-strap charging sequence) is explained in the following graph
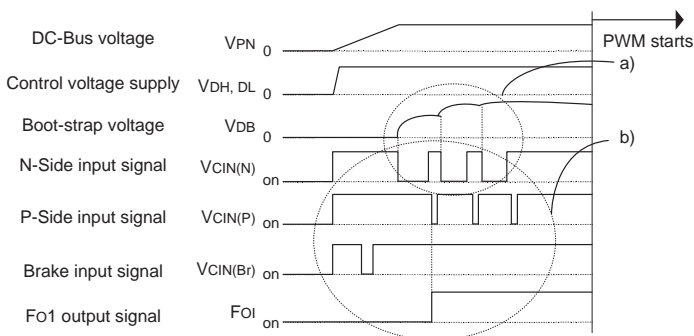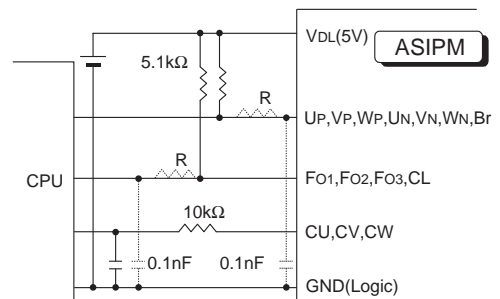

Fig. 10 RECOMMENDED I/O INTERFACE CIRCUIT

a) Boot-strap charging scheme :
Apply a train of short ON pulses at all N-IGBT input pins for adequate charging (pulse width = approx. 20µs number of pulses =10 ~ 500 depending on the boot-strap capacitor size)

b) F_{O1} resetting sequence:
Apply ON signals to the following input pins : Br → Un/Vn/Wn → Up/Vp/Wp in that order.

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