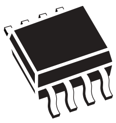
M25P05-A

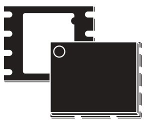
512-Kbit, serial flash memory, 50 MHz SPI bus interface

Features

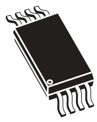
- 512 Kbits of flash memory
- Page program (up to 256 bytes) in 1.4 ms (typical)
- Sector erase (256 Kbits) in 0.65 s (typical)
- Bulk erase (512 Kbits) in 0.85 s (typical)
- 2.3 to 3.6 V single supply voltage
- SPI bus compatible serial interface
- 50 MHz clock rate (maximum)
- Deep power-down mode 1 µA (typical)
- Electronic signatures
  - JEDEC standard two-byte signature (2010h)
  - RES instruction, one-byte, signature (05h), for backward compatibility
- More than 100,000 erase/program cycles per sector
- More than 20 years data retention
- ECOPACK® packages available



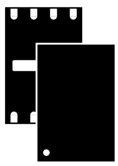
SO8 (MN)
150 mil width



VFQFPN8 (MP)
(MLP8)



TSSOP8 (DW)



UFDFPN8 (MB)
2 x 3 mm

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1 Description

The M25P05-A is a 512-Kbit (64 Kbits ×8) serial flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

The memory can be programmed 1 to 256 bytes at a time, using the page program instruction.

The memory is organized as 2 sectors, each containing 128 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 256 pages, or 65,536 bytes.

The whole memory can be erased using the bulk erase instruction, or a sector at a time, using the sector erase instruction.

Figure 1. Logic diagram

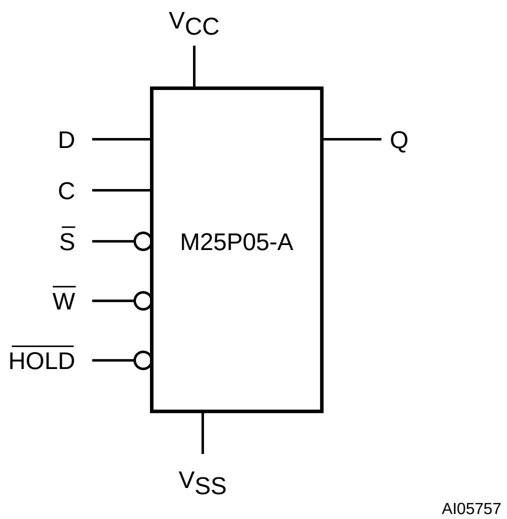
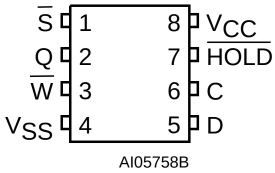


Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data input	Input
Q	Serial Data output	Output
$\overline{S}$	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	Supply
V_{SS}	Ground	Supply

Figure 2. SO, VFQFPN and TSSOP connections



1. There is an exposed central pad on the underside of the VFQFPN package. This is pulled, internally, to V_{SS}, and must not be allowed to be connected to any other voltage or signal line on the PCB.
2. See *Package mechanical* section for package dimensions, and how to identify pin-1.

2 Signal descriptions

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is High, the device is deselected and Serial Data output (Q) is at high impedance. Unless an internal program, erase or write status register cycle is in progress, the device will be in the standby mode (this is not the deep power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.

After power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are don't care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.

2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP1 and BP0 bits of the status register).

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

3 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

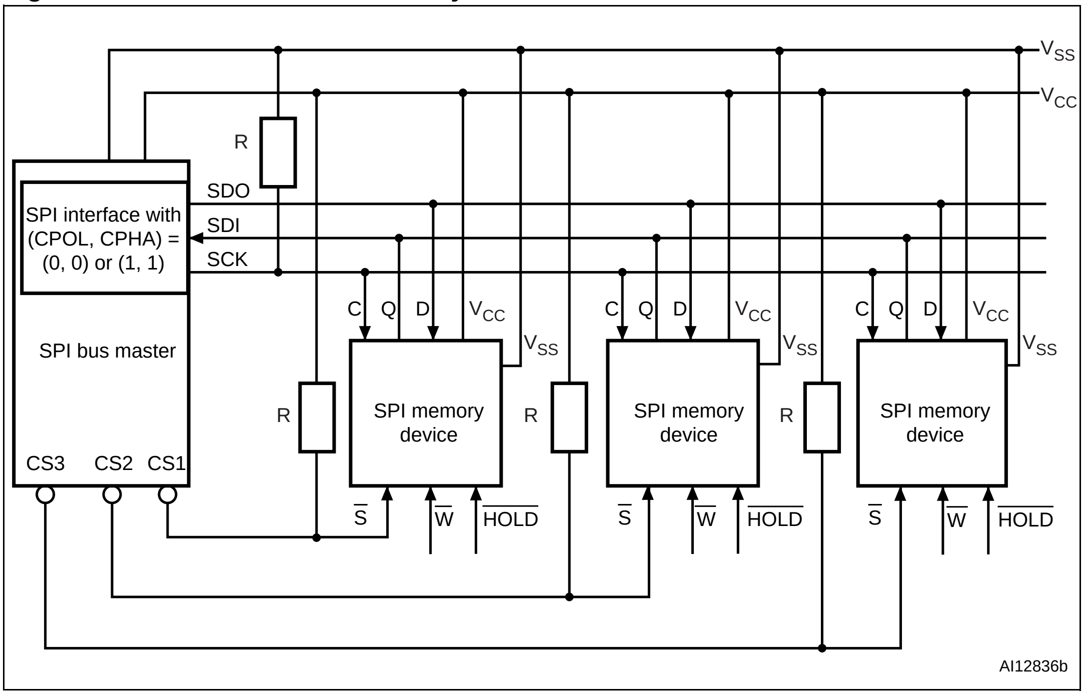
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 3. Bus master and memory devices on the SPI bus

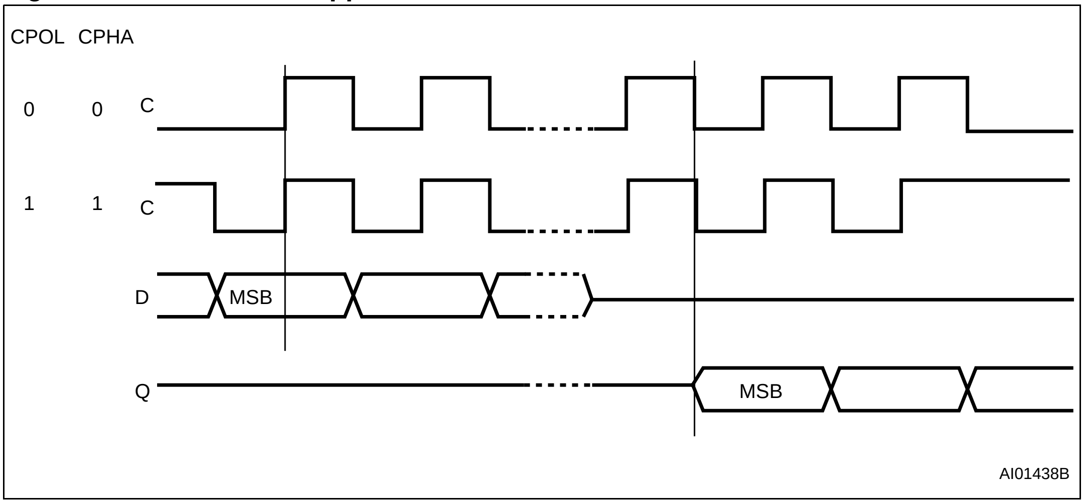


1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 3 shows an example of three devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, the other devices are high impedance. Resistors R (represented in *Figure 3*) ensure that the M25P05-A is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state. As the bus master may enter a state where all inputs/outputs are in high impedance at the same time (for example, when the bus master is reset), the clock line (C) must be connected to an external pull-down resistor so that, when all inputs/outputs become high impedance, the $\overline{S}$ line is pulled High while the C line is pulled Low (thus ensuring that $\overline{S}$ and C do not become High at the same time, and so, that the t_{SHCH} requirement is met). The typical value of R is 100 kΩ, assuming that the time constant R*C_p (C_p = parasitic capacitance of the bus line) is shorter than the time during which the bus master leaves the SPI bus in high impedance.

Example: C_p = 50 pF, that is R*C_p = 5 µs <=> the application must ensure that the bus master never leaves the SPI bus in the high impedance state for a time period shorter than 5 µs.

Figure 4. SPI modes supported



4 Operating features

4.1 Page programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a page program (PP) sequence, which consists of four bytes plus data. This is followed by the internal program cycle (of duration t_{PP}).

To spread this overhead, the page program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Section 6.8: Page program (PP)* and *Table 14: Instruction times*).

4.2 Sector erase and bulk erase

The page program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved either a sector at a time, using the sector erase (SE) instruction, or throughout the entire memory, using the bulk erase (BE) instruction. This starts an internal erase cycle (of duration t_{SE} or t_{BE}).

The erase instruction must be preceded by a write enable (WREN) instruction.

4.3 Polling during a write, program or erase cycle

A further improvement in the time to write status register (WRSR), program (PP) or erase (SE or BE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, or t_{BE}). The write in progress (WIP) bit is provided in the status register so that the application program can monitor its value, polling it to establish when the previous write cycle, program cycle or erase cycle is complete.

4.4 Active power, standby power and deep power-down modes

When Chip Select ($\overline{S}$) is Low, the device is selected, and in the active power mode.

When Chip Select ($\overline{S}$) is High, the device is deselected, but could remain in the active power mode until all internal cycles have completed (program, erase, write status register). The device then goes in to the standby power mode. The device consumption drops to I_{CC1}.

The deep power-down mode is entered when the specific instruction (the deep power-down (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the release from deep power-down and read electronic signature (RES) instruction) is executed.

While in the deep power-down mode, the device ignores all write, program and erase instructions (see *Section 6.11: Deep power-down (DP)*). This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent write, program or erase instructions.

4.5 Status register

The status register contains a number of status and control bits, as shown in *Table 6*, that can be read or set (as appropriate) by specific instructions.

4.5.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write status register, program or erase cycle.

4.5.2 WEL bit

The write enable latch (WEL) bit indicates the status of the internal write enable latch.

4.5.3 BP1, BP0 bits

The block protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against program and erase instructions.

4.5.4 SRWD bit

The status register write disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the hardware protected mode. In this mode, the non-volatile bits of the status register (SRWD, BP1, BP0) become read-only bits.

4.6 Protection modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the M25P05-A features the following data protection mechanisms:

- Power on reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification
- Program, erase and write status register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution
- All instructions that modify data must be preceded by a write enable (WREN) instruction to set the write enable latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write disable (WRDI) instruction completion
  - Write status register (WRSR) instruction completion
  - Page program (PP) instruction completion
  - Sector erase (SE) instruction completion
  - Bulk erase (BE) instruction completion
- The block protect (BP1, BP0) bits allow part of the memory to be configured as read-only. This is the software protected mode (SPM)
- The Write Protect ($\overline{W}$) signal, in co-operation with the status register write disable (SRWD) bit, allows the block protect (BP1, BP0) bits and status register write disable (SRWD) bit to be write-protected. This is the hardware protected mode (HPM)
- In addition to the low power consumption feature, the deep power-down mode offers extra software protection, as all write, program and erase instructions are ignored.

Table 2. Protected area sizes

<table>
<tr><th colspan="2">Status Register content</th><th colspan="2">Memory content</th></tr>
<tr><th>BP1 bit</th><th>BP0 bit</th><th>Protected area</th><th>Unprotected area</th></tr>
<tr><td>0</td><td>0</td><td>none</td><td>All sectors (sectors 0 and 1)</td></tr>
<tr><td>0</td><td>1</td><td colspan="2" rowspan="2">No protection against page program (PP) and sector erase (SE)
All sectors (sectors 0 and 1) protected against bulk erase (BE)</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>All sectors (sectors 0 and 1)</td><td>none</td></tr>
</table>

1. The device is ready to accept a bulk erase instruction if, and only if, both block protect (BP1, BP0) are 0.

4.7 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any write status register, program or erase cycle that is currently in progress.

To enter the hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

The hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in *Figure 5*).

The hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low.

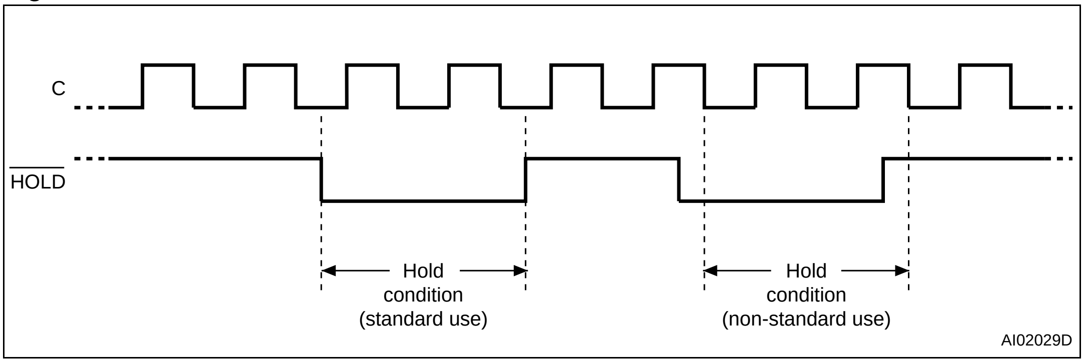
If the falling edge does not coincide with Serial Clock (C) being Low, the hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the hold condition ends after Serial Clock (C) next goes Low (this is shown in *Figure 5*).

During the hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are don't care.

Normally, the device is kept selected, with Chip Select ($\overline{S}$) driven Low, for the whole duration of the hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the hold condition.

If Chip Select ($\overline{S}$) goes High while the device is in the hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{HOLD}$) High, and then to drive Chip Select ($\overline{S}$) Low. This prevents the device from going back to the hold condition.

Figure 5. Hold condition activation



5 Memory organization

The memory is organized as:

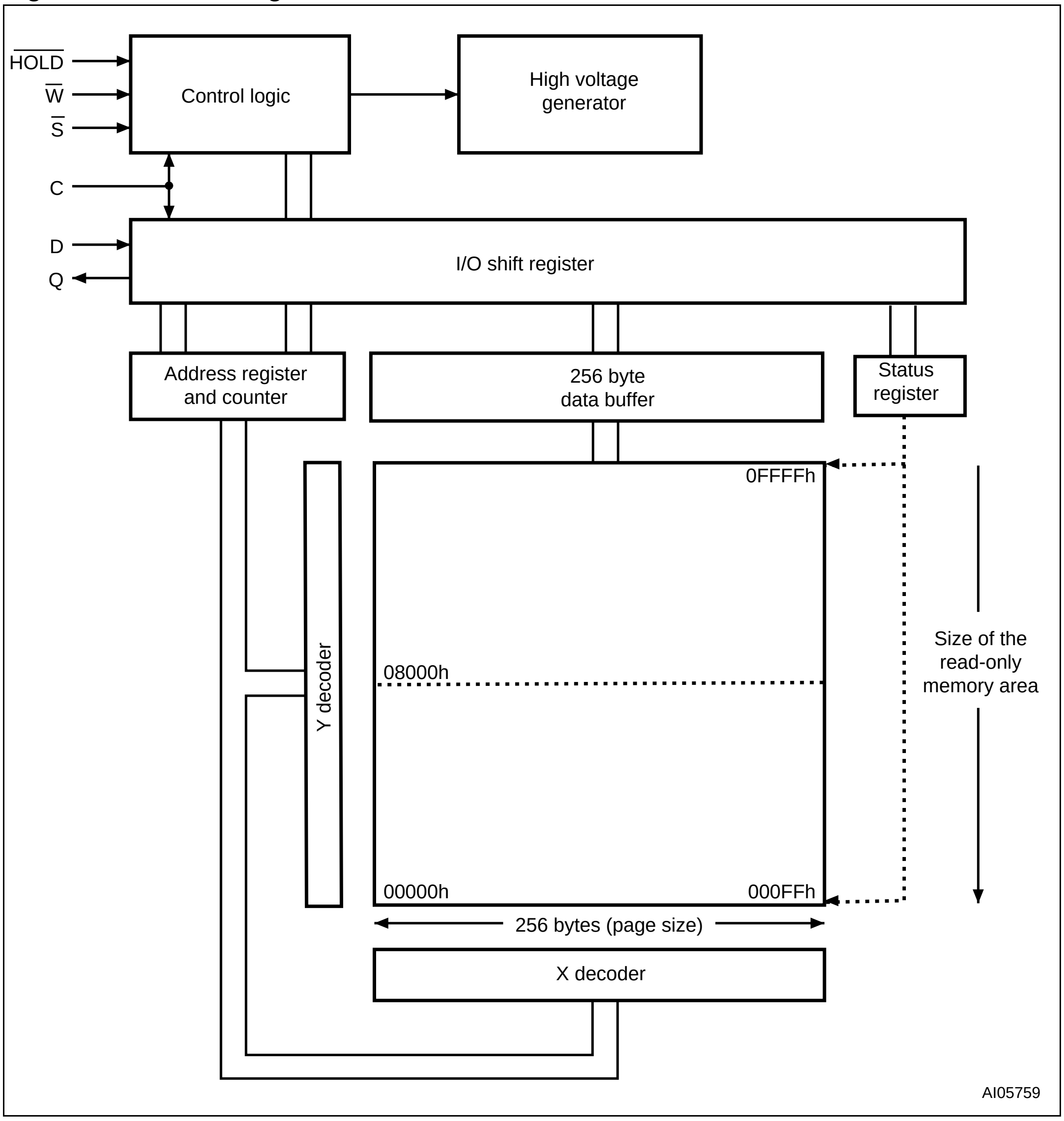
- 65,536 bytes (8 bits each)
- 2 sectors (256 Kbits, 32768 bytes each)
- 256 pages (256 bytes each).

Each page can be individually programmed (bits are programmed from 1 to 0). The device is sector or bulk erasable (bits are erased from 0 to 1) but not page erasable.

Table 3. Memory organization

Sector	Address range	
1	08000h	0FFFFh
0	00000h	07FFFh

Figure 6. Block diagram



6 Instructions

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in *Table 4*.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select ($\overline{S}$) must be driven High after the last bit of the instruction sequence has been shifted in.

In the case of a read data bytes (READ), read data bytes at higher speed (Fast_Read), read identification (RDID), read status register (RDSR) or release from deep power-down, and read electronic signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a page program (PP), sector erase (SE), bulk erase (BE), write status register (WRSR), write enable (WREN), write disable (WRDI) or deep power-down (DP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a write status register cycle, program cycle or erase cycle are ignored, and the internal write status register cycle, program cycle or erase cycle continues unaffected.

Table 4. Instruction set

Instruction	Description	One-byte instruction code		Address bytes	Dummy bytes	Data bytes
WREN	Write enable	0000 0110	06h	0	0	0
WRDI	Write disable	0000 0100	04h	0	0	0
RDID(1)	Read identification	1001 1111	9Fh	0	0	1 to 3
RDSR	Read status register	0000 0101	05h	0	0	1 to ∞
WRSR	Write status register	0000 0001	01h	0	0	1
READ	Read data bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read data bytes at higher speed	0000 1011	0Bh	3	1	1 to ∞
PP	Page program	0000 0010	02h	3	0	1 to 256
SE	Sector erase	1101 1000	D8h	3	0	0
BE	Bulk erase	1100 0111	C7h	0	0	0
DP	Deep power-down	1011 1001	B9h	0	0	0
RES	Release from deep power-down, and read electronic signature	1010 1011	ABh	0	3	1 to ∞
	Release from deep power-down			0	0	0

1. The read identification (RDID) instruction is available only in products with process technology code X and Y (see application note AN1995).

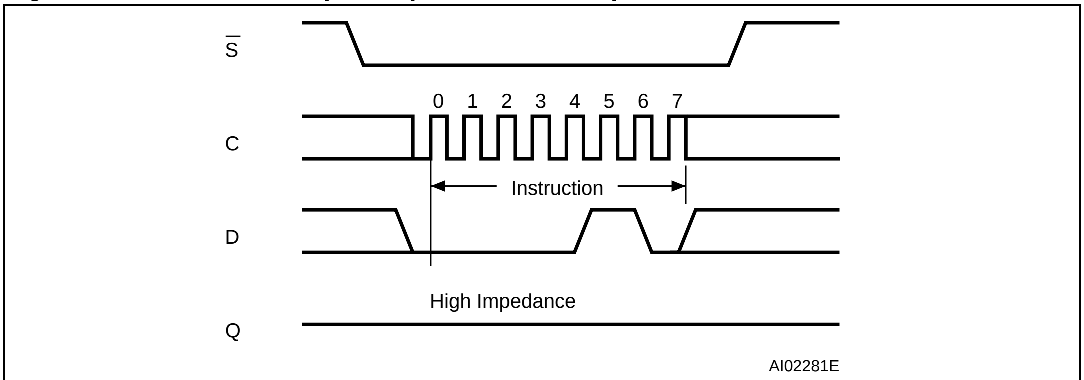
6.1 Write enable (WREN)

The write enable (WREN) instruction (*Figure 7*) sets the write enable latch (WEL) bit.

The write enable latch (WEL) bit must be set prior to every page program (PP), sector erase (SE), bulk erase (BE) and write status register (WRSR) instruction.

The write enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 7. Write enable (WREN) instruction sequence



6.2 Write disable (WRDI)

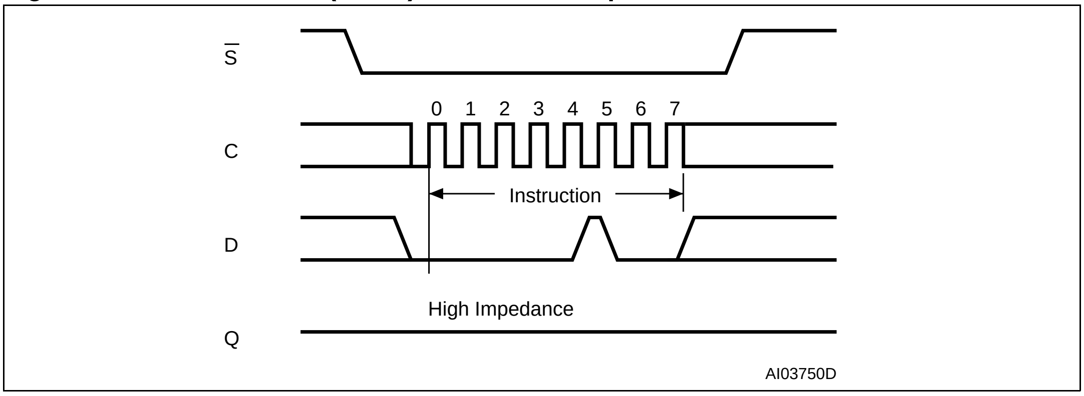
The write disable (WRDI) instruction (*Figure 8*) resets the write enable latch (WEL) bit.

The write disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

The write enable latch (WEL) bit is reset under the following conditions:

- Power-up
- Write disable (WRDI) instruction completion
- Write status register (WRSR) instruction completion
- Page program (PP) instruction completion
- Sector erase (SE) instruction completion
- Bulk erase (BE) instruction completion.

Figure 8. Write disable (WRDI) instruction sequence



6.3 Read identification (RDID)

The read identification (RDID) instruction is available in products with process technology code X and Y.

The read identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 20h for Numonyx. The device identification is assigned by the device manufacturer, and indicates the memory type in the first byte (20h), and the memory capacity of the device in the second byte (10h).

Any read identification (RDID) instruction while an erase or program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The read identification (RDID) instruction should not be issued while the device is in deep power-down mode.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in *Figure 9*.

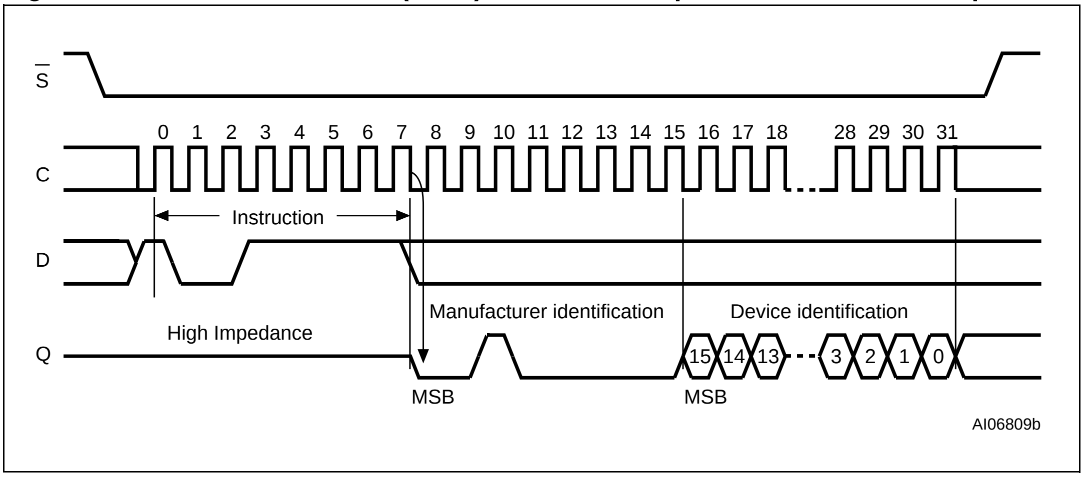
The read identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the standby power mode. Once in the standby power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 5. Read identification (RDID) data-out sequence

Manufacturer identification	Device identification	
	Memory type	Memory capacity
20h	20h	10h

Figure 9. Read identification (RDID) instruction sequence and data-out sequence



6.4 Read status register (RDSR)

The read status register (RDSR) instruction allows the status register to be read. The status register may be read at any time, even while a program, erase or write status register cycle is in progress. When one of these cycles is in progress, it is recommended to check the write in progress (WIP) bit before sending a new instruction to the device. It is also possible to read the status register continuously, as shown in *Figure 10*.

Table 6. Status register format

b7							b0
SRWD	0	0	0	BP1	BP0	WEL	WIP
Status register write protect				Block protect bits	Block protect bits	Write enable latch bit	Write in progress bit

The status and control bits of the status register are as follows:

6.4.1 WIP bit

The write in progress (WIP) bit indicates whether the memory is busy with a write status register, program or erase cycle. When set to ‘1’, such a cycle is in progress, when reset to ‘0’ no such cycle is in progress.

6.4.2 WEL bit

The write enable latch (WEL) bit indicates the status of the internal write enable latch. When set to ‘1’ the internal write enable latch is set, when set to ‘0’ the internal write enable latch is reset and no write status register, program or erase instruction is accepted.

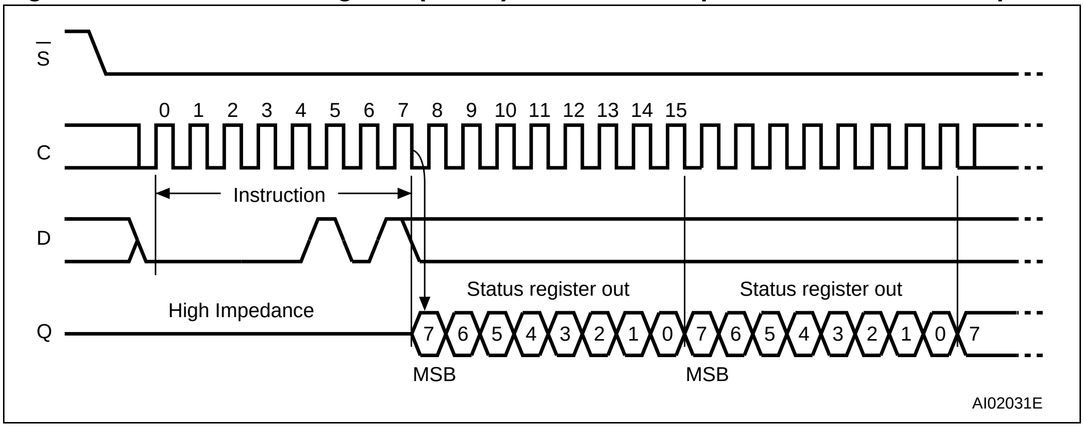
6.4.3 BP1, BP0 bits

The block protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against program and erase instructions. These bits are written with the write status register (WRSR) instruction. When one or both of the block protect (BP1, BP0) bits is set to ‘1’, the relevant memory area (as defined in *Table 2*) becomes protected against page program (PP) and sector erase (SE) instructions. The block protect (BP1, BP0) bits can be written provided that the hardware protected mode has not been set. The bulk erase (BE) instruction is executed if, and only if, both block protect (BP1, BP0) bits are 0.

6.4.4 SRWD bit

The status register write disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and write protect ($\overline{W}$) signal allow the device to be put in the hardware protected mode (when the status register write disable (SRWD) bit is set to ‘1’, and write protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the status register (SRWD, BP1, BP0) become read-only bits and the write status register (WRSR) instruction is no longer accepted for execution.

Figure 10. Read status register (RDSR) instruction sequence and data-out sequence



6.5 Write status register (WRSR)

The write status register (WRSR) instruction allows new values to be written to the status register. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded and executed, the device sets the write enable latch (WEL).

The write status register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data input (D).

The instruction sequence is shown in *Figure 11*.

The write status register (WRSR) instruction has no effect on b6, b5, b4, b1 and b0 of the status register. b6, b5 and b4 are always read as 0.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in. If not, the write status register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed write status register cycle (whose duration is t_W) is initiated. While the write status register cycle is in progress, the status register may still be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed write status register cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) is reset.

The write status register (WRSR) instruction allows the user to change the values of the block protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 2*. The write status register (WRSR) instruction also allows the user to set or reset the status register write disable (SRWD) bit in accordance with the Write Protect ($\overline{W}$) signal. The status register write disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the hardware protected mode (HPM). The write status register (WRSR) instruction is not executed once the hardware protected mode (HPM) is entered.

The protection features of the device are summarized in *Table 7*.

When the status register write disable (SRWD) bit of the status register is 0 (its initial delivery state), it is possible to write to the status register provided that the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the status register write disable (SRWD) bit of the status register is set to '1', two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven High, it is possible to write to the status register provided that the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction
- If Write Protect ($\overline{W}$) is driven Low, it is not possible to write to the status register even if the write enable latch (WEL) bit has previously been set by a write enable (WREN) instruction (attempts to write to the status register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the block protect (BP1, BP0) bits of the status register, are also hardware protected against data modification.

Regardless of the order of the two events, the hardware protected mode (HPM) can be entered:

- by setting the status register write disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low
- or by driving Write Protect ($\overline{W}$) Low after setting the status register write disable (SRWD) bit.

The only way to exit the hardware protected mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

If Write Protect ($\overline{W}$) is permanently tied High, the hardware protected mode (HPM) can never be activated, and only the software protected mode (SPM), using the block protect (BP1, BP0) bits of the status register, can be used.

Figure 11. Write status register (WRSR) instruction sequence

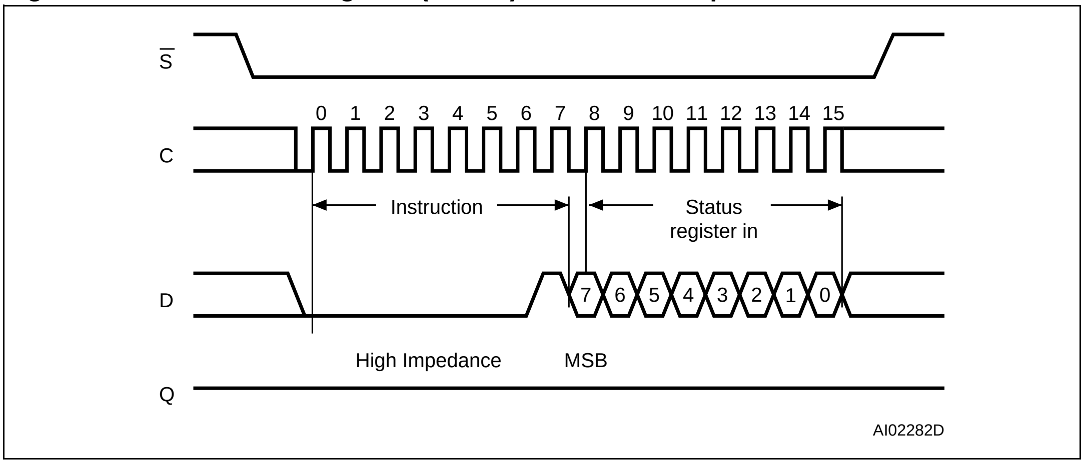


Table 7. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the status register	Memory content	
				Protected area[1]	Unprotected area[1]
1	0	Software protected (SPM)	Status register is writable (if the WREN instruction has set the WEL bit). The values in the SRWD, BP1 and BP0 bits can be changed	Protected against page program, sector erase and bulk erase	Ready to accept page program and sector erase instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	Status register is hardware write protected. The values in the SRWD BP1 and BP0 bits cannot be changed	Protected against page program, sector erase and bulk erase	Ready to accept page program and sector erase instructions

1. As defined by the values in the block protect (BP1, BP0) bits of the status register, as shown in *Table 2*.

6.6 Read data bytes (READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

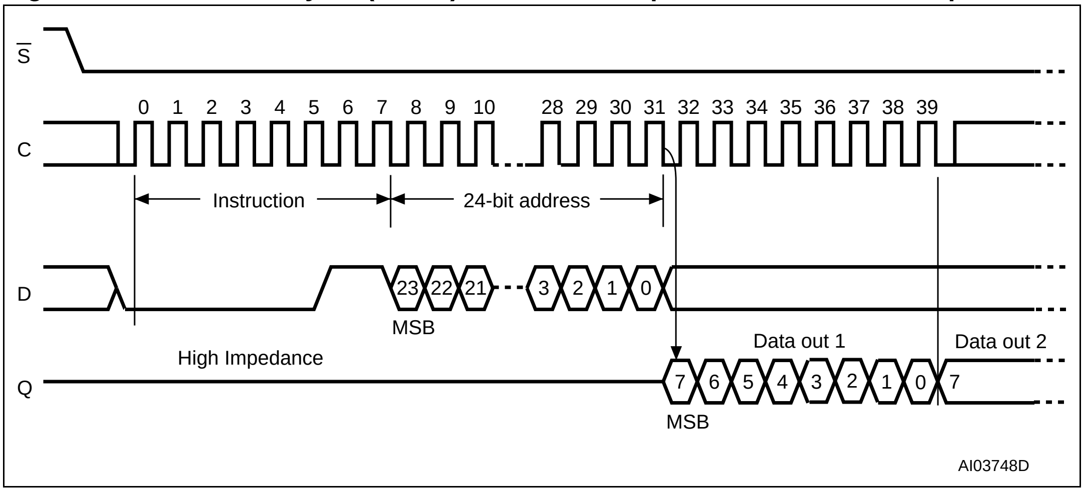
The instruction sequence is shown in *Figure 12*.

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes (READ) instruction.

There is no address roll-over; when the highest address (0FFFFh) is reached, the instruction should be terminated.

The read data bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes (READ) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 12. Read data bytes (READ) instruction sequence and data-out sequence



1. Address bits A23 to A16 must be set to 00h.

6.7 Read data bytes at higher speed (FAST_READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the read data bytes at higher speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data output (Q), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

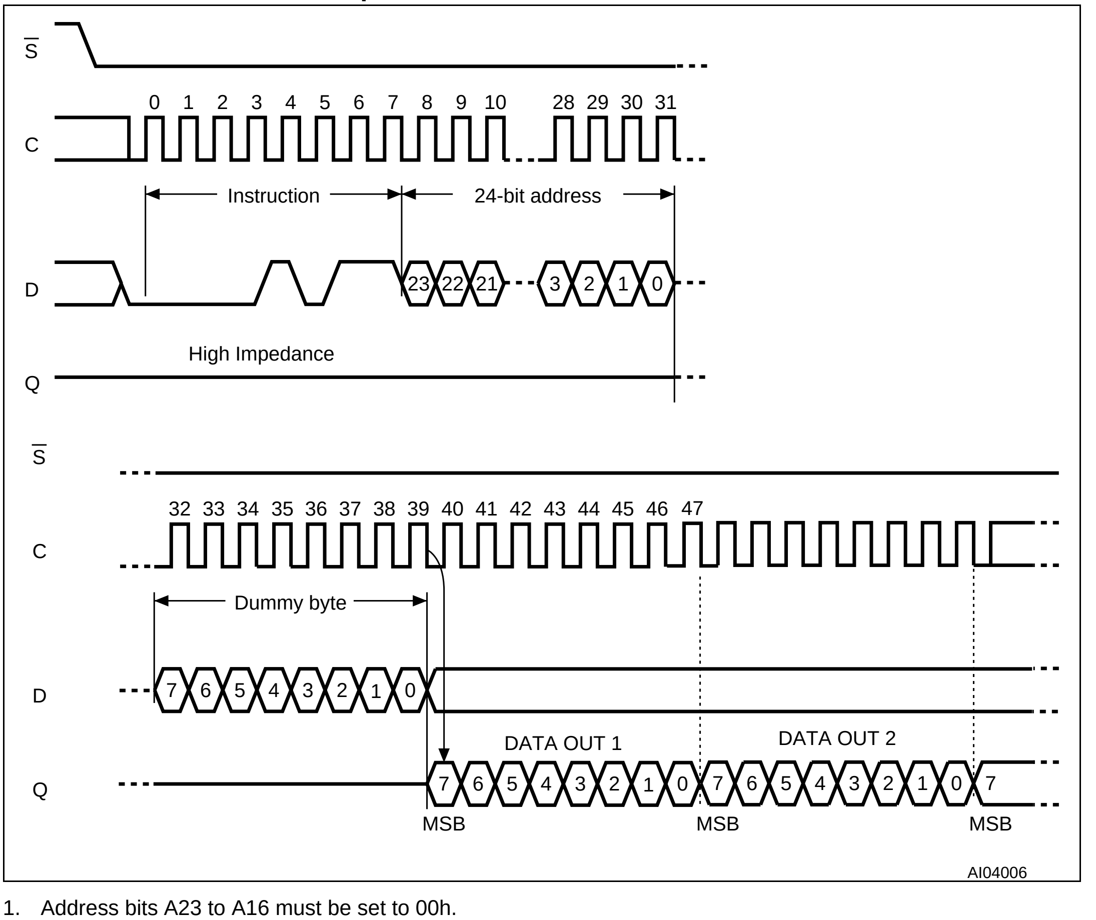
The instruction sequence is shown in *Figure 13.*

The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single read data bytes at higher speed (FAST_READ) instruction.

There is no address roll-over; when the highest address (0FFFFh) is reached, the instruction should be terminated.

The read data bytes at higher speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any read data bytes at higher speed (FAST_READ) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 13. Read data bytes at higher speed (FAST_READ) instruction sequence and data-out sequence



1. Address bits A23 to A16 must be set to 00h.

6.8 Page program (PP)

The page program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

The page program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (D). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 14.*

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

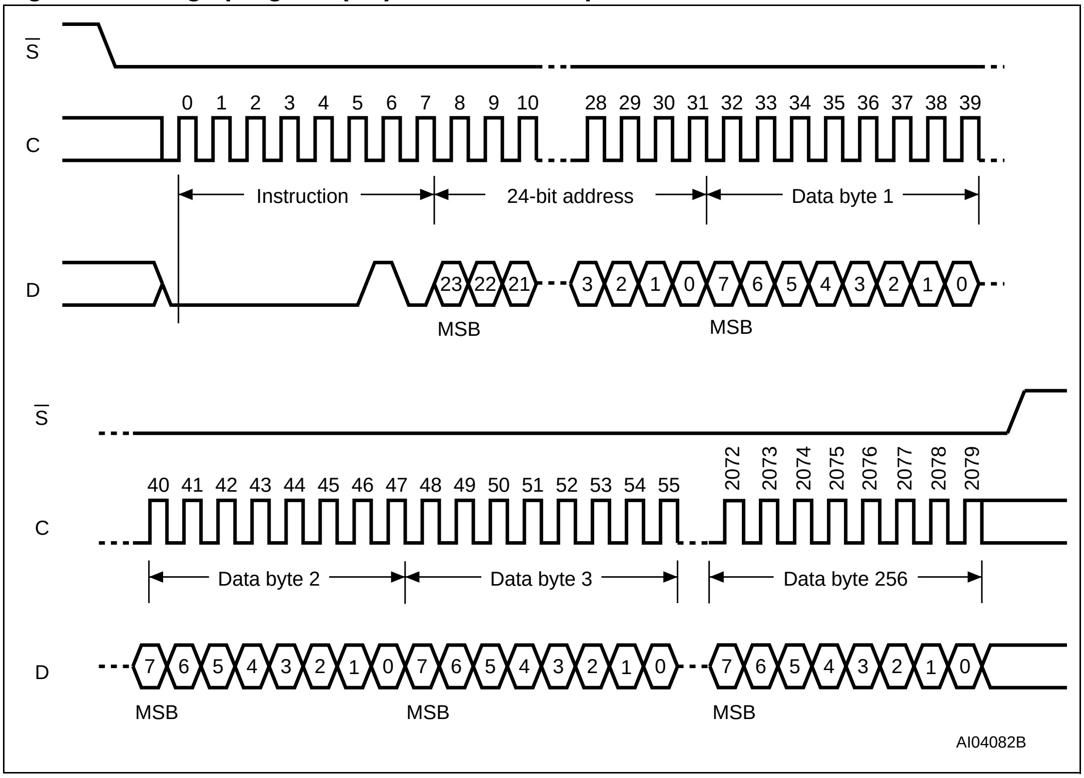
For optimized timings, it is recommended to use the page program (PP) instruction to program all consecutive targeted bytes in a single sequence versus using several page program (PP) sequences with each containing only a few bytes (see *Table 14: Instruction times*).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the page program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed page program cycle (whose duration is t_{PP}) is initiated. While the page program cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed page program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

A page program (PP) instruction applied to a page which is protected by the block protect (BP1, BP0) bits (see *Table 3.* and *Table 2.*) is not executed.

Figure 14. Page program (PP) instruction sequence



1. Address bits A23 to A16 must be set to 00h.

6.9 Sector erase (SE)

The sector erase (SE) instruction sets to '1' (FFh) all bits inside the chosen sector. Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

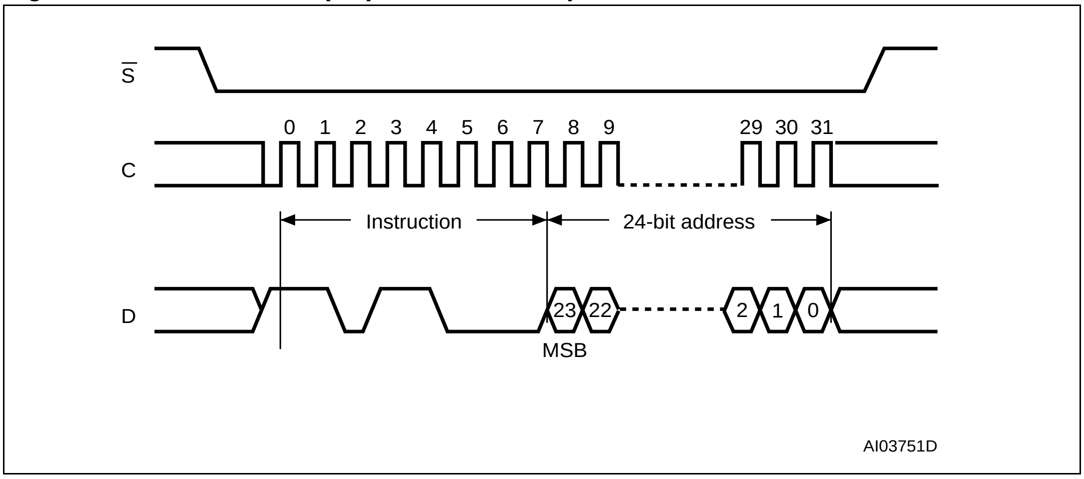
The sector erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, and three address bytes on Serial Data input (D). Any address inside the sector (see *Table 3*) is a valid address for the sector erase (SE) instruction. Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 15.*

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the sector erase (SE) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed sector erase cycle (whose duration is t_{SE}) is initiated. While the sector erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed sector erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

A sector erase (SE) instruction applied to a page which is protected by the block protect (BP1, BP0) bits (see *Table 3* and *Table 2*) is not executed.

Figure 15. Sector erase (SE) instruction sequence



1. Address bits A23 to A16 must be set to 00h.

6.10 Bulk erase (BE)

The bulk erase (BE) instruction sets all bits to ‘1’ (FFh). Before it can be accepted, a write enable (WREN) instruction must previously have been executed. After the write enable (WREN) instruction has been decoded, the device sets the write enable latch (WEL).

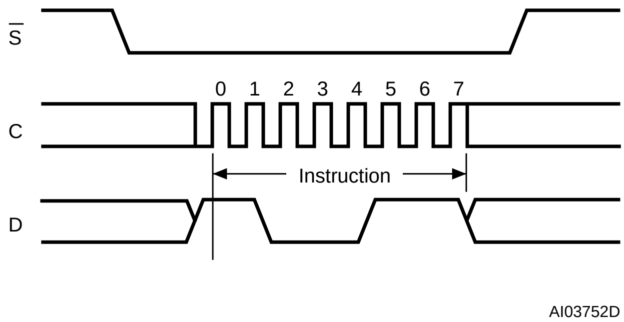
The bulk erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 16.*

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the bulk erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed bulk erase cycle (whose duration is t_{BE}) is initiated. While the bulk erase cycle is in progress, the status register may be read to check the value of the write in progress (WIP) bit. The write in progress (WIP) bit is 1 during the self-timed bulk erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the write enable latch (WEL) bit is reset.

The bulk erase (BE) instruction is executed only if both block protect (BP1, BP0) bits are 0. The bulk erase (BE) instruction is ignored if one, or more, sectors are protected.

Figure 16. Bulk erase (BE) instruction sequence



6.11 Deep power-down (DP)

Executing the deep power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the deep power-down mode). It can also be used as a software protection mechanism, while the device is not in active use, as in this mode, the device ignores all write, program and erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in standby mode (if there is no internal cycle currently in progress). But this mode is not the deep power-down mode. The deep power-down mode can only be entered by executing the deep power-down (DP) instruction, subsequently reducing the standby current (from I_{CC1} to I_{CC2}, as specified in *Table 13*).

To take the device out of deep power-down mode, the release from deep power-down and read electronic signature (RES) instruction must be issued. No other instruction must be issued while the device is in deep power-down mode.

The release from deep power-down and read electronic signature (RES) instruction, and the read identification (RDID) instruction also allow the electronic signature of the device to be output on Serial Data output (Q).

The deep power-down mode automatically stops at power-down, and the device always powers-up in the standby mode.

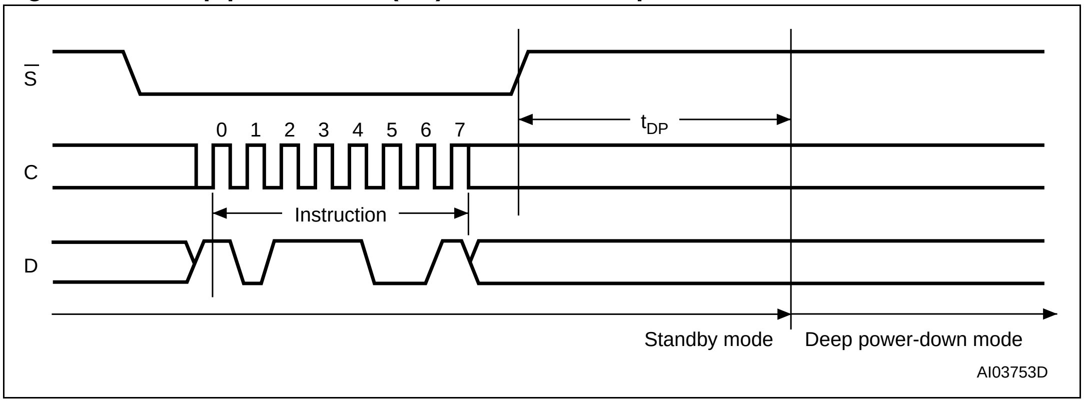
The deep power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data input (D). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in *Figure 17.*

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the deep power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the deep power-down mode is entered.

Any deep power-down (DP) instruction, while an erase, program or write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 17. Deep power-down (DP) instruction sequence



6.12 Release from deep power-down and read electronic signature (RES)

To take the device out of deep power-down mode, the release from deep power-down and read electronic signature (RES) instruction must be issued. No other instruction must be issued while the device is in deep power-down mode.

The instruction can also be used to read, on Serial Data output (Q), the 8-bit electronic signature, whose value for the M25P05-A is 05h.

Except while an erase, program or write status register cycle is in progress, the release from deep power-down and read electronic signature (RES) instruction always provides access to the 8-bit electronic signature of the device, and can be applied even if the deep power-down mode has not been entered.

Any release from deep power-down and read electronic signature (RES) instruction while an erase, program or write status register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data input (D) during the rising edge of Serial Clock (C). Then, the 8-bit electronic signature, stored in the memory, is shifted out on Serial Data output (Q), each bit being shifted out during the falling edge of Serial Clock (C).

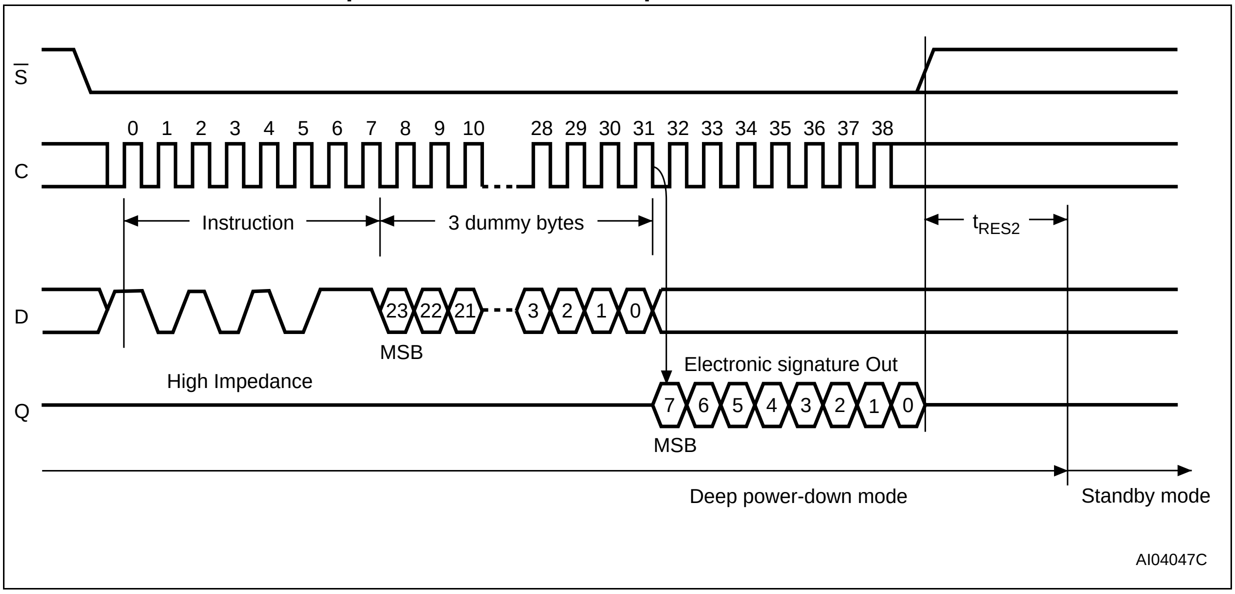
The instruction sequence is shown in *Figure 18.*

The release from deep power-down and read electronic signature (RES) instruction is terminated by driving Chip Select ($\overline{S}$) High after the electronic signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the electronic signature to be output repeatedly.

When Chip Select ($\overline{S}$) is driven High, the device is put in the standby power mode. If the device was not previously in the deep power-down mode, the transition to the standby power mode is immediate. If the device was previously in the deep power-down mode, though, the transition to the standby power mode is delayed by t_{RES2}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES2}(max), as specified in *Table 15.* Once in the standby power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

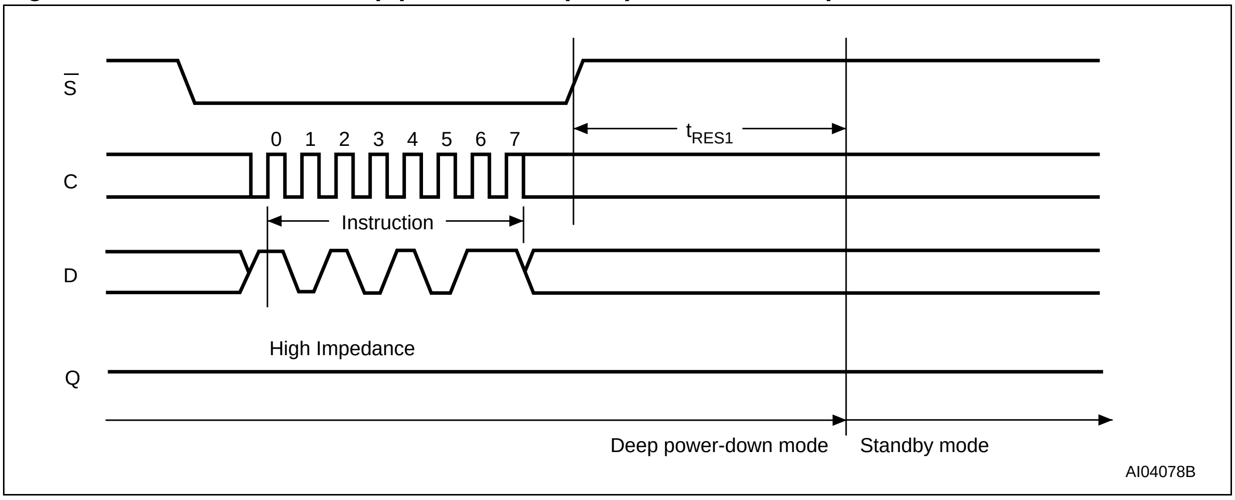
Driving Chip Select ($\overline{S}$) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit electronic signature has been transmitted for the first time (as shown in *Figure 19*), still ensures that the device is put into standby power mode. If the device was not previously in the deep power-down mode, the transition to the standby power mode is immediate. If the device was previously in the deep power-down mode, though, the transition to the standby power mode is delayed by t_{RES1}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES1}(max), as specified in *Table 15.* Once in the standby power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 18. Release from deep power-down and read electronic signature (RES) instruction sequence and data-out sequence



1. The value of the 8-bit electronic signature, for the M25P05-A, is 05h.

Figure 19. Release from deep power-down (RES) instruction sequence



7 Power-up and power-down

At power-up and power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC}(min) at power-up, and then for a further delay of t_{VSL}
- V_{SS} at power-down

A safe configuration is provided in *Section 3: SPI modes*.

To avoid data corruption and inadvertent write operations during power-up, a power on reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the power on reset (POR) threshold voltage, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all write enable (WREN), page program (PP), sector erase (SE), bulk erase (BE) and write status register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No write status register, program or erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the V_{WI} threshold
- t_{VSL} after V_{CC} passed the V_{CC}(min) level

These values are specified in *Table 8.*

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for read instructions even if the t_{PUW} delay is not yet fully elapsed.

At power-up, the device is in the following state:

- The device is in the standby mode (not the deep power-down mode)
- The write enable latch (WEL) bit is reset
- The write in progress (WIP) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} supply. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (generally, this capacitor is of the order of 100 nF).

At power-down, when V_{CC} drops from the operating voltage, to below the power on reset (POR) threshold voltage, V_{WI}, all operations are disabled and the device does not respond to any instruction (the designer needs to be aware that if a power-down occurs while a write, program or erase cycle is in progress, some data corruption can result).

Figure 20. Power-up timing

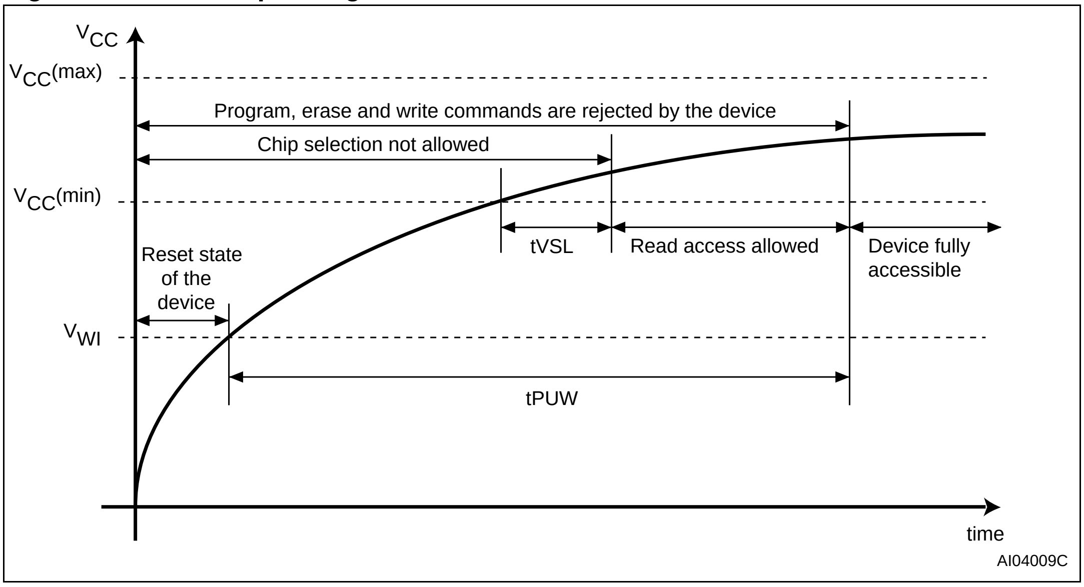


Table 8. Power-up timing and V_{WI} threshold

Symbol	Parameter	Min	Max	Unit
t_{VSL}(1)	V_{CC}(min) to $\overline{S}$ low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
V_{WI}(1)	Write inhibit voltage	1	2	V

1. These parameters are characterized only.

8 Initial delivery state

The device is delivered with the memory array erased: all bits are set to ‘1’ (each byte contains FFh). The status register contains 00h (all status register bits are 0).

9 Maximum ratings

Stressing the device above the rating listed in *Table 9: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering		see(1)	°C
V_{IO}	Input and output voltage (with respect to ground)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4.0	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–2000	2000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the Numonyx ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. JEDEC Std JESD22-A114A (C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω).

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 10. Operating conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage	2.3[1]	3.6	V
T_A	Ambient operating temperature	–40	85	°C

1. Only in products with process technology code Y. In products with process technology code X, V_{CC}(min) is 2.7 V.

Table 11. AC measurement conditions[1]

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		5	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output timing reference voltages	V_{CC} / 2		V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 21. AC measurement I/O waveform

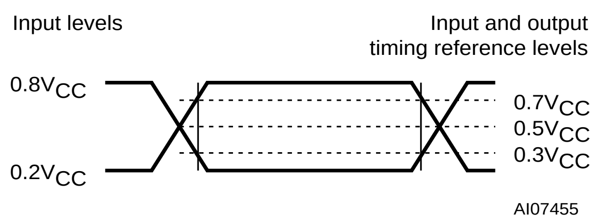


Table 12. Capacitance[1]

Symbol	Parameter	Test condition	Min	Max	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested, at T_A = 25 °C and a frequency of 25 MHz.

Table 13. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 10.*)	Min	Max	Unit
I_{LI}	Input leakage current			± 2	µA
I_{LO}	Output leakage current			± 2	µA
I_{CC1}	Standby current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		50	µA
I_{CC2}	Deep power-down current	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		5	µA
I_{CC3}	Operating current (READ)	C = 0.1V_{CC} / 0.9.V_{CC} at 50 MHz, Q = open		8	mA
		C = 0.1V_{CC} / 0.9.V_{CC} at 25 MHz, Q = open		4	mA
I_{CC4}	Operating current (PP)	$\overline{S} = V_{CC}$		15	mA
I_{CC5}	Operating current (WRSR)	$\overline{S} = V_{CC}$		15	mA
I_{CC6}	Operating current (SE)	$\overline{S} = V_{CC}$		15	mA
I_{CC7}	Operating current (BE)	$\overline{S} = V_{CC}$		15	mA
V_{IL}	Input low voltage		– 0.5	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC}–0.2		V

Table 14. Instruction times

Test conditions specified in *Table 10* and *Table 11.*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
t_W		Write status register cycle time		5	15	ms
t_{PP}(1)		Page program cycle time (256 bytes)		1.4	5	ms
		Page program cycle time (n bytes)		0.4+n*1/256(2)		
t_{SE}		Sector erase cycle time		0.65	3	s
t_{BE}		Bulk erase cycle time		0.85	6	s

1. When using the page program (PP) instruction to program consecutive bytes, optimized timings are obtained with one sequence including all the bytes versus several sequences of only a few bytes ($1 \leq n \leq 256$).
2. t_{PP}=2µs+8µs*[int(n-1)/2+1]+4µs*[int(n-1)/2]+2µs, only in products with process technology code X and Y.

Table 15. AC characteristics (25 MHz operation)

Test conditions specified in *Table 10* and *Table 11.*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		25	MHz
f_R		Clock frequency for read instructions	D.C.		20	MHz
t_{CH}[1]	t_{CLH}	Clock high time	18			ns
t_{CL}[1]	t_{CLL}	Clock low time	18			ns
t_{CLCH}[2]		Clock rise time[3] (peak to peak)	0.1			V/ns
t_{CHCL}[2]		Clock fall time[3] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	10			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	10			ns
t_{DVCH}	t_{DSU}	Data in setup time	5			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	10			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	10			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	100			ns
t_{SHQZ}[2]	t_{DIS}	Output disable time			15	ns
t_{CLQV}	t_V	Clock Low to Output Valid			15	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{HLCH}		$\overline{HOLD}$ setup time (relative to C)	10			ns
t_{CHHH}		$\overline{HOLD}$ hold time (relative to C)	10			ns
t_{HHCH}		$\overline{HOLD}$ setup time (relative to C)	10			ns
t_{CHHL}		$\overline{HOLD}$ hold time (relative to C)	10			ns
t_{HHQX}[2]	t_{LZ}	$\overline{HOLD}$ to Output Low-Z			15	ns
t_{HLQZ}[2]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			20	ns
t_{WHSL}[4]		Write protect setup time	20			ns
t_{SHWL}[4]		Write protect hold time	100			ns
t_{DP}[2]		$\overline{S}$ High to deep power-down mode			3	µs
t_{RES1}[2]		$\overline{S}$ High to standby mode without electronic signature read			3	µs
t_{RES2}[2]		$\overline{S}$ High to standby mode with electronic signature read			1.8	µs

1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/ f_C$.
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.

Table 16. AC characteristics (40 MHz operation)

40 MHz available for products marked since week 20 of 2004, only[1] Test conditions specified in *Table 10.* and *Table 11.*						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDSR, WRSR	D.C.		40	MHz
f_R		Clock frequency for read instructions	D.C.		20	MHz
t_{CH} [2]	t_{CLH}	Clock high time	11			ns
t_{CL} [2]	t_{CLL}	Clock low time	11			ns
t_{CLCH} [3]		Clock rise time[4] (peak to peak)	0.1			V/ns
t_{CHCL} [3]		Clock fall time[4] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	100			ns
t_{SHQZ} [3]	t_{DIS}	Output disable time			9	ns
t_{CLQV}	t_V	Clock Low to Output Valid			9	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{HLCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHL}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHQX} [3]	t_{LZ}	$\overline{HOLD}$ to Output Low-Z			9	ns
t_{HLQZ} [3]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			9	ns
t_{WHSL} [5]		Write protect setup time	20			ns
t_{SHWL} [1]		Write protect hold time	100			ns
t_{DP} [3]		$\overline{S}$ High to deep power-down mode			3	µs
t_{RES1} [3]		$\overline{S}$ High to standby mode without electronic signature read			3	µs
t_{RES2} [3]		$\overline{S}$ High to standby mode with electronic signature read			1.8	µs

1. Only applicable as a constraint for a WRSR instruction when SRWD is set to '1'.
2. t_{CH} + t_{CL} must be greater than or equal to 1/ f_C.
3. Value guaranteed by characterization, not 100% tested in production.
4. Expressed as a slew-rate.
5. Details of how to find the date of marking are given in application note, AN1995.

Table 17. AC characteristics (50 MHz operation)

50 MHz available only in products with process technology code Y(1)(2) Test conditions specified in Table 10 and Table 11.						
Symbol	**Alt.**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_C	f_C	Clock frequency(1) for the following instructions: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, RDID, RDSR, WRSR	D.C.		50	MHz
f_R		Clock frequency for read instructions	D.C.		25	MHz
t_{CH}(3)	t_{CLH}	Clock high time	9			ns
t_{CL}(3)	t_{CLL}	Clock low time	9			ns
t_{CLCH}(4)		Clock rise time(5) (peak to peak)	0.1			V/ns
t_{CHCL}(4)		Clock fall time(5) (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ active setup time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ not active hold time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data in setup time	2			ns
t_{CHDX}	t_{DH}	Data in hold time	5			ns
t_{CHSH}		$\overline{S}$ active hold time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ not active setup time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ deselect time	100			ns
t_{SHQZ}(4)	t_{DIS}	Output disable time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid			8	ns
t_{CLQX}	t_{HO}	Output hold time	0			ns
t_{HLCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHCH}		$\overline{HOLD}$ setup time (relative to C)	5			ns
t_{CHHL}		$\overline{HOLD}$ hold time (relative to C)	5			ns
t_{HHQX}(4)	t_{LZ}	$\overline{HOLD}$ to Output Low-Z			8	ns
t_{HLQZ}(4)	t_{HZ}	$\overline{HOLD}$ to Output High-Z			8	ns
t_{WHSL}(6)		Write protect setup time	20			ns
t_{SHWL}(6)		Write protect hold time	100			ns
t_{DP}(4)		$\overline{S}$ High to deep power-down mode			3	µs
t_{RES1}(4)		$\overline{S}$ High to standby mode without electronic signature read			30	µs
t_{RES2}(4)		$\overline{S}$ High to standby mode with electronic signature read			30	µs

1. Details of how to find the process on the device marking are given in application note AN1995.
2. 50 MHz operation is also available in products with process technology code X, but with a reduced supply voltage range (2.7 to 3.6 V).
3. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$.
4. Value guaranteed by characterization, not 100% tested in production.
5. Expressed as a slew-rate.
6. Only applicable as a constraint for a WRSR instruction when SRWD is set to ‘1’.

Figure 22. Serial input timing

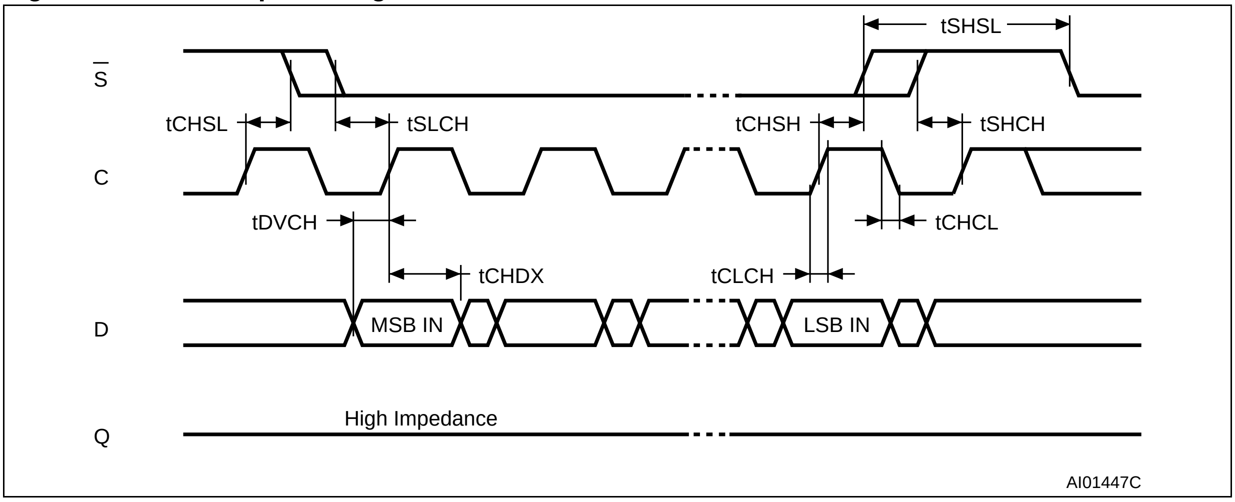


Figure 23. Write protect setup and hold timing during WRSR when SRWD =1

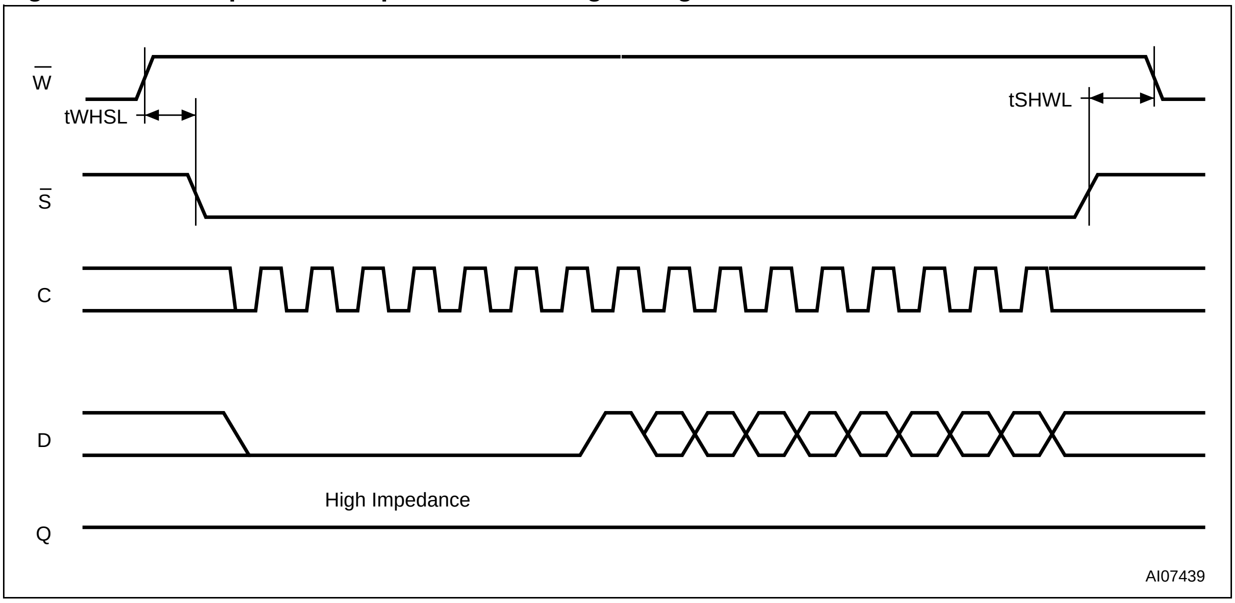


Figure 24. Hold timing

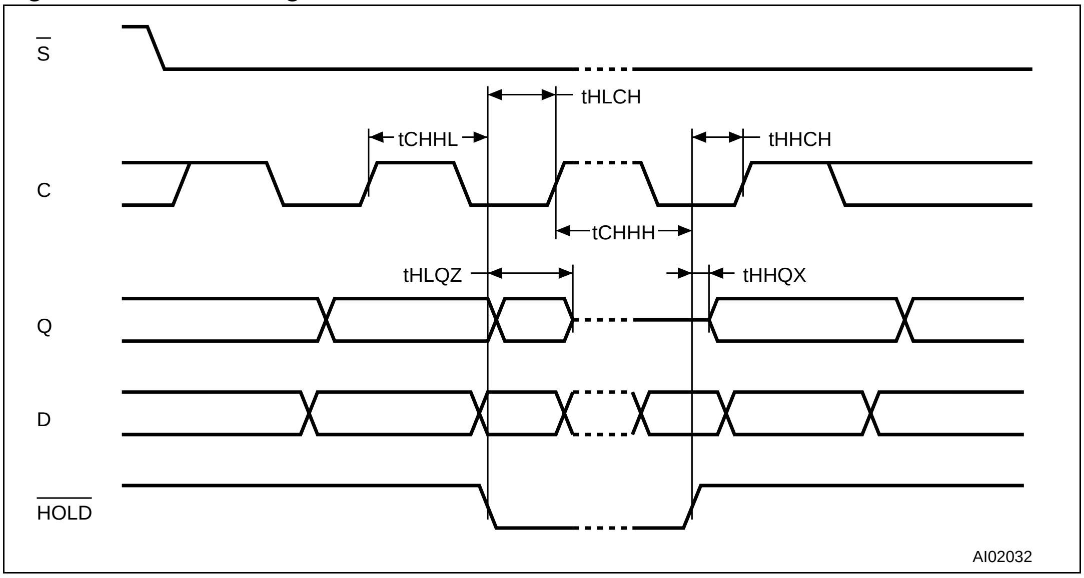
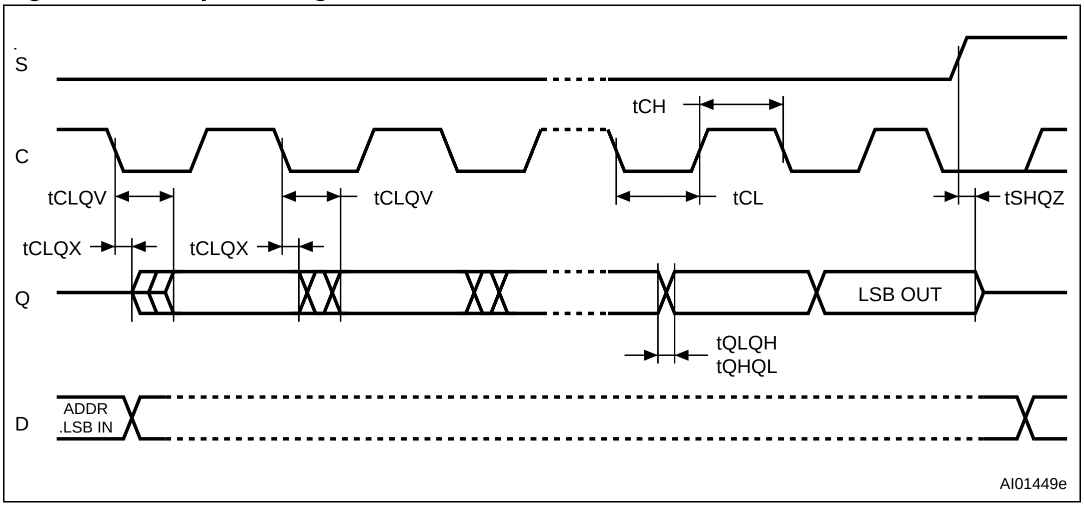


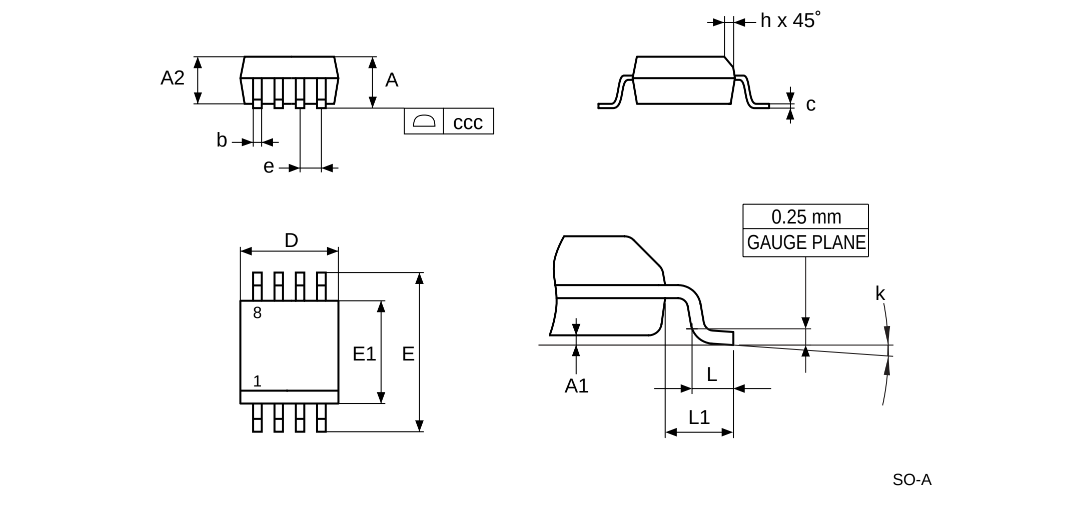
Figure 25. Output timing



11 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 26. SO8N – 8 lead plastic small outline, 150 mils body width, package outline

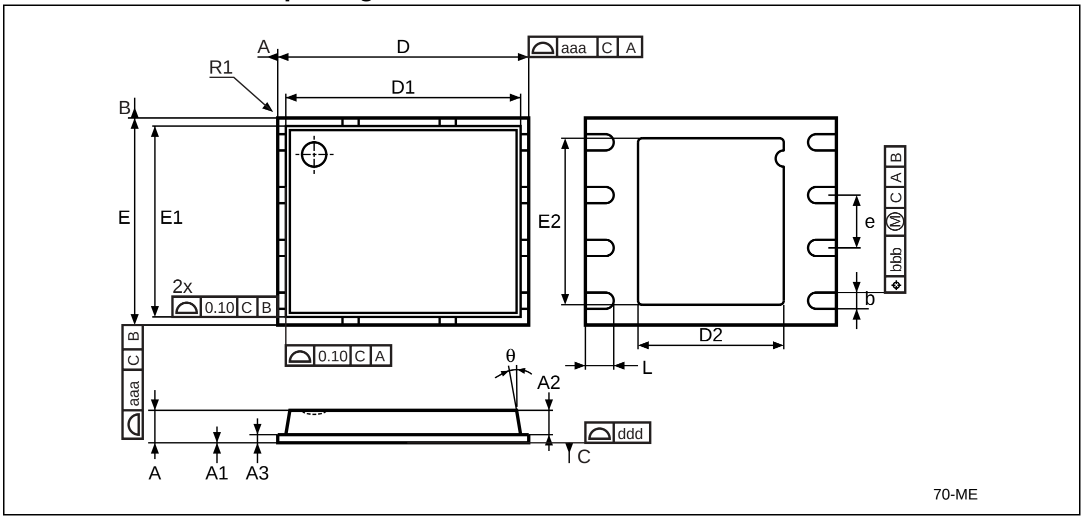


1. Drawing is not to scale.

Table 18. SO8N – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
b		0.28	0.48		0.011	0.019
c		0.17	0.23		0.007	0.009
ccc			0.10			0.004
D	4.90	4.80	5.00	0.193	0.189	0.197
E	6.00	5.80	6.20	0.236	0.228	0.244
E1	3.90	3.80	4.00	0.154	0.150	0.157
e	1.27	–	–	0.050	–	–
h		0.25	0.50		0.010	0.020
k		0°	8°		0°	8°
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		

Figure 27. VFQFPN8 (MLP8) - 8 lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package outline

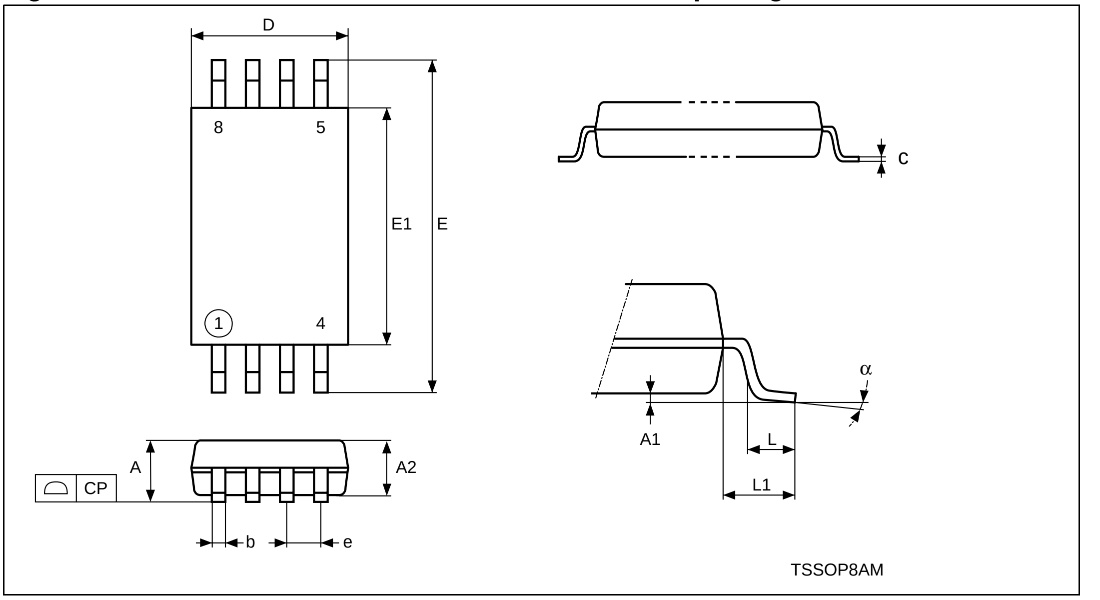


1. Drawing is not to scale.
2. The circle in the top view of the package indicates the position of pin 1.

Table 19. VFQFPN8 (MLP8) - 8 lead very thin fine pitch quad flat package no lead, 6 × 5 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.85	0.80	1.00	0.033	0.031	0.039
A1		0.00	0.05		0.000	0.002
A2	0.65			0.026		
A3	0.20			0.008		
b	0.40	0.35	0.48	0.016	0.014	0.019
D	6.00			0.236		
D1	5.75			0.226		
D2	3.40	3.20	3.60	0.134	0.126	0.142
E	5.00			0.197		
E1	4.75			0.187		
E2	4.00	3.80	4.30	0.157	0.150	0.169
e	1.27	–	–	0.050	–	–
R1	0.10	0.00		0.004	0.000	
L	0.60	0.50	0.75	0.024	0.020	0.029
Q			12°			12°
aaa			0.15			0.006
bbb			0.10			0.004
ddd			0.05			0.002

Figure 28. TSSOP8 – 8 lead thin shrink small outline, package outline

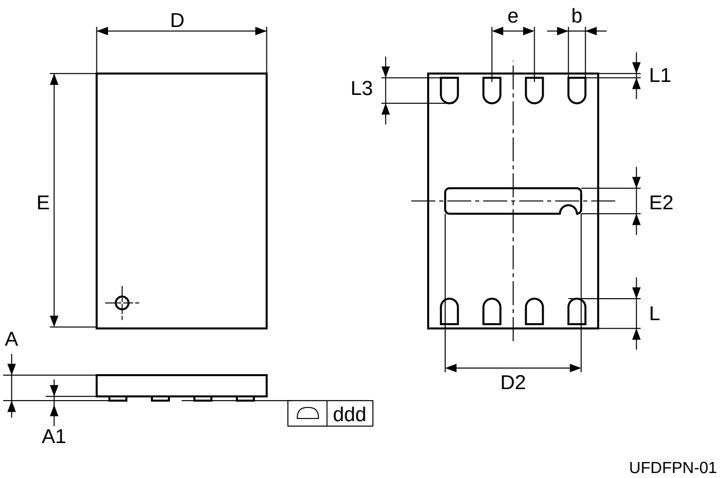


1. Drawing is not to scale.

Table 20. TSSOP8 – 8 lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2	1.00	0.80	1.05	0.039	0.031	0.041
b		0.19	0.30		0.007	0.012
c		0.09	0.20		0.003	0.008
CP			0.10			0.004
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65	–	–	0.026	–	–
E	6.40	6.20	6.60	0.252	0.244	0.260
E1	4.40	4.30	4.50	0.173	0.169	0.177
L	0.60	0.45	0.75	0.024	0.018	0.029
L1	1.00			0.039		
α		0°	8°		0°	8°
N	8			8		

Figure 29. UFDFPN8 (MLP8) – 8 lead ultra thin fine pitch dual flat package no lead, 2 x 3 mm package outline



1. Drawing is not to scale.

Table 21. UFDFPN8 (MLP8) – 8 lead ultra thin fine pitch dual flat package no lead, 2 x 3 mm package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.45	0.60	0.022	0.018	0.024
A1	0.02	0.00	0.05	0.001	0.000	0.002
b(1)	0.25	0.20	0.30	0.010	0.008	0.012
D	2.00	1.90	2.10	0.079	0.075	0.083
D2	1.60	1.50	1.70	0.063	0.059	0.067
ddd(2)			0.08			0.003
E	3.00	2.90	3.10	0.118	0.114	0.122
E2	0.20	0.10	0.30	0.008	0.004	0.012
e	0.50	–	–	0.020	–	–
L	0.45	0.40	0.50	0.018	0.016	0.020
L1			0.15			0.006
L3		0.30			0.012	

1. Dimension b applies to plated terminal and is measured between 0.15 and 0.30 mm from the terminal tip.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

12 Ordering information

Table 22. Ordering information scheme

Example: M25P05-A V MN 6 T P

Device type

M25P

Device function

05-A = 512 Kbits (64 Kbit x8)

Operating voltage

V = V_{CC} = 2.3 to 3.6 V

Package

MN = SO8 (150 mil width)

MP = VFQFPN8 (MLP8)

DW = TSSOP8(1)

MB = UFDFPN8 (MLP8)

Temperature range

6 = –40 to 85 °C

Option

blank = standard packing

T = tape & reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

1. The TSSOP8 package is available in products with process technology code X and Y (details of how to find the process on the device marking are given in application note AN1995).

Note: For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Numonyx sales office.

13 Revision history

Table 23. Document revision history

Date	Revision	Changes
25-Feb-2001	1.0	Initial release.
11-Apr-2002	1.1	Clarification of descriptions of entering Standby Power mode from Deep Power-down mode, and of terminating an instruction sequence or data-out sequence.
12-Sep-2002	1.2	VFQFPN8 package (MLP8) added.
13-Dec-2002	1.3	Typical Page Program time improved. Write Protect setup and hold times specified, for applications that switch Write Protect to exit the Hardware Protection mode immediately before a WRSR, and to enter the Hardware Protection mode again immediately after.
24-Nov-2003	2	Table of contents, warning about exposed paddle on MLP8, and Pb-free options added. 40 MHz AC characteristics table included as well as 25 MHz. I_{CC3}(max), t_{SE}(typ) and t_{BE}(typ) values improved. Change of naming for VDFPN8 package
13-Jan-2005	3	Devices with process technology code X added (*Read identification (RDID)* and *Table 17: AC characteristics (50 MHz operation)*) added. TSSOP8 package added. Notes 1 and 2 removed from *Table 22: Ordering information scheme* and Note 1 added. Note 1 to *Table 9: Absolute maximum ratings* changed, note 2 and T_{LEAD} values removed. Small text changes.
01-Apr-2005	4	Frequency test condition modified for I_{CC3} in *Table 13: DC characteristics*. *Read identification (RDID)*, *Deep power-down (DP)* and *Release from deep power-down and read electronic signature (RES)* instructions and *Active power, standby power and deep power-down modes* paragraph clarified. SO8 package specifications updated (see *Figure 26.* and *Table 18*).
01-Aug-2005	5	Updated Page Program (PP) instructions in *Page programming*, *Page program (PP)* and *Instruction times*.
06-Jul-2006	6	Packages are fully ECOPACK® compliant. SO8N and VFQFPN8 package specifications updated (see *Section 11: Package mechanical*). *Figure 3: Bus master and memory devices on the SPI bus* updated and *Note 2* added. T_{LEAD} removed from *Section Table 9.: Absolute maximum ratings*. Small text changes.
19-Dec-2006	7	*VCC supply voltage* and *VSS ground* descriptions added. *Figure 3: Bus master and memory devices on the SPI bus* updated, note 2 removed replaced by explanatory paragraph. WIP bit behavior at power-up specified in *Section 7: Power-up and power-down*. T_{LEAD} added and V_{IO} max modified in *Table 9: Absolute maximum ratings*. VFQFPN8 and SO8N packages updated (see *Section 11: Package mechanical*).

Table 23. Document revision history (continued)

Date	Revision	Changes
07-Aug-2007	8	Removed ‘low voltage’ from the title. Small text changes. Changed note below *Table 12: Capacitance*. Changed the minimum value for V_{CC} (from 2.7 to 2.3 V). UFDFPN8 package (MLP8) added. Frequency test condition modified for I_{CC3} in *Table 13: DC characteristics*. t_{SE}(typ), t_{BE}(typ) and t_{PP}(typ) values improved in *Table 14: Instruction times*. Changed maximum value for f_R in *Table 17: AC characteristics (50 MHz operation)*.
10-Oct-2007	9	Added the reference to a new process technology (code Y).
10-Dec-2007	10	Applied Numonyx branding.
18-Apr-2008	11	Updated *Table 3: Bus master and memory devices on the SPI bus*. Modified the code for UFDFPN8 package from ‘ZW’ to ‘MB’. Minor text changes.

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