CM1442-06LP

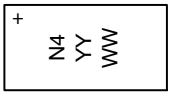
LCD and Camera EMI Filter Array with ESD Protection

ON Semiconductor®

http://onsemi.com

WLCSP15
LP SUFFIX
CASE 567CM

MARKING DIAGRAM



CM1442−06LP
15−Bump CSP Package

N4 = CM1442−06LP
YYWW = Datecode

ORDERING INFORMATION

Device	Package	Shipping†
CM1442−06LP	CSP−15 (Pb−Free)	3500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Functional Description

The CM1442-06LP is part of a family of pi-style EMI filter arrays with ESD protection, which integrates six filters (C-R-C) in a Chip Scale Package (CSP) form factor with 0.40 mm pitch. The CM1442-06LP (low profile) has component values of 15 pF – 100 Ω – 15 pF per channel. The CM1442-06LP has a cut-off frequency of 120 MHz and can be used in applications where the data rates are as high as 48 Mbps. The parts include avalanche-type ESD diodes on every pin, which provide a very high level of protection for sensitive electronic components against potential electrostatic discharge (ESD). The ESD protection diodes safely dissipate ESD strikes of ±15 kV, well beyond the maximum requirement of the IEC61000-4-2 international standard. Using the MIL-STD-883 (Method 3015) specification for Human Body Model (HBM) ESD, the pins are protected for contact discharges at greater than ±30 kV.

The CM1442-06LP is available in a space-saving, low-profile CSP with RoHS-compliant, lead-free finishing. It is manufactured with a 0.40 mm pitch and 0.15 mm CSP solder ball to provide up to 28% board space saving versus competing CSP devices with 0.50 mm pitch and 0.30 mm CSP solder ball.

Features

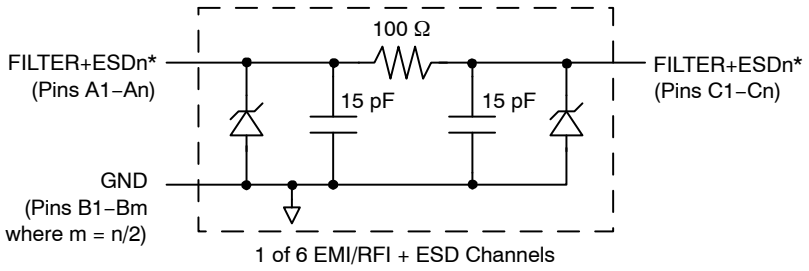
- Six Channels of EMI Filtering with Integrated ESD Protection
- 0.4 mm Pitch, 15−Bump, 2.360 mm x 1.053 mm Footprint Chip Scale Package (CSP)
- Pi−Style EMI Filters in a Capacitor−Resistor−Capacitor (C−R−C) Network
- ±15 kV ESD Protection on Each Channel (IEC 61000−4−2 Level 4, Contact Discharge)
- ±30 kV ESD Protection on Each Channel (HBM)
- Greater than 30 dB Attenuation (Typical) at 1 GHz
- These Devices are Pb−Free and are RoHS Compliant

Applications

- LCD and Camera Data Lines in Mobile Handsets
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
- EMI Filtering for Data Ports in Cell Phones, PDAs or Notebook Computers
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules

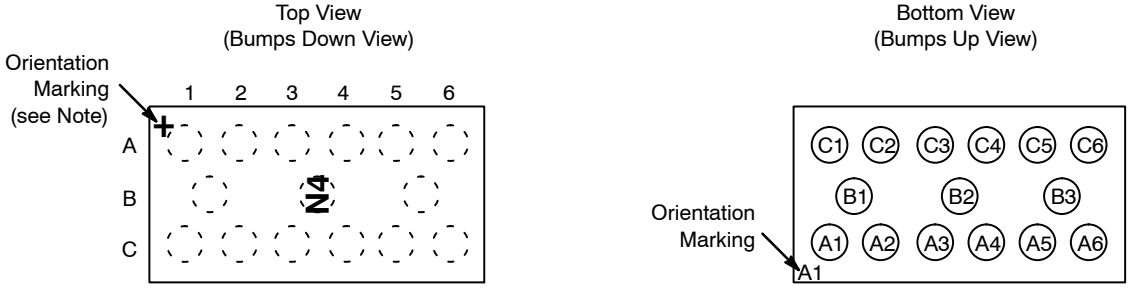
Publication Order Number:
CM1442−06LP/D

BLOCK DIAGRAM



*See Package/Pinout Diagrams for expanded pin information.

PACKAGE / PINOUT DIAGRAMS



CM1442−06LP
15−Bump CSP Package

Table 1. PIN DESCRIPTIONS

Pins	Name	Description	Pins	Name	Description
A1	FILTER1	Filter + ESD Channel 1	C1	FILTER1	Filter + ESD Channel 1
A2	FILTER2	Filter + ESD Channel 2	C2	FILTER2	Filter + ESD Channel 2
A3	FILTER3	Filter + ESD Channel 3	C3	FILTER3	Filter + ESD Channel 3
A4	FILTER4	Filter + ESD Channel 4	C4	FILTER4	Filter + ESD Channel 4
A5	FILTER5	Filter + ESD Channel 5	C5	FILTER5	Filter + ESD Channel 5
A6	FILTER6	Filter + ESD Channel 6	C6	FILTER6	Filter + ESD Channel 6
B1−B3	GND	Device Ground			

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	−65 to +150	°C
DC Power per Resistor	100	mW
DC Package Power Rating	500	mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	−40 to +85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R	Resistance		80	100	120	Ω
C_{TOTAL}	Total Channel Capacitance	At 2.5 VDC Reverse Bias, 1 MHz, 30 mVAC	24	30	36	pF
C	Capacitance C1	At 2.5 VDC Reverse Bias, 1 MHz, 30 mVAC	12	15	18	pF
V_{DIODE}	Standoff Voltage	I_{DIODE} = 10 μA		6.0		V
I_{LEAK}	Diode Leakage Current (reverse bias)	V_{DIODE} = +3.3 V		0.1	1	μA
V_{SIG}	Signal Clamp Voltage Positive Clamp Negative Clamp	 I_{LOAD} = 10 mA I_{LOAD} = −10 mA	 5.6 −1.5	 6.8 −0.8	 9.0 −0.4	V
V_{ESD}	In−system ESD Withstand Voltage a) Human Body Model, MIL−STD−883, Method 3015 b) Contact Discharge per IEC 61000−4−2 Level 4	(Notes 2 and 3)	 ±30 ±15			kV
R_{DYN}	Dynamic Resistance Positive Negative			 2.3 0.9		Ω
f_C	Cut−off Frequency Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω	R = 100 Ω, C = 15 pF		 115		MHz

1. T_A = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.
3. Unused pins are left open.

PERFORMANCE INFORMATION

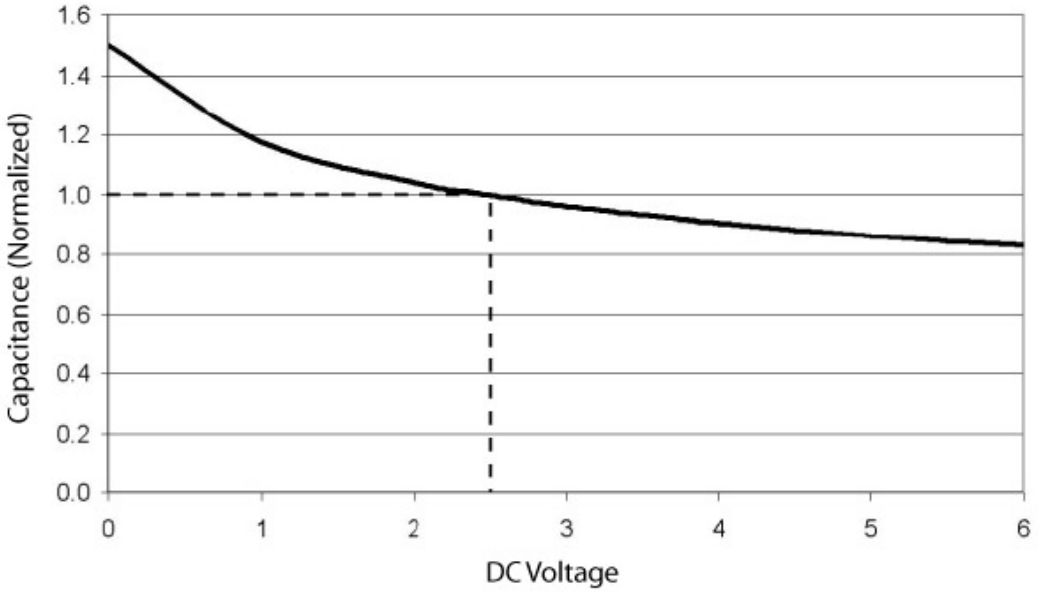


Figure 1. Filter Capacitance vs. Input Voltage (normalized to capacitance at 2.5 VDC and 25°C)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

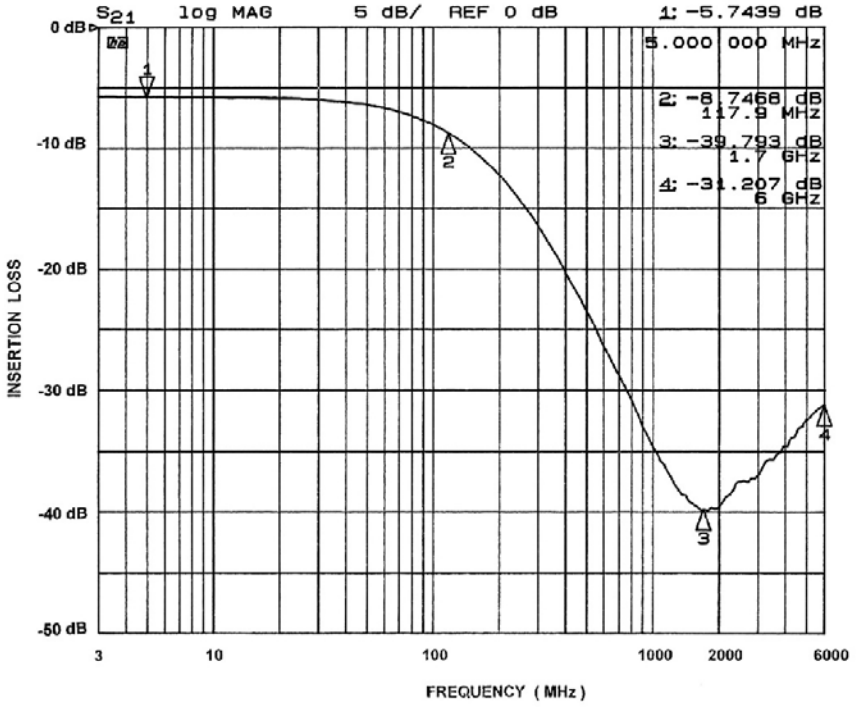


Figure 2. Insertion Loss vs. Frequency (A1−C1 to GND B1)

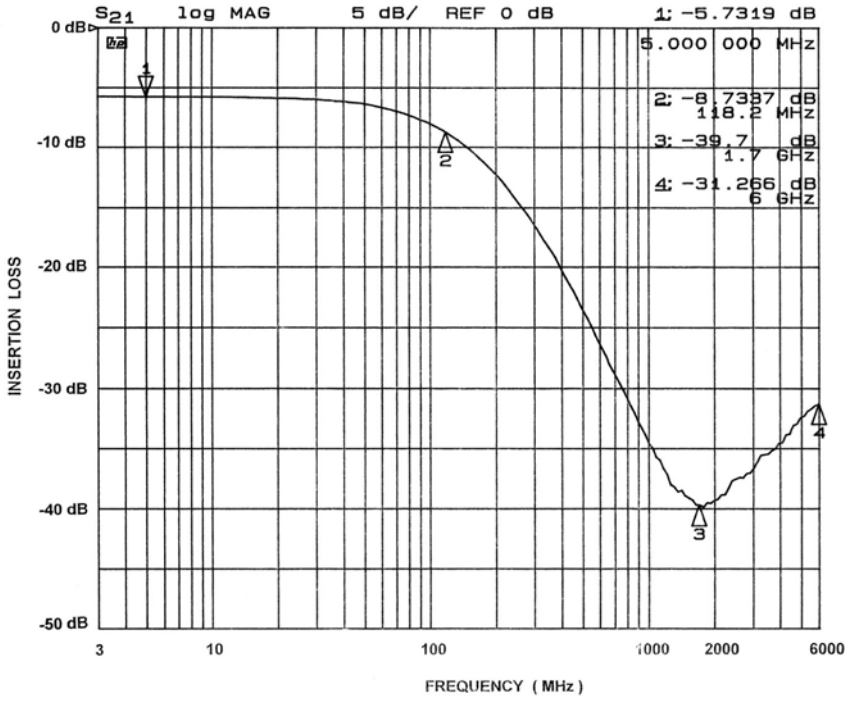


Figure 3. Insertion Loss vs. Frequency (A2−C2 to GND B1)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

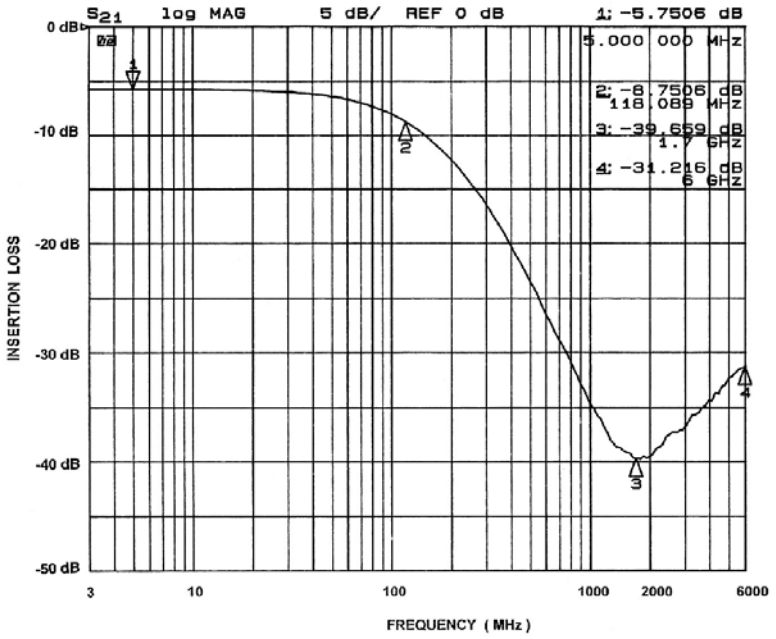


Figure 4. Insertion Loss vs. Frequency (A3−C3 to GND B2)

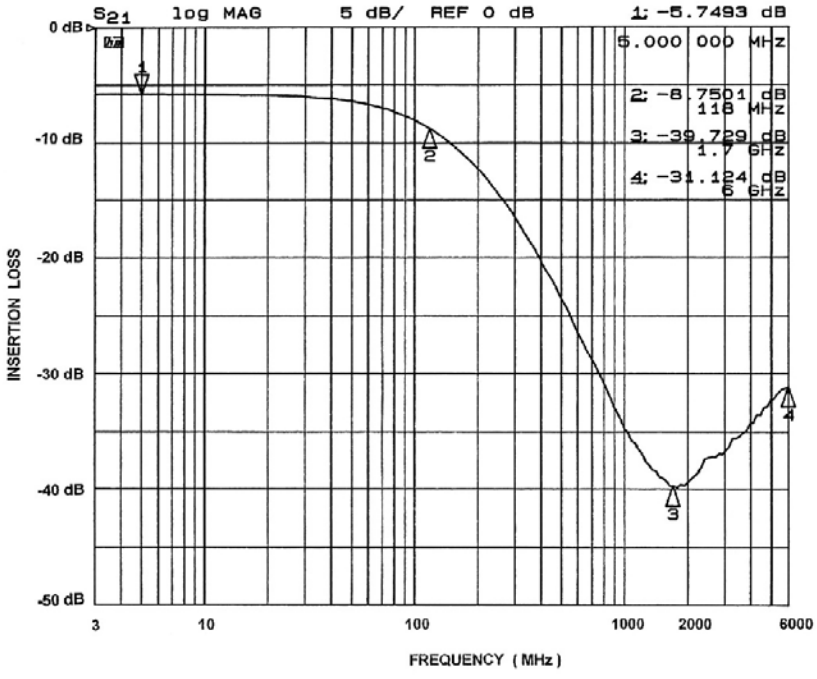


Figure 5. Insertion Loss vs. Frequency (A4−C4 to GND B2)

PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance (T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

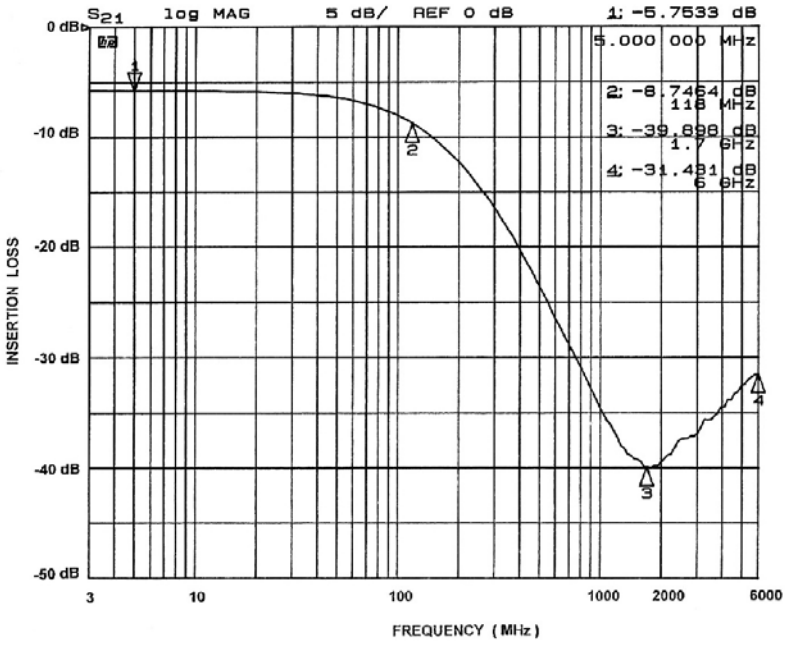


Figure 6. Insertion Loss vs. Frequency (A5−C5 to GND B3)

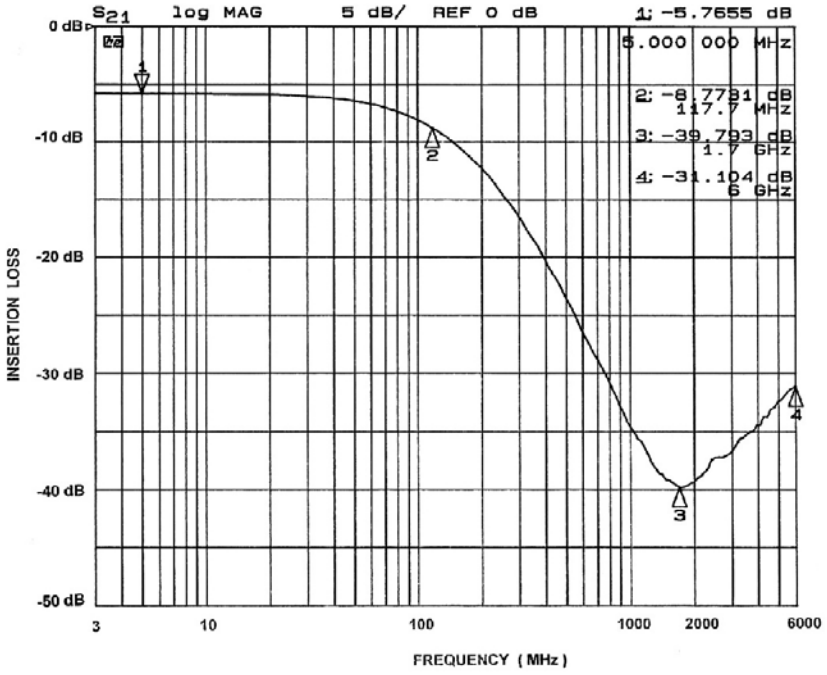


Figure 7. Insertion Loss vs. Frequency (A6−C6 to GND B3)

APPLICATION INFORMATION

Table 5. PRINTED CIRCUIT BOARD RECOMMENDATIONS

Parameter	Value
Pad Size on PCB	0.240 mm
Pad Shape	Round
Pad Definition	Non−Solder Mask defined pads
Solder Mask Opening	0.290 mm Round
Solder Stencil Thickness	0.125 − 0.150 mm
Solder Stencil Aperture Opening (laser cut, 5% tapered walls)	0.300 mm Round
Solder Flux Ratio	50/50 by volume
Solder Paste Type	No Clean
Pad Protective Finish	OSP (Entek Cu Plus 106A)
Tolerance − Edge To Corner Ball	±50 μm
Solder Ball Side Coplanarity	±20 μm
Maximum Dwell Time Above Liquidous	60 seconds
Maximum Soldering Temperature for Lead−free Devices using a Lead−free Solder Paste	260°C

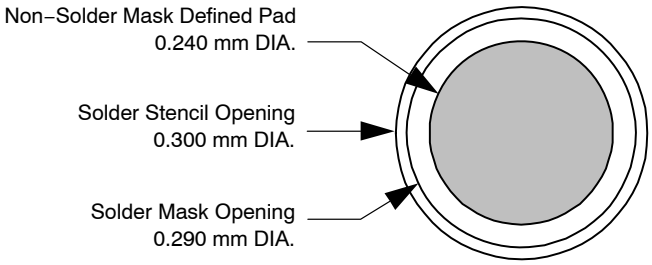


Figure 8. Recommended Non−Solder Mask Defined Pad Illustration

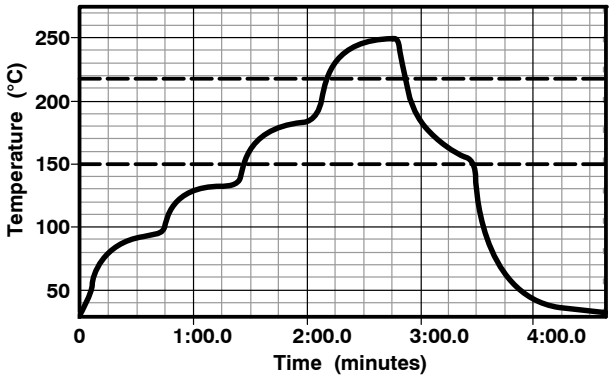
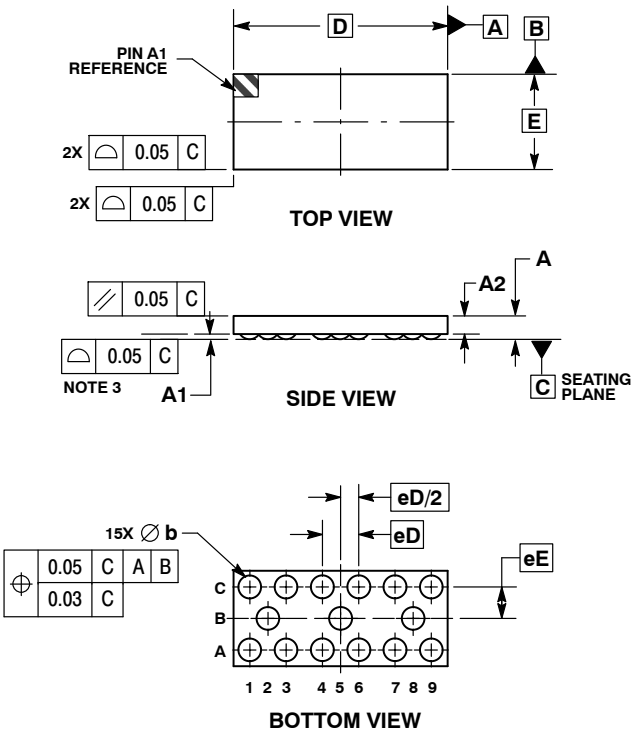


Figure 9. Lead−free (SnAgCu) Solder Ball Reflow Profile

PACKAGE DIMENSIONS

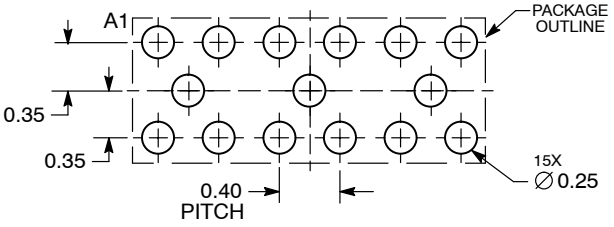
WLCSP15, 2.36x1.05
CASE 567CM−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.22	0.30
A1	0.04	0.12
A2	0.20 REF	
b	0.23	0.28
D	2.36 BSC	
E	1.05 BSC	
eD	0.400 BSC	
eE	0.347 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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