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FPM21500QFN

LOW-NOISE HIGH-LINEARITY BALANCED AMPLIFIER MODULE

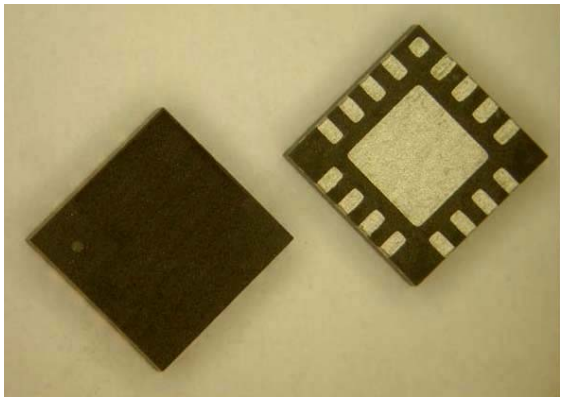
Package: 4mmx4mm QFN

Product Description

The FPM21500QFN is a packaged pair of transistors (pHEMT) specifically optimized for balanced configuration systems. Our 0.25µm process ensures class-leading noise performance. The use of a small footprint plastic package allows for a cost effective total system implementation.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



Features

- Balanced Low Noise Amplifier Module
- Excellent Noise figure: 0.45dB at 900MHz
- Combined IP3: 38dBm (100mA)
- Combined P1dB: 29dBm (100mA)
- Small footprint: 4mm x 4mm x 0.9mm QFN
- RoHS Compliant: (Directive 2002/95/EC)

Applications

- Wireless Infrastructure: Tower-Mounted Amplifiers and Front End LNAs for EGSM/PCS/WCDMA/UMTS Base Stationx
- High Intercept-Point LNAs

RF Parameter	Typical Performance			Unit	Condition
	0.9GHz	1.85GHz	2.6GHz		
OP_{1dB} at Gain Compression	28	29	29	dBm	V_{DS}=4V, I_{DS}=100mA
Small-Signal Gain (SSG)	18	16.5	14	dB	V_{DS}=4V, I_{DS}=100mA
PAE	50	45	45	%	V_{DS}=4V, I_{DS}=100mA, P_{OUT}=P_{1dB}
Maximum Stable Gain (|S21/S12|)	24	20	18	dB	V_{DS}=4V, I_{DS}=100mA
Noise Figure (NF)	0.55	0.65	0.7	dB	V_{DS}=4V, I_{DS}=100mA
	0.45			dB	V_{DS}=3V, I_{DS}=70mA
OIP_3 (15dB to 5dB below P_{1dB})	37	38	38	dBm	V_{DS}=4V, I_{DS}=100mA
	34	38	38	dBm	V_{DS}=3V, I_{DS}=70mA, POUT=12dBm per tone

*Note: Based on measured data taken on applications circuits. $T_{AMBIENT}$=22°C.

RF/DC Parameter	Electrical Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency		2.0		GHz	
OP_{1dB} at Gain Compression	25	26		dBm	V_{DS}=4.5V, I_{DS}=120mA
Small-Signal Gain (SSG)	14	15		dB	V_{DS}=4.5V, I_{DS}=120mA
Saturated Drain-Source Current (I_{DSS})	375	465	550	mA	V_{DS}=1.3V, V_{GS}=0V
Transconductance (GM)		400		ms	V_{DS}=1.3V, V_{GS}=0V
Pinch-Off Voltage (V_P)	|0.7|	|1.0|	|1.3|	V	V_{DS}=1.3V, I_{DS}=1.5mA
Gate-Source Breakdown Vltg (V_{BDGS})	|12|	|16|		V	I_{GS}=1.5mA
Gate-Drain Breakdown Vltg (V_{BDGD})	|12|	|18|		V	I_{DS}=1.5mA
Thermal Resistivity (θJC) *		60		°C/W	1W dissipation, case temperature 22°C

*Note: All devices are 100% RF and DC tested at 2.0GHz (unmatched into 50Ω). $T_{AMBIENT}$=22°C.

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Absolute Maximum Ratings[1]

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS})	6	V
Gate-Source Voltage (V_{GS})	-3	V
Drain-Source Current (I_{DS}) (V_{DS}<2V)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	15	mA
RF Input Power (P_{IN})[2] (Under any acceptable bias state)	350	mW
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-55 to 150	°C
Total Power Dissipation (P_{TOT})[3, 4, 5]	2.2	W
Gain Compression (Under bias conditions)	5	dB

Notes: [1]$T_{AMBIENT}$=22 °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2]Max. RF input limit must be further limited if input VSWR>2.5:1.
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously.
[4]Total Power Dissipation (P_{TOT}) defined as (P_{DC}+P_{IN})−P_{OUT}, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
Total Power Dissipation to be de-rated as follows above 22 °C:
P_{TOT}=(150-T_{CASE})/θJC, where T_{CASE}=temperature of the thermal pad on the underside of the package.
θJC increases linearly from 60 °C/W at a T_{CASE} of 22 °C to 81 °C/W at a T_{CASE} of 145 °C. (Coefficient of de-rating formula is Thermal Conductivity.)
Information on the mounting of QFN-style packages for optimum thermal performance is available on request.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

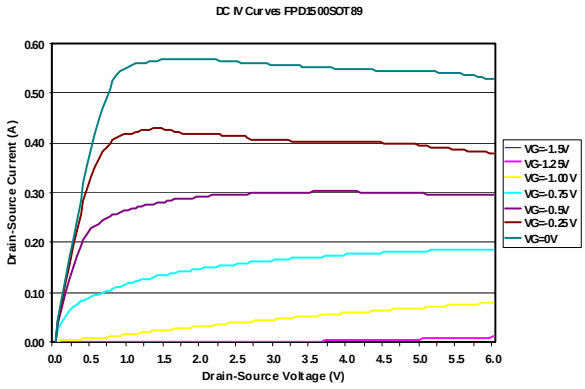
Biasing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-biased or dual-biased circuits. Such circuits should include provisions to ensure that gate bias is applied before drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices used in the FPM21500QFN.

For standard Class A operation, a 50% I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Class A/B bias of 25% to 33% offers an optimized solution for NF and OIP_3.

Typical I-V Characteristics



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the Drain-Source voltage (V_{DS}) to 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented here). Setting the V_{DS}>1.3V will generally cause errors in the current measurements, even in stabilized circuits.

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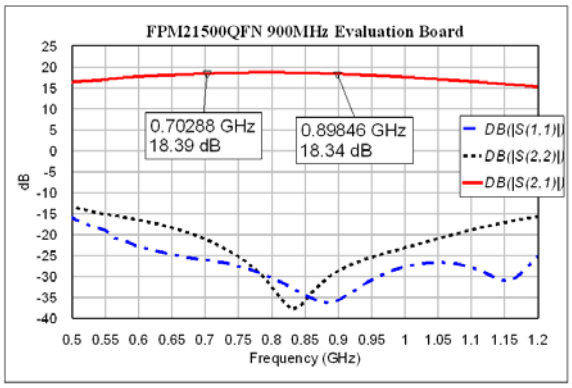
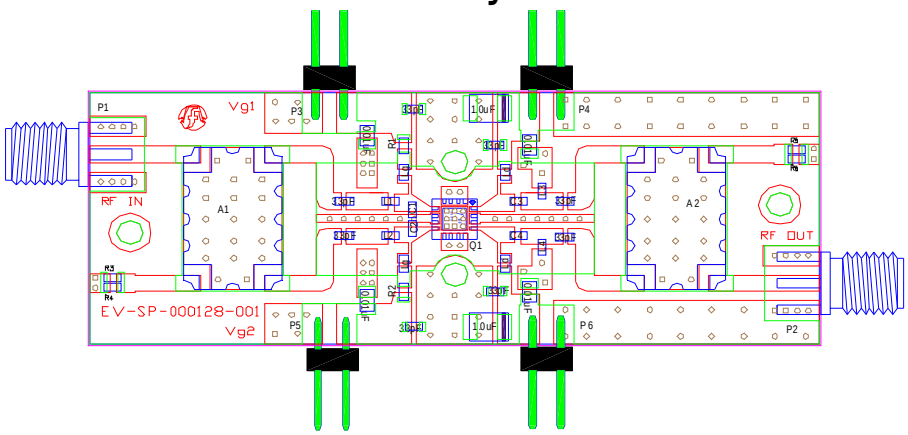
Reference Design (700MHz to 950MHz)



Parameter	Typ.	Unit
Frequency	900	MHz
Gain	18	dB
P_{1dB}	23	dBm
OIP_3	34	dBm
NF	0.45	dB
S11	-35	dB
S22	-28	dB
V_D	3	V
V_G	-0.4 to -0.6	V
I_D	70	mA

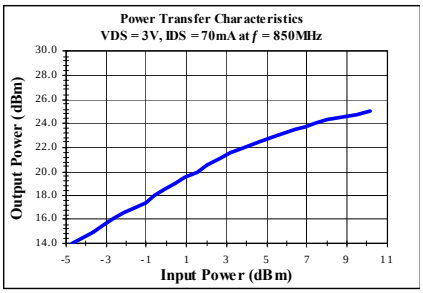
Note: OIP_3 measured at P_{OUT} of 12dBm per tone.

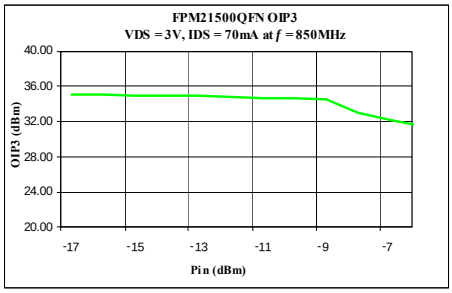
Board Layout

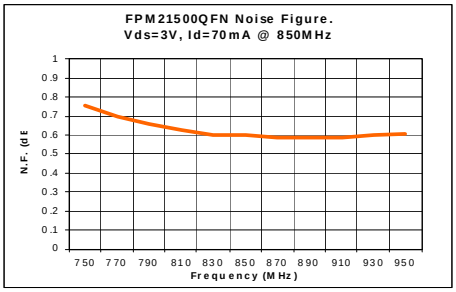


Comp:	Description
C1&C2	Cap, 0603 0.5pF ATC 600S
C3&C4	Cap, 0603 2.7pF ATC 600S
33pF x 8	Cap, 0603 ATC 600S
.01uF x 4	Cap, 0805 ATC805X103KL2AT
1.0uF x 2	SMD-B Tantallum x 2
L1 & L2	Inductor LL1005-FH 8.2nH TOKO
L3 & L4	Inductor LL1005-FH 10nH TOKO
Lg & Ld	Inductor LL1608-FH 56nH TOKO
Q1	FPM2150DQFN
R1, R2	20 Ohm 0603 size Chip Resistor
R3,R4,R5,R6	100 Ohm 0603 size CHip Resistor x 4
A1 & A2	Anaren XC0900A-03 Hybrid Coupler (900MHz)
P1 & P2	Edge mount RF Connector (Radial) R125.423.200
P3, P4, P5, P6	2-Pin Header.

Typical Performance at 850MHz







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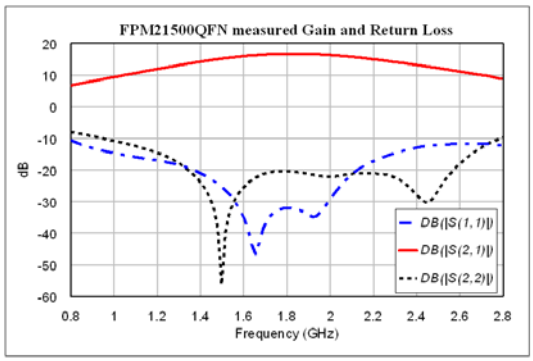
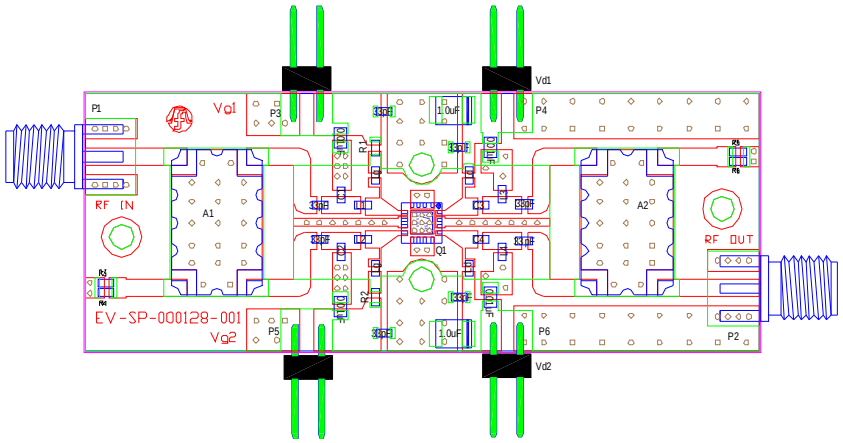
Reference Design (1700MHz to 2000MHz)



Parameter	Typ.	Unit
Frequency	1850	MHz
Gain	16.5	dB
P_{1dB}	29	dBm
OIP_3	38	dBm
NF	0.65	dB
S11	-30	dB
S22	-20	dB
V_D	4	V
V_G	-0.4 to -0.6	V
I_D	100	mA

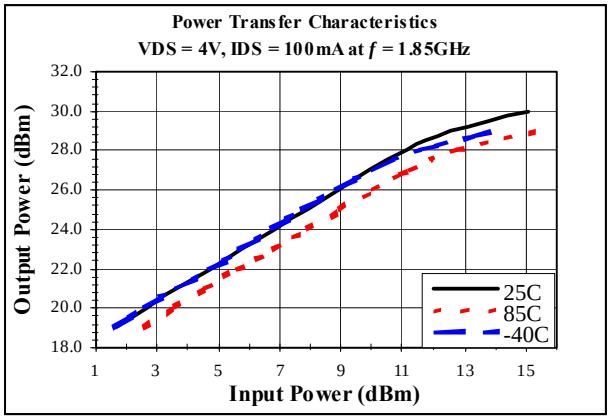
Note: OIP_3 measured at P_{OUT} of 12dBm per tone.

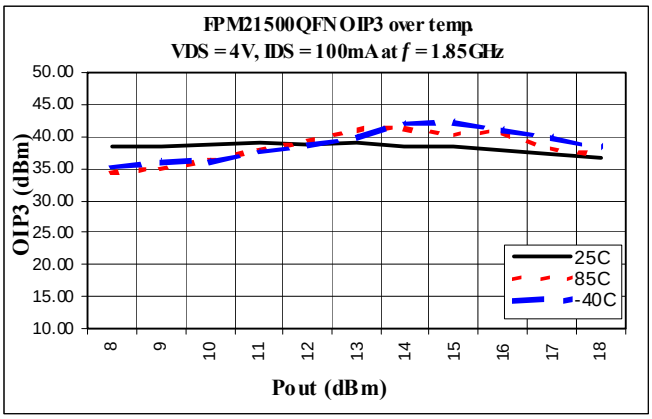
Board Layout

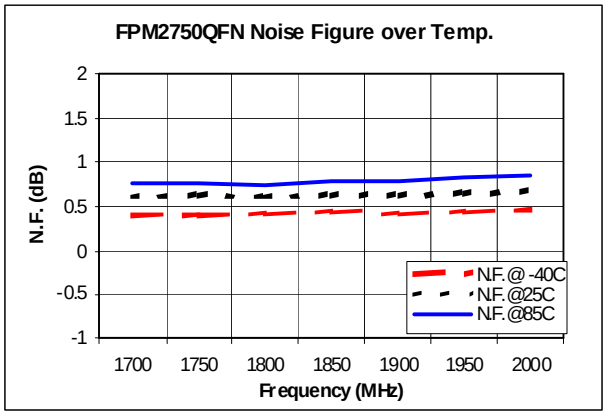


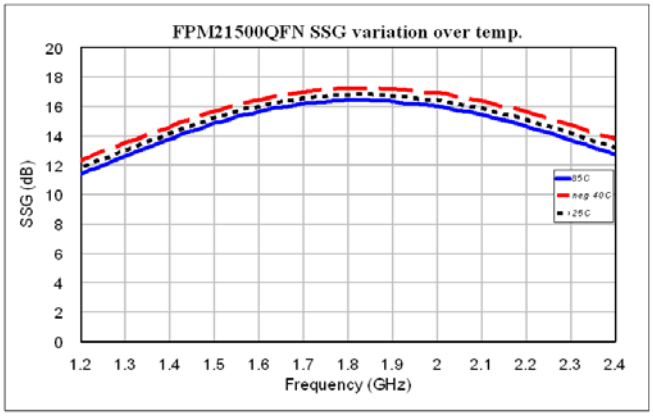
Comp:	Description
C1&C2	Cap. 0603 0.7pF ATC 600S ±0.05pF Tol.
C3&C4	Cap. 0603 1.5pF ATC 600S ±0.1pF Tol.
33pF x 8	Cap. 0603 ATC 600S
.01uF x 4	Cap. 0805 ATC805X103KL2AT
1.0uF x 2	SMD-B Tantallum x 2
L1 & L2	Inductor LL1005-FH 1.5nH TOKO ±0.3nH Tol.
L3 & L4	Inductor LL1005-FH 2.2nH TOKO ±0.3nH Tol.
Lg & Ld	Inductor LL1608-FH 22nH TOKO
Q1	FPM21500QFN
R1, R2	20 Ohm 0603 size Chip Resistor
R3,R4,R5,R6	100 Ohm 0603 size Chip Resistor x 4
A1 & A2	Anaren XC1900A-03 Hybrid Coupler (1900MHz)
P1 & P2	Edge mount RF Connector (Radial) R125.423.200
P3, P4, P5, P6	2-Pin Header.

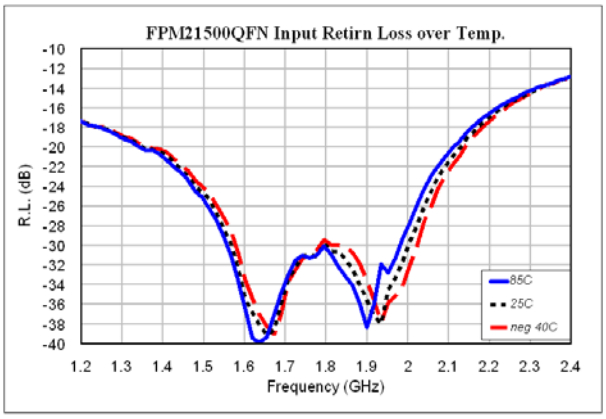
Typical Performance at 1.85GHz

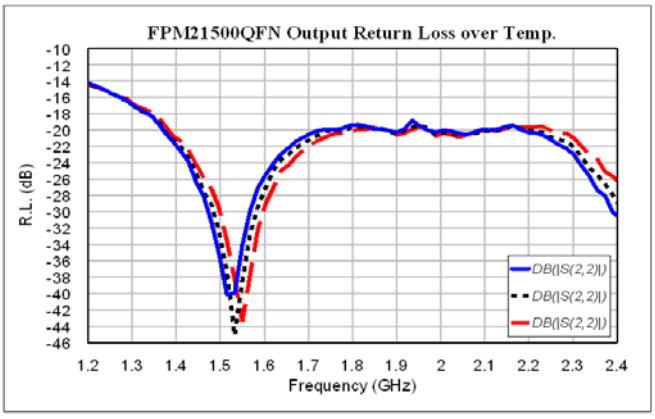












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Noise Parameters

Bias 4V, 100mA (Lower device)

Freq (GHz)	N.F.min. (dB)	Γopt Mag.	Γopt Angle	Rn/50
0.90	0.16	0.492	32.4	0.047
1.20	0.21	0.508	49.9	0.047
1.80	0.18	0.473	82.5	0.040
2.40	0.25	0.365	112.2	0.033
2.70	0.31	0.326	125.7	0.030
3.30	0.39	0.304	159.3	0.027
3.60	0.56	0.269	-178.2	0.036
4.50	0.55	0.41	-152.7	0.035
5.10	0.62	0.502	-141.6	0.038
5.70	0.68	0.56	-130.9	0.055

Bias 4V, 100mA (Upper device)

Freq (GHz)	N.F.min. (dB)	Γopt Mag.	Γopt Angle	Rn/50
0.90	0.16	0.415	36	0.046
1.20	0.16	0.471	51.6	0.046
1.80	0.22	0.409	83.4	0.040
2.40	0.28	0.346	114.3	0.034
2.70	0.36	0.327	124.1	0.031
3.30	0.45	0.3	156.5	0.028
3.60	0.42	0.277	173.3	0.035
4.50	0.5	0.363	-161.8	0.033
5.10	0.62	0.436	-140	0.042
5.70	0.66	0.485	-124.8	0.063

Bias 3V, 50mA (Lower device)

Freq (GHz)	N.F.min. (dB)	Γopt Mag.	Γopt Angle	Rn/50
0.90	0.19	0.562	33.9	0.049
1.20	0.2	0.637	50.4	0.050
1.80	0.15	0.572	81.6	0.042
2.40	0.22	0.442	108	0.035
2.70	0.28	0.399	120.5	0.030
3.30	0.36	0.353	150.8	0.026
3.60	0.56	0.282	173.9	0.035
4.50	0.52	0.432	-160.1	0.029
5.10	0.56	0.531	-148.4	0.030
5.70	0.61	0.598	-136.3	0.044

Bias 3V, 50mA (Upper device)

Freq (GHz)	N.F.min. (dB)	Γopt Mag.	Γopt Angle	Rn/50
0.90	0.18	0.476	37.6	0.048
1.20	0.15	0.584	52.6	0.049
1.80	0.18	0.487	82.9	0.042
2.40	0.24	0.419	109.9	0.036
2.70	0.31	0.397	120.3	0.031
3.30	0.4	0.353	149.1	0.026
3.60	0.35	0.327	164.8	0.031
4.50	0.44	0.403	-170	0.027
5.10	0.54	0.468	-147.6	0.033
5.70	0.57	0.504	-131.4	0.053

S-Parameters

Bias 4V, 100mA (Lower Device)

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.300	0.933	-61.8	21.674	142.6	0.021	59.6	0.237	-118.3
0.600	0.855	-99.7	16.086	120.3	0.031	44.2	0.320	-140.2
0.900	0.818	-125.5	12.326	104.8	0.037	35.2	0.363	-156.3
1.200	0.797	-142.9	9.860	93.4	0.041	30.0	0.381	-167.3
1.500	0.785	-156.1	8.178	84.1	0.044	26.5	0.388	-175.9
1.800	0.778	-166.7	6.977	75.9	0.047	23.7	0.392	176.6
2.100	0.759	-175.1	6.247	68.2	0.051	21.0	0.375	170.8
2.400	0.756	176.4	5.528	61.1	0.054	18.4	0.377	163.7
2.700	0.755	168.6	4.956	54.1	0.058	15.8	0.378	156.6
3.000	0.755	161.3	4.487	47.3	0.061	13.1	0.380	150.0
3.300	0.755	154.2	4.085	40.7	0.064	10.2	0.385	143.3
3.600	0.757	147.6	3.753	34.3	0.067	7.3	0.391	136.5
3.900	0.763	141.1	3.465	28.1	0.071	4.3	0.401	130.1
4.200	0.768	134.5	3.230	21.7	0.075	1.0	0.411	123.1
4.500	0.772	128.1	3.012	15.2	0.078	-2.7	0.421	116.5
4.800	0.775	121.8	2.796	8.7	0.081	-6.5	0.432	110.3
5.100	0.778	115.7	2.603	2.6	0.083	-10.4	0.445	105.1
5.400	0.783	109.7	2.431	-3.4	0.086	-13.8	0.460	99.6
5.700	0.785	103.7	2.273	-9.4	0.089	-17.5	0.477	95.0
6.000	0.792	98.2	2.138	-14.1	0.092	-20.1	0.503	93.2

Bias 4V, 100mA (Upper Device)

FREQ[GHz]	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
0.300	0.948	-59.4	17.894	143.8	0.027	60.1	0.261	-120.0
0.600	0.874	-95.1	13.490	122.9	0.041	43.2	0.373	-141.2
0.900	0.830	-121.2	10.448	107.2	0.049	32.7	0.428	-157.2
1.200	0.808	-138.9	8.427	95.6	0.053	25.9	0.454	-168.4
1.500	0.798	-152.7	7.025	86.2	0.057	21.3	0.465	-177.3
1.800	0.784	-163.4	6.027	77.9	0.060	17.6	0.469	175.0
2.100	0.770	-171.8	5.416	70.2	0.065	14.2	0.456	168.4
2.400	0.765	179.3	4.807	63.0	0.068	10.9	0.459	161.2
2.700	0.762	171.5	4.317	55.9	0.070	7.9	0.461	154.0
3.000	0.763	163.7	3.925	49.0	0.074	4.8	0.463	147.2
3.300	0.758	156.2	3.578	42.3	0.076	1.7	0.468	140.1
3.600	0.761	149.2	3.287	35.7	0.079	-1.6	0.474	133.6
3.900	0.765	142.2	3.032	29.3	0.082	-4.8	0.483	126.9
4.200	0.766	135.8	2.812	22.7	0.085	-8.3	0.489	120.2
4.500	0.773	129.2	2.608	16.5	0.088	-11.8	0.500	114.0
4.800	0.772	122.6	2.426	10.3	0.090	-15.3	0.513	107.8
5.100	0.781	116.3	2.260	4.3	0.092	-18.9	0.527	102.6
5.400	0.787	110.3	2.109	-1.5	0.094	-22.1	0.541	97.1
5.700	0.792	104.6	1.971	-7.4	0.096	-25.6	0.555	92.2
6.000	0.778	96.5	1.841	-13.0	0.097	-29.1	0.584	89.8

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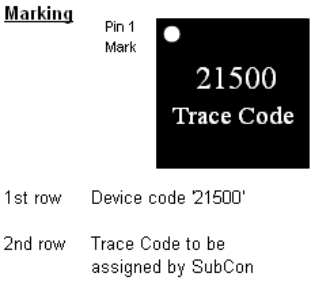
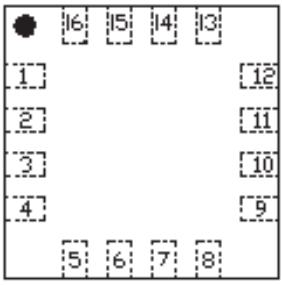
Part Identification



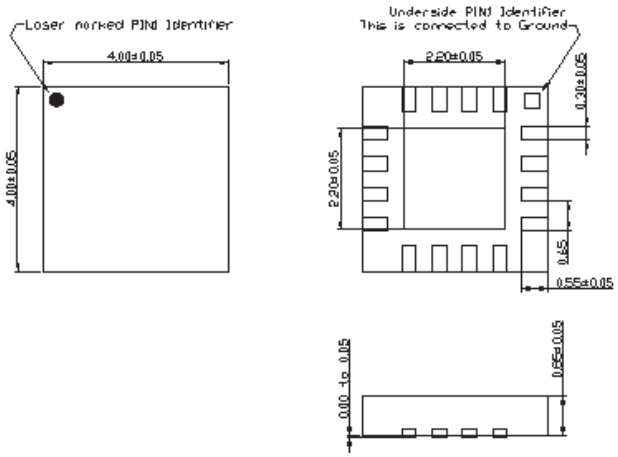
Pad Layout



Terminal	Function
1-4, 6, 15	Source 1
5	RFin 1
7, 9-12, 14	Source 2
8	RFin 2
13	RFout 2
16	RFout 1

Note: Dimensions in millimeters. Center paddle and pin 1 identifier are grounded.

Package Drawing



Tape and Reel

Tape and reel information on this material is in accordance with EIA-481-1 except where exceptions are identified.

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Preferred Assembly Instructions

This package is compatible with both lead-free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020. The maximum package temperature should not exceed 260 °C.

Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control can be found in MIL-STD-1686 AND MIL-HDBK-263.

MSL Rating

The device has an MSL rating of Level 1. To determine this rating, the preconditioning was performed on the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, Moisture/Reflow sensitivity classification for non-hermatic solid state surface mount devices.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise parameters, and device model are available from http://www.rfmd.com.

Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Description	Ordering Code
Packaged pHEMT	FPM21500QFN
Evaluation Board (1.85 GHz)	FPM21500QFNPCK

Delivery Quantity	Ordering Code
Reel of 1000	FPM21500QFN
Reel of 100	FPM21500QFNSR
Bag of 25	FPM21500QFNSQ
Bag of 5	FPM21500QFNSB

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