RF1604D

BROADBAND LOW POWER SP4T SWITCH

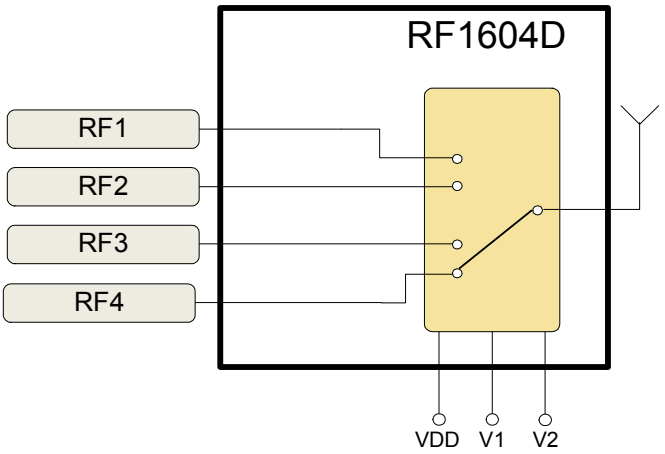
Package Style: QFN, 12-pin, 2.5mm x 2.5mm

Features

- 2kV HBM ESD Protection on All Ports
- Low Frequency to > 2.7GHz Operation
- Low Insertion Loss: 0.4dB at 1GHz
- Very High Isolation: 40dB at 1GHz
- Compatible With Low Voltage Logic (V_{HIGH} Min = 1.3V)
- High Linearity: IIP2 > 120dBm
- No External DC Blocking Capacitors Required on RF Paths Unless DC is applied Externally

Applications

- Multi-Mode GSM/EDGE/WCDMA, and LTE Applications
- Cellular Infrastructure Applications
- Receive Diversity Switching



Functional Block Diagram

Product Description

RF1604D is a single-pole four-throw (SP4T) switch designed for Receive Diversity switching applications. The RF1604D is ideally suited for battery operated applications requiring high performance switching with very low DC power consumption. The RF1604D features very low insertion loss with excellent linearity performance down to 1.3V control voltage. Additionally, RF1604D includes integrated decoding logic, allowing just two control lines needed for switch control. The RF1604D is packaged in a very compact 2.5mm x 2.5mm x 0.6mm, 12-pin, leadless QFN package. No DC-blocking capacitors are required on RF paths unless DC is applied externally to the device ports.

Ordering Information

RF1604D	Broadband Low Power SP4T Switch
RF1604DPCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
V_{DD}	3.0	V
Maximum Power Handling (6 to 1 VSWR over Temperature)	+23	dBm
Operating Temperature	-30 to +85	°C
Storage Temperature	-35 to +100	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Characteristics					Active Mode: $V_{HIGH} \geq 1.8V$, $V_{LOW} \leq 0.3V$; Temp = 25°C; V_{DD} = 2.5V P_{IN} = 16dBm @ 0.9GHz or 16dBm @ 1.98GHz; All RF ports terminated to $Z_O = 50\Omega$.
Insertion Loss					
RF1, RF2, RF3, RF4-ANT		0.40	0.50	dB	0.5GHz to 1GHz
		0.45	0.55	dB	1.0GHz to 2.0GHz
		0.45	0.55	dB	2.0GHz to 2.5GHz
		0.7	0.85	dB	2.5GHz to 3.5GHz
Isolation					
RF1, RF2, RF3, RF4-ANT	36	40		dB	0.5GHz to 1.0GHz
	31	35		dB	1.0GHz to 2.0GHz
	30	33		dB	2.0GHz to 2.5GHz
	23	28		dB	2.5GHz to 3.5GHz
RF Port Return Loss					
RF1, RF2, RF3, RF4-ANT	23	30		dB	0.5GHz to 3.5GHz, All RF ports in Insertion Loss state.
900MHz Harmonics					
Second Harmonic ($2f_0$)		-85	-75	dBc	P_{IN} = 35dBm
Third Harmonic ($3f_0$)		-90	-75	dBc	
1980MHz Harmonics					
Second Harmonic ($2f_0$)		-85	-75	dBc	P_{IN} = 16dBm
Third Harmonic ($3f_0$)		-90	-75	dBc	
IIP2					
RF1, RF2, RF3, RF4-ANT Cell	115	120		dBm	Tone 1: 836.5MHz at 16dBm, Tone 2: 1718MHz at -20dBm, Receive Freq: 881.5MHz
RF1, RF2, RF3, RF4-ANT AWS	115	120		dBm	Tone 1: 1732.5MHz at 16dBm, Tone 2: 3865MHz at -20dBm, Receive Freq: 2132.5MHz
RF1, RF2, RF3, RF4-ANT PCS	115	120		dBm	Tone 1: 1880MHz at 216dBm, Tone 2: 3840MHz at -20dBm, Receive Freq: 1960MHz
IIP3					

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Characteristics (Continued)					Active Mode:$V_{HIGH} \geq 1.8V$, $V_{LOW} \leq 0.3V$; Temp = 25°C; V_{DD} = 2.5V P_{IN} = 16dBm @ 0.9GHz or 16dBm @ 1.98GHz; All RF ports terminated to $Z_O = 50\Omega$.
RF1, RF2, RF3, RF4-ANT Cell	68	73		dBm	Tone 1: 836.5MHz at 16dBm, Tone 2: 791.5MHz at -20dBm, Receive Freq: 881.5MHz
RF1, RF2, RF3, RF4-ANT IMT	68	73		dBm	Tone 1: 1950MHz at 16dBm, Tone 2: 1760MHz at -20dBm, Receive Freq: 2140MHz
Triple Beat Ratio (TBR)					
TBR BC0 (GSM800)	85	99		dBc	VSWR = 2:1; Temp = -20°C, 25°C, +85°C
TBR BC1 (PCS)	85	99		dBc	VSWR = 2:1; Temp = -20°C, 25°C, +85°C
TBR BC4	85	99		dBc	VSWR = 2:1; Temp = -20°C, 25°C, +85°C
TBR BC5 (GSM400)	85	99		dBc	VSWR = 2:1; Temp = -20°C, 25°C, +85°C
TBR BC14 (PCS)	85	99		dBc	VSWR = 2:1; Temp = -20°C, 25°C, +85°C
TBR BC15 (AWS)	85	99		dBc	VSWR = 2:1; Temp = -20°C, 25°C, +85°C
Max Operating Power					
			21	dBm	VSWR = 6:1, Temp = -30° to +85°C
Switching Time					
Switching Speed ON		2	5	µs	50% control to 90% RF
Switching Speed OFF		2	5	µs	50% control to 10% RF
Start-Up Time			10	µs	Maximum set up time for the switch to reach fully compliant operation
Supply and Control Signal Characteristics					
Switched Supply Voltage (V_{DD})					
V_{HIGH}	2.2	2.5	2.7	V	
V_{LOW}		0	0.3	V	
Switched Supply Current (V_{DD})					
I_{HIGH}		50	100	µA	P_{IN} = 16dBm
I_{LOW}		0		mA	
Control Voltage (V1, V2)					
V_{HIGH}	1.3	1.8	2.6	V	
V_{LOW}	0	0	0.45	V	
Control Current (V1, V2)					
I_{HIGH}		1.0	5.0	µA	
I_{LOW}		0.5	1.0	µA	

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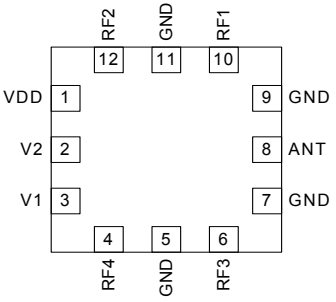
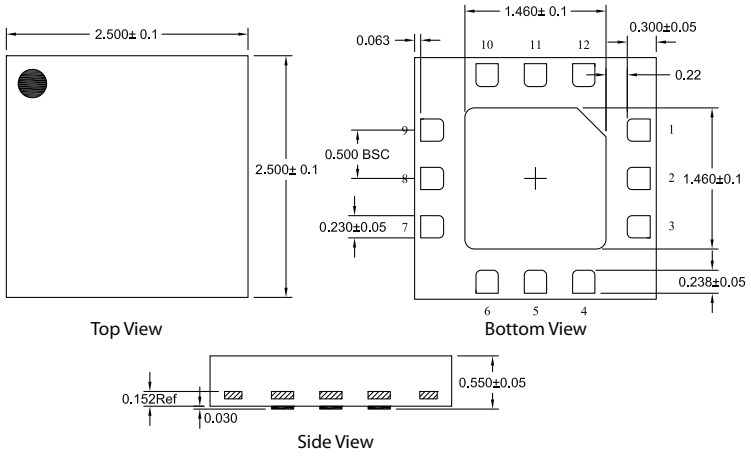
Pin	Function	Description
1	VDD	Supply. The voltage at this node will be switched and it is important that the switch is operating within the specified start up time. This signal might be used as a mode control.
2	V2	Control signal 2.
3	V1	Control signal 1.
4	RF4	RF output 4.
5	GND	Ground.
6	RF3	RF output 3.
7	GND	Ground.
8	ANT	RF input (connected to antenna).
9	GND	Ground.
10	RF1	RF output 1.
11	GND	Ground.
12	RF2	RF output 2.
Pkg Base	GND	Ground.

Pin Out



Top View

Package Drawing



General Information

Truth Table for Switch States

State	V1	V2	RF Path
1	V_{LOW}	V_{LOW}	ANT-RF1
2	V_{LOW}	V_{HIGH}	ANT-RF2
3	V_{HIGH}	V_{LOW}	ANT-RF3
4	V_{HIGH}	V_{HIGH}	ANT-RF4

Control Logic

The switch is operable in four states (see Truth Table). When V_{DD} is high, the switch is active. The start-up time is defined as the delay time that control signal(s) cross 0.8V threshold until KF output level is 90% of final RF voltage peak.

Power Sequence

ON Sequence: First turn ON V_{DD}, then apply control signals.

OFF Sequence: First turn OFF the control signals, then turn OFF V_{DD}.

Note:

Not following the power ON/OFF sequence could cause damage to the switch and may affect the long-term reliability of the device.

Electrical Test Methods

The electrical parameters for the switch were measured on RFMD evaluation board. The test PWB includes means for decoupling RF signals from control signal port (shunt capacitor at control signal ports).

All measurements are done with calibration plane at switch pins. The effect of test board losses and phase delay has been removed from the results.

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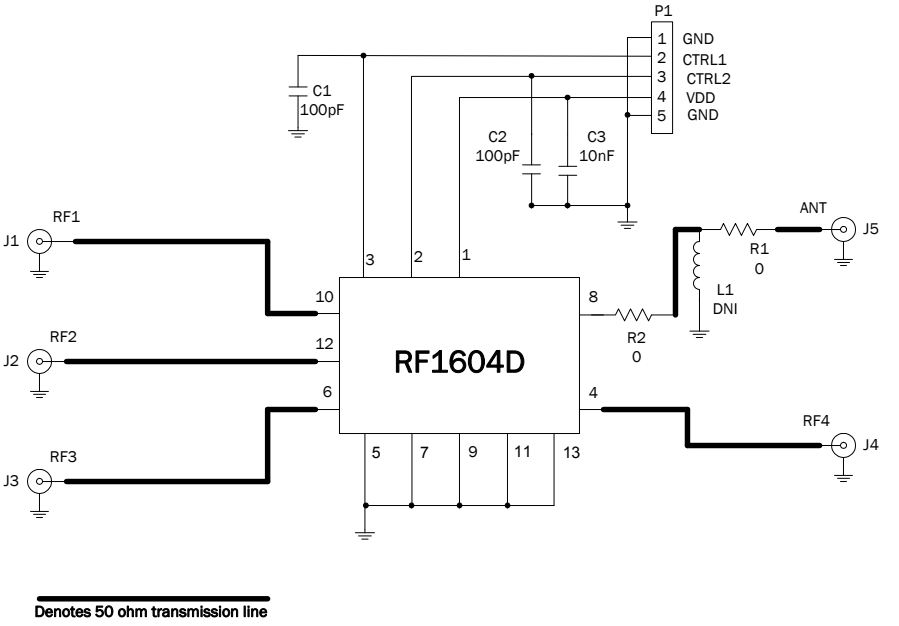
Evaluation Board Schematic



PCB Design Requirements

PCB Surface Finish

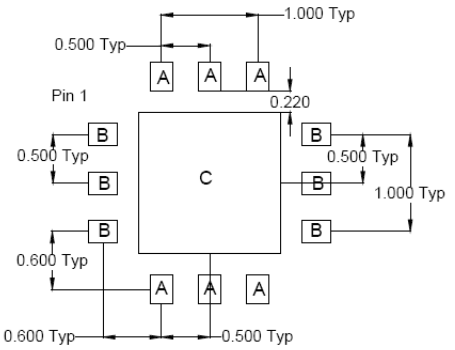
The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

A = 0.230 x 0.300 (mm) Typ
B = 0.300 x 0.230 (mm) Typ
C = 1.460 (mm) Sq



PCB METAL LAND PATTERN

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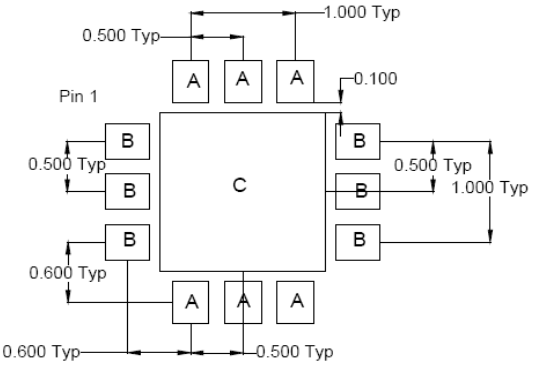
PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2 mil to 3 mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

A = 0.350 x 0.420 (mm) Typ
B = 0.420 x 0.350 (mm) Typ
C = 1.580 (mm) Sq



PCB SOLDER MASK LAND PATTERN

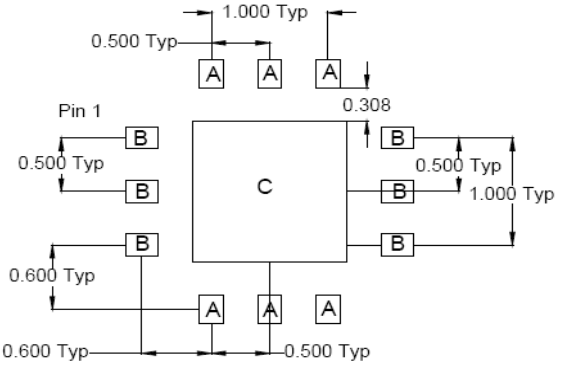
Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

A = 0.207 x 0.270 (mm) Typ
B = 0.270 x 0.207 (mm) Typ
C = 1.314 (mm) Sq



PCB STENCIL PATTERN

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