

RoHS Compliant & Pb-Free Product  
Package Style: QFN, 16-Pin, 4mmx4mm

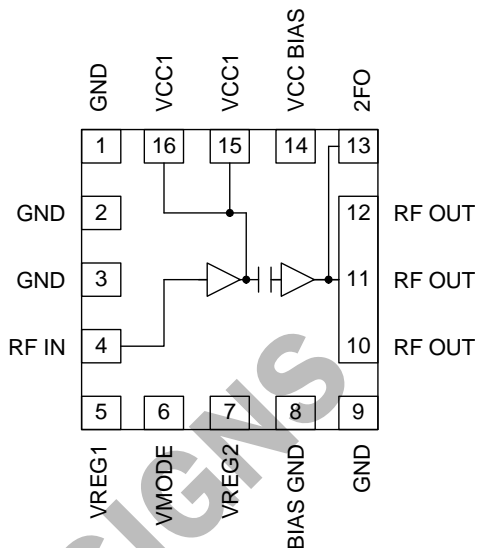


**Features**

- Single 3V Supply
- 29dBm Linear Output Power
- 37% Linear Efficiency
- Low Power Mode
- 45 mA idle current
- 47% Peak Efficiency 31dBm Output

**Applications**

- 3V CDMA/AMPS Cellular Handsets
- 3V JCDMA Cellular Handsets
- 3V CDMA2000 Cellular Handsets
- 3V TDMA/GAIT Cellular Handsets
- 3V CDMA 450MHz Band Handsets
- Portable Battery-Powered Equipment



Functional Block Diagram

**Product Description**

The RF2192 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA/AMPS and CDMA2000 handheld digital cellular equipment, spread-spectrum systems, and other applications in the 800MHz to 960MHz band. The RF2192 has a low power mode to extend battery life under low output power conditions. The device is packaged in a 16-pin, 4mmx4mm QFN.

**Ordering Information**

RF2192                      3V 900MHz Linear Power Amplifier  
RF2192PCBA-41X        Fully Assembled Evaluation Board

**Optimum Technology Matching® Applied**

- |  |                                      |                                     |                                   |
|--|--------------------------------------|-------------------------------------|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET         | <input type="checkbox"/> Si BiCMOS   | <input type="checkbox"/> Si CMOS    | <input type="checkbox"/> RF MEMS  |
| <input type="checkbox"/> InGaP HBT           | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT     |                                   |

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## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V <sub>DC</sub>
Supply Voltage (P <sub>OUT</sub> ≤ 31dBm)	+5.2	V <sub>DC</sub>
Mode Voltage (V <sub>MODE</sub> )	+4.2	V <sub>DC</sub>
Control Voltage (V <sub>REG</sub> )	+3.0	V <sub>DC</sub>
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

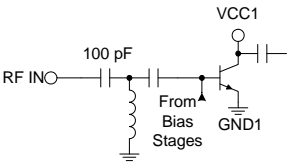
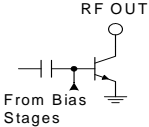
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Parameter	Specification			Unit	Chondition
	Min.	Typ.	Max.		
<b>Usable Frequency Range</b>	400		960	MHz	
<b>High Power State-US-CDMA (V<sub>MODE</sub> Low)</b>					Case T = 25 °C, V <sub>CC</sub> = 3.4V, V <sub>REG</sub> = 2.85V, V <sub>MODE</sub> = 0V to 0.5V, Freq = 824 MHz to 849 MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain	27	30		dB	
Second Harmonic		-33		dBc	
Third Harmonic		< -60		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		37		%	P <sub>OUT</sub> = 29 dBm
Adjacent Channel Power Rejection		-48	-44	dBc	ACPR @ 885 kHz
		-58	-56	dBc	ACPR @ 1980 kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. > -70 dBc
Noise Power		-133		dBm/Hz	At 45 MHz offset
<b>Low Power State-US-CDMA (V<sub>MODE</sub> High)</b>					Case T = 25 °C, V <sub>CC</sub> = 3.4V, V <sub>REG</sub> = 2.85V, V <sub>MODE</sub> = 1.8V to 3V, Freq = 824 MHz to 849 MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain	19	22		dB	
Second Harmonic		-33		dBc	
Third Harmonic		< -60		dBc	
Maximum Linear Output Power (CDMA Modulation)	16	20		dBm	
Max I <sub>CC</sub>		150		mA	P <sub>OUT</sub> = +16 dBm (all currents included)
Adjacent Channel Power Rejection		-48	-46	dBc	ACPR @ 885 kHz
		< -60	-58	dBc	ACPR @ 1980 kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. > -70 dBc

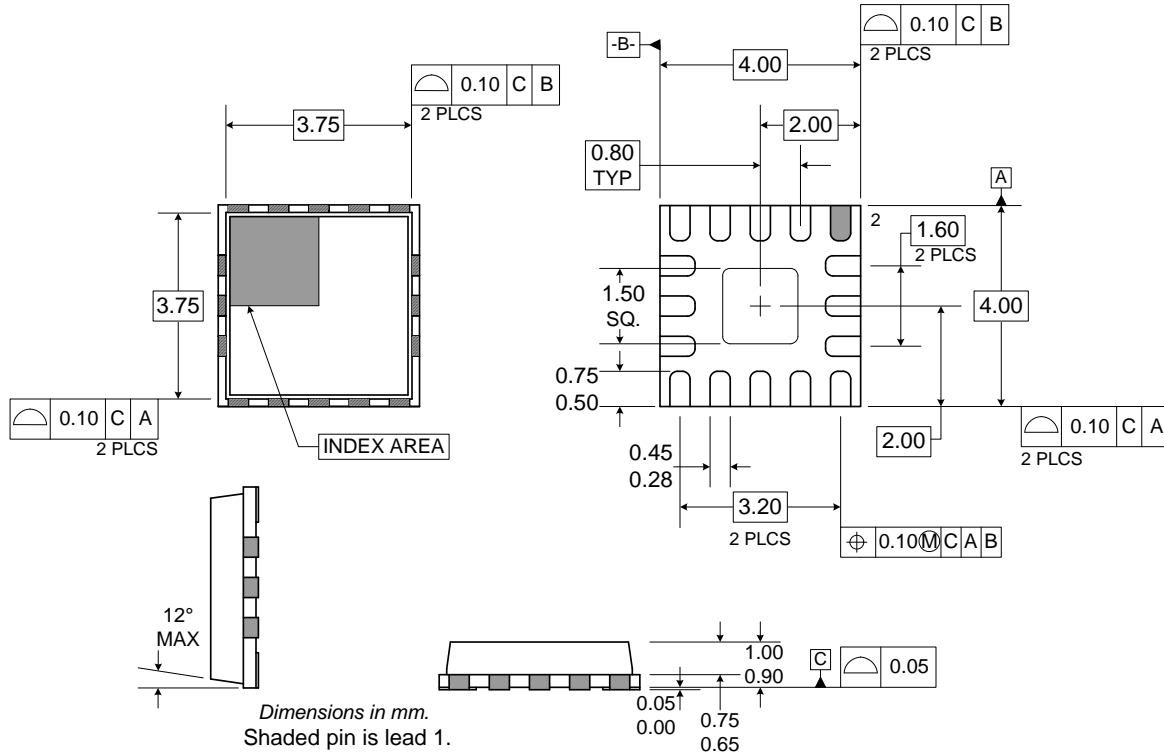
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Power State CDMA 2000 1x (V<sub>MODE</sub> LOW)</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V. V <sub>MODE</sub> =0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Linear Gain		29		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	26.5			dBm	2.5 dB Backoff included in IS98D CCDF 1% 5.4 dB Peak Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		-47		dBc	ACPR@885 kHz
		< -60		dBc	ACPR@1.98MHz
Pilot+FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	29			dBm	4.5 dB Peak Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		-47		dBc	ACPR@885 kHz
		< -60		dBc	ACPR@1.98MHz
<b>Low Power State CDMA 2000 1x (V<sub>MODE</sub> HIGH)</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V. V <sub>MODE</sub> =1.8V to 3V, Freq=824MHz to 849MHz
Frequency Range	824		849	MHz	
Linear Gain		22		dB	
Pilot+DCCH 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	5.4 dB Peak to Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		-48		dBc	ACPR@885 kHz
		< -85		dBc	ACPR@1.98MHz
Efficiency		15		%	P <sub>OUT</sub> =20dBm
Pilot+FCH 9600+SCHO 9600					
Maximum Linear Output Power (CDMA 2000 Modulation)	16	20		dBm	4.5 dB Peak to Average Ratio at CCDF 1%
Adjacent Channel Power Rejection		< -50		dBc	ACPR@885 kHz
		< -65		dBc	ACPR@1.98MHz
<b>FM Mode</b>					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =0V to 0.5V, Freq=824MHz to 849MHz (unless otherwise specified)
Frequency Range	824		849	MHz	
Gain		30		dB	
Second Harmonic		-33		dBc	
Third Harmonic		< -60		dBc	
Max CW Output Power	31	32		dBm	
Total Efficiency (AMPS mode)		47		%	P <sub>OUT</sub> =31dBm (room temperature)
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. > -70dBc

Note: DCCH: Dedicated Control Channel  
 FCH: Fundamental Channel  
 CCDF: Complementary Cumulative Distribution Function

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>High Power State-CDMA450</b> (V <sub>MODE</sub> Low)					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =0V to 0.5V, Freq=452MHz to 458MHz (unless otherwise specified)
Frequency Range	452		458	MHz	
Linear Gain		31		dB	
Second Harmonic		30		dBc	
Third Harmonic		-60		dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		35		%	P <sub>OUT</sub> =29dBm
Adjacent Channel Power Rejection		-49		dBc	ACPR @ 885 kHz
		-56		dBc	ACPR @ 1980 kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. > -70 dBc
<b>Low Power State-CDMA450</b> (V <sub>MODE</sub> High)					Case T=25°C, V <sub>CC</sub> =3.4V, V <sub>REG</sub> =2.85V, V <sub>MODE</sub> =2.85V, Freq=452MHz to 458MHz (unless otherwise specified)
Frequency Range	452		458	MHz	
Linear Gain		23		dB	
Maximum Linear Output Power (CDMA Modulation)	16			dBm	
Max I <sub>CC</sub>		160		mA	P <sub>OUT</sub> =+16dBm (all currents included)
Adjacent Channel Power Rejection		-52		dBc	ACPR @ 885 kHz
		-70		dBc	ACPR @ 1980 kHz
Input VSWR		2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations. > -70 dBc
<b>DC Supply</b>					
Supply Voltage	3.0	3.4	4.2	V	The maximum power out for V <sub>CC</sub> =3.0V is 28dBm.
Quiescent Current		160		mA	V <sub>MODE</sub> =Low
		45	70	mA	V <sub>MODE</sub> =High
V <sub>REG</sub> Current			10	mA	
V <sub>MODE</sub> Current			1	mA	
Turn On/Off Time			<40	μs	Time between V <sub>REG</sub> turned on and PA reaching full power. Turn on/off time can be reduced by lowering the bypass capacitor value on the V <sub>REG</sub> line.
Total Current (Power Down)			10	μA	V <sub>REG</sub> =Low
V <sub>REG</sub> "Low" Voltage	0		0.5	V	
V <sub>REG</sub> "High" Voltage	2.75	2.85	2.95	V	
V <sub>MODE</sub> "Low" Voltage	0		0.5	V	
V <sub>MODE</sub> "High" Voltage	1.8	2.85	3.0	V	

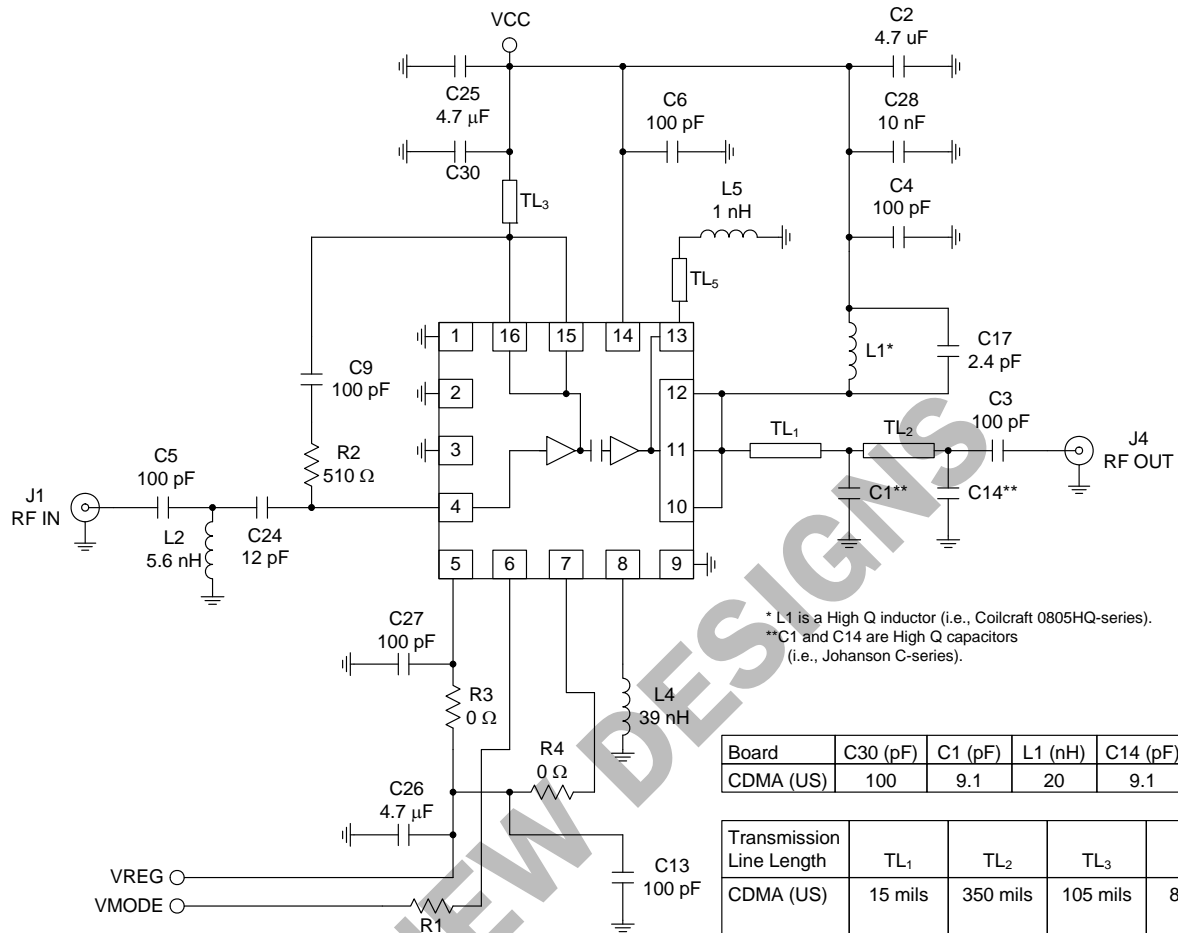
Pin	Function	Description	Interface Schematic
1	GND	Ground connection.	
2	GND	Ground connection.	
3	GND	Ground connection.	
4	RF IN	RF input. An external 100 pF series capacitor is required as a DC block. In addition, shunt inductor and series capacitor are required to provide 2:1 VSWR.	
5	VREG1	Power Down control for first stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V <sub>REG</sub> and V <sub>MODE</sub> need to be LOW (<0.5V).	
6	VMODE	For nominal operation (High Power Mode), V <sub>MODE</sub> is set LOW. When set HIGH, the driver and final stage are dynamically scaled to reduce the device size and as a result to reduce the idle current.	
7	VREG2	Power Down control for the second stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V <sub>REG</sub> and V <sub>MODE</sub> need to be LOW (<0.5V).	
8	BIAS GND	Bias circuitry ground. See application schematic.	
9	GND	Ground connection.	
10	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 824 MHz to 849 MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	RF OUT	Same as pin 10.	See pin 10.
12	RF OUT	Same as pin 10.	
13	2FO	Harmonic trap. This pin connects to the RF output but is used for providing a low impedance to the second harmonic of the operating frequency. An inductor or transmission line resonating with an on chip capacitor at 2fo is required at this pin.	
14	VCC BIAS	Power supply for bias circuitry. A 100 pF high frequency bypass capacitor is recommended.	
15	VCC1	Power supply for first stage.	
16	VCC1	Same as Pin 15.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

## Package Drawing

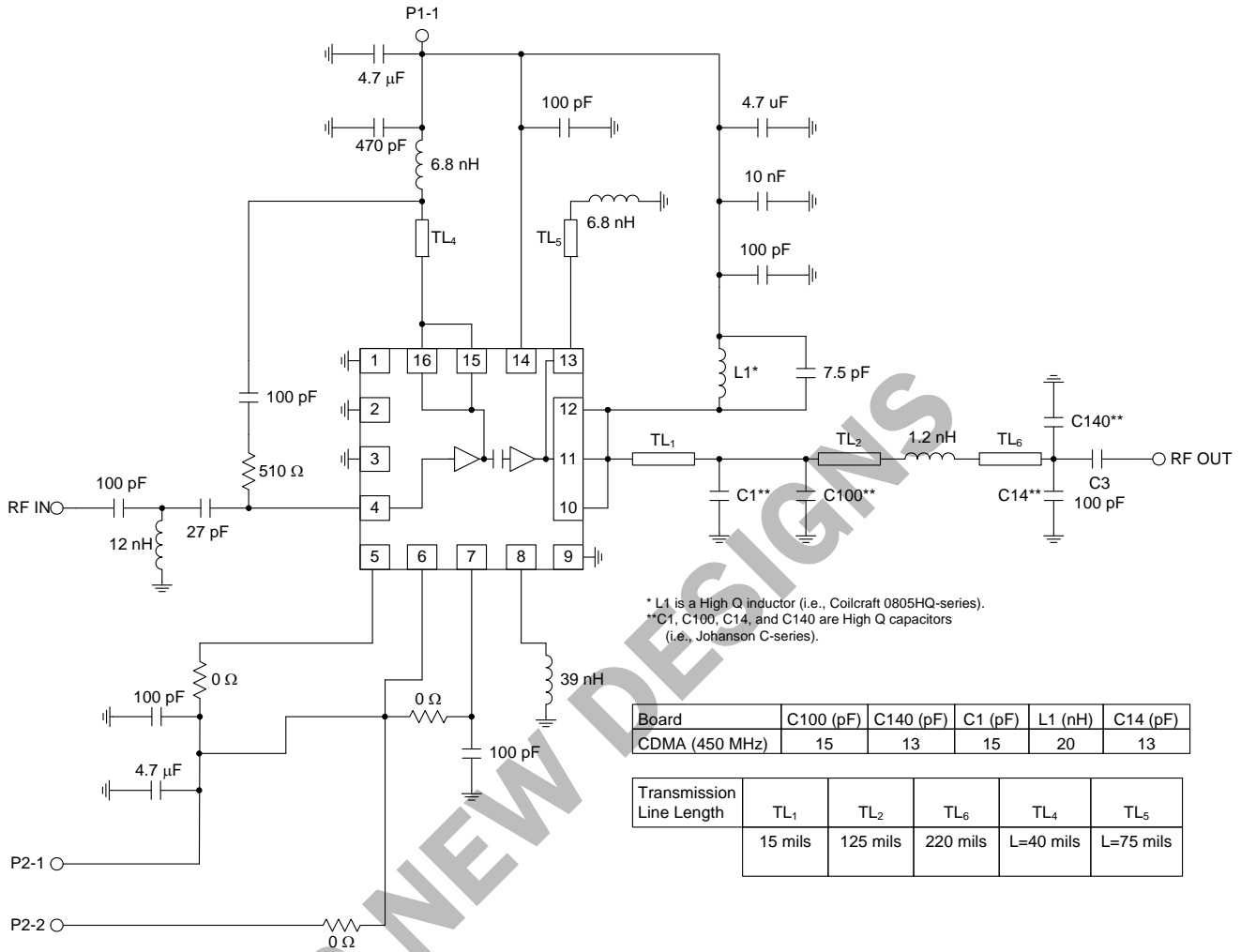


NOT FOR NEW DESIGN

Evaluation Board Schematic  
US-CDMA



## Application Schematic CDMA-450MHz Band



\* L1 is a High Q inductor (i.e., Coilcraft 0805HQ-series).  
 \*\*C1, C100, C14, and C140 are High Q capacitors (i.e., Johanson C-series).

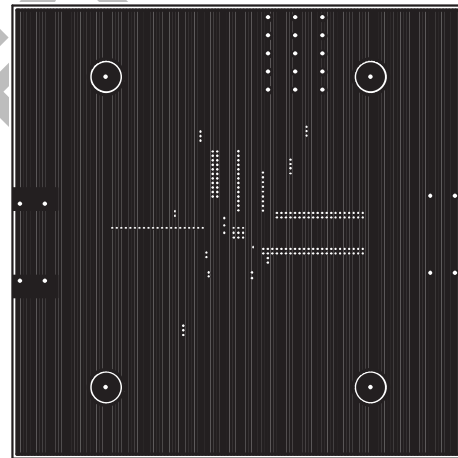
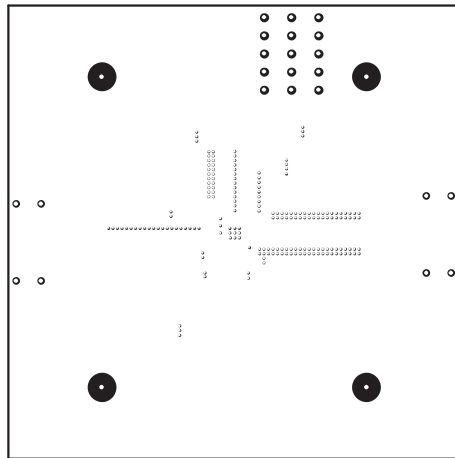
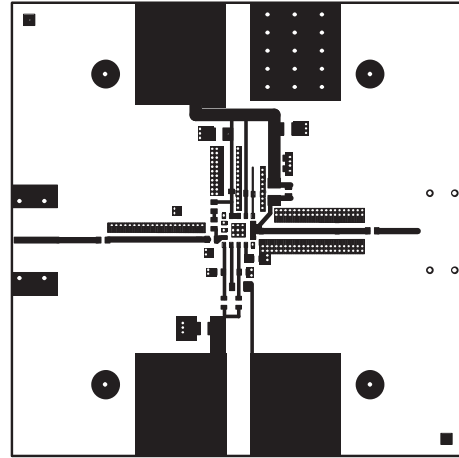
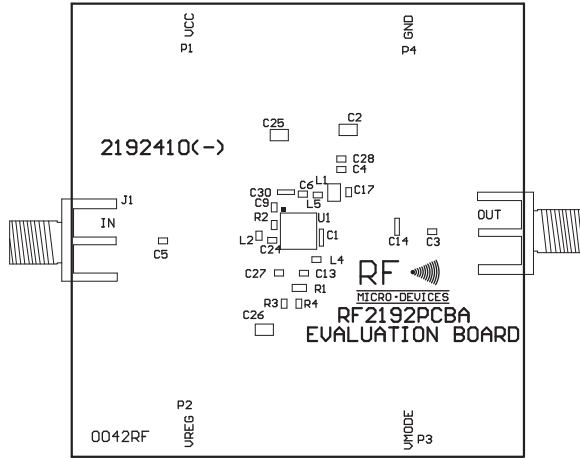
Board	C100 (pF)	C140 (pF)	C1 (pF)	L1 (nH)	C14 (pF)
CDMA (450 MHz)	15	13	15	20	13

Transmission Line Length	TL <sub>1</sub>	TL <sub>2</sub>	TL <sub>6</sub>	TL <sub>4</sub>	TL <sub>5</sub>
	15 mils	125 mils	220 mils	L=40 mils	L=75 mils



**Evaluation Board Layout - US-CDMA**  
**2.0" x 2.0"**

Board Thickness 0.031", Board Material FR-4, Multi-Layer, Ground Plane at 0.015"



## PCB Design Requirements

### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

### PCB Metal Land Pattern

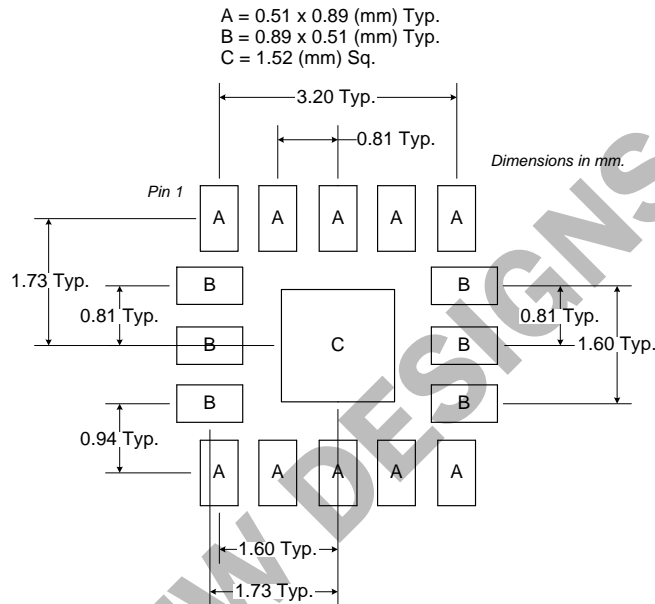


Figure 1. PCB Metal Land Pattern (Top View)



**NOT FOR NEW DESIGNS**