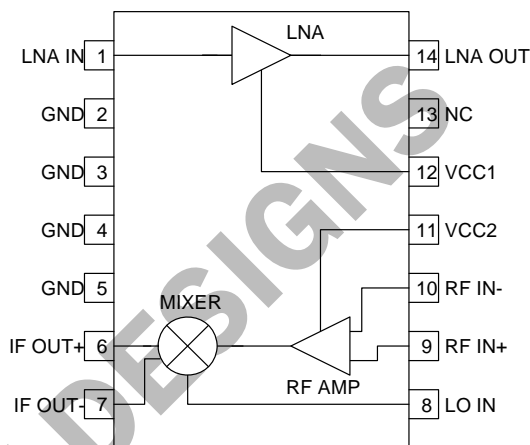


**Features**

- Single 3V to 6.5V Power Supply
- 500MHz to 1900MHz Operation
- 25dB Small Signal Gain
- 2.5dB Cascaded Noise Figure
- 8.5 mA DC Current Consumption
- -8dBm Input IP<sub>3</sub>

**Applications**

- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread-Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- General Purpose Frequency Conversion



Functional Block Diagram

**Product Description**

The RF2411 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the RF functions of the receiver except for the passive filtering and LO generation. It contains an LNA (low-noise amplifier), a second RF amplifier, and a balanced mixer which can drive a single-ended or balanced load. The output of the LNA is made available as a pin to permit the insertion of a bandpass filter between the LNA and the RF/Mixer section. The LNA output is buffered to permit a wide range of choices for the interstage filter without altering the VSWR or noise figure at the LNA input and to provide high isolation from the LO to the input port. The LNA section may be disabled to conserve power.

**Ordering Information**

RF2411	Low Noise Amplifier/Mixer
RF2411 PCBA-L	Fully Assembled Evaluation Board (850MHz)
RF2411 PCBA-H	Fully Assembled Evaluation Board (1800MHz)

**Optimum Technology Matching® Applied**

- |  |                                      |                                     |                                   |
|--|--------------------------------------|-------------------------------------|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET         | <input type="checkbox"/> Si BiCMOS   | <input type="checkbox"/> Si CMOS    |                                   |
| <input type="checkbox"/> InGaP HBT           | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT     |                                   |

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## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V <sub>DC</sub>
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

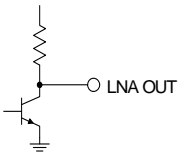
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Parameter (850 MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T = 25 °C, V <sub>CC</sub> = 5V, RF = 850 MHz, LO = 0 dBm, IF = 50 MHz, Application Schematic 2 configuration
RF Frequency Range		500 to 1900		MHz	
IF Frequency Range		DC to 150		MHz	
Cascade Gain		27		dB	IF = 10 MHz
	21	25	29		IF = 50 MHz
		20			IF = 150 MHz
Cascade IP3		-8		dBm	Referenced to the input
Cascade Noise Figure		2.4		dB	Single sideband, IF = 10 MHz
		2.4			Single sideband, IF = 50 MHz
		3.4			Single sideband, IF = 150 MHz
<b>First Section (LNA)</b>					
Noise Figure		1.6		dB	
Input VSWR		1.5:1			
Input IP3		-3.5		dBm	
Gain		14		dB	
Reverse Isolation		30		dB	
Output VSWR		2.0:1			
<b>Second Section (RF Amp, Mixer, IF1)</b>					
Noise Figure		11.0		dB	Single Sideband
Input VSWR		2.0:1			
Input IP3		+6		dBm	
Conversion Gain		11		dB	
Output Impedance		4		kΩ	Open Collector
<b>LO Input</b>					
LO Level		-6 to +6		dBm	
LO to RF Rejection		30		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.5:1			
<b>Power Supply</b>					
Voltage		3 to 6.5		V	
Current Consumption		8		mA	V <sub>CC</sub> = 3.0V
		20		mA	V <sub>CC</sub> = 5.0V

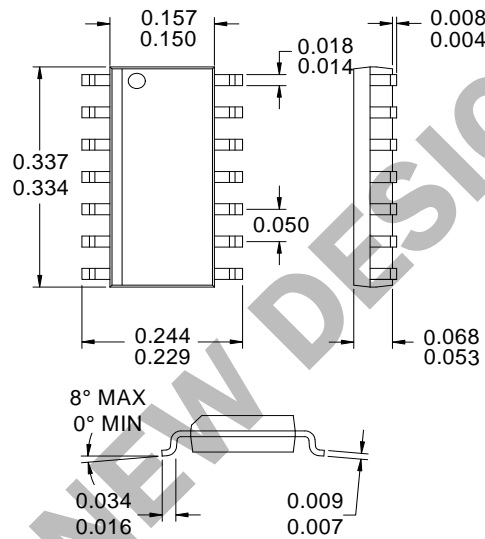
Parameter (1800 MHz)	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Overall</b>					T = 25 ° C, V <sub>CC</sub> = 5V, RF = 1800MHz, LO = 0dBm, IF = 50MHz, Application Schematic 2 configuration
RF Frequency Range		500 to 1900		MHz	
IF Frequency Range		DC to 100		MHz	
Cascade Gain		22		dB	IF = 10MHz
		21			IF = 50MHz
		17			IF = 150MHz
Cascade IP3		-7		dBm	Referenced to the input
Cascade Noise Figure		4.0		dB	Single sideband, IF = 10MHz
		4.0			Single sideband, IF = 50MHz
		4.8			Single sideband, IF = 150MHz
<b>First Section (LNA)</b>					
Noise Figure		2.6		dB	
Input VSWR		1.2:1			
Input IP3		-3.5		dBm	
Gain		10		dB	
Reverse Isolation		25		dB	
Output VSWR		1.5:1			
<b>Second Section (RF Amp, Mixer, IF1)</b>					
Noise Figure		10.0		dB	Single Sideband
Input VSWR		2.0:1			
Input IP3		+3		dBm	
Conversion Gain		11		dB	
Output Impedance		4		kΩ	Open Collector
<b>LO Input</b>					
LO Level		-6 to +6		dBm	
LO to RF Rejection		30		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.2:1			

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Pin	Function	Description	Interface Schematic
1	LNA IN	This pin is NOT internally DC-blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz.	
2	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
3	GND	Same as pin 2.	
4	GND	Same as pin 2.	
5	GND	Same as pin 2.	
6	IF OUT+	Balanced open collector output of the mixer. External bias needs to be supplied to this pin. This can be done with a resistor to $V_{CC}$ (see application schematic, "1800MHz, Balanced Resistor Output Matching"), with a balun (see application schematic, "1800MHz, Output Matching with Balun") or when used in a single-ended configuration (see application schematic, "1800MHz, Single-Ended Resistive Output Matching"). When using a resistor to $V_{CC}$ the resistor value will set the output impedance. Typical values for this resistor are 200 $\Omega$ to 1k $\Omega$ . A shunt inductor/capacitor resonator to $V_{CC}$ is needed to maintain proper DC voltage at the mixer. At low resistor values the resonator may be omitted at the expense of gain, output power and IP3. To obtain maximum gain and output power a balun as shown in application schematics "1800MHz, Output Matching with Balun" and "850MHz, Output Matching with Balun" is recommended. Using both outputs and matching them correctly to a single ended load will result in a 6dB gain improvement over the plain single ended configuration.	
7	IF OUT-	Same as pin 6 except complementary output.	See pin 6.
8	LO IN	50 $\Omega$ mixer LO input. This pin has an internal pull-up resistor to $V_{CC}$ and is not DC-blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz.	
9	RF IN+	Balanced mixer RF Input port. This pin is NOT internally DC-blocked. An external blocking capacitor must be provided if the pin is connected to a device with a DC path. A value of 100pF is recommended for 900MHz and 22pF for 1800MHz. Matching is required; see the applications schematics. To minimize the noise figure it is recommended to have a bandpass filter before this input. This will prevent noise at the image frequency from being converted to the IF.	
10	RF IN-	Same as pin 9 except complementary input.	See pin 9.
11	VCC2	Supply voltage for the mixer bias circuits.	
12	VCC1	Supply Voltage for the LNA only. A 47 pF external bypass capacitor is required and an optional 0.01 $\mu$ F will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	

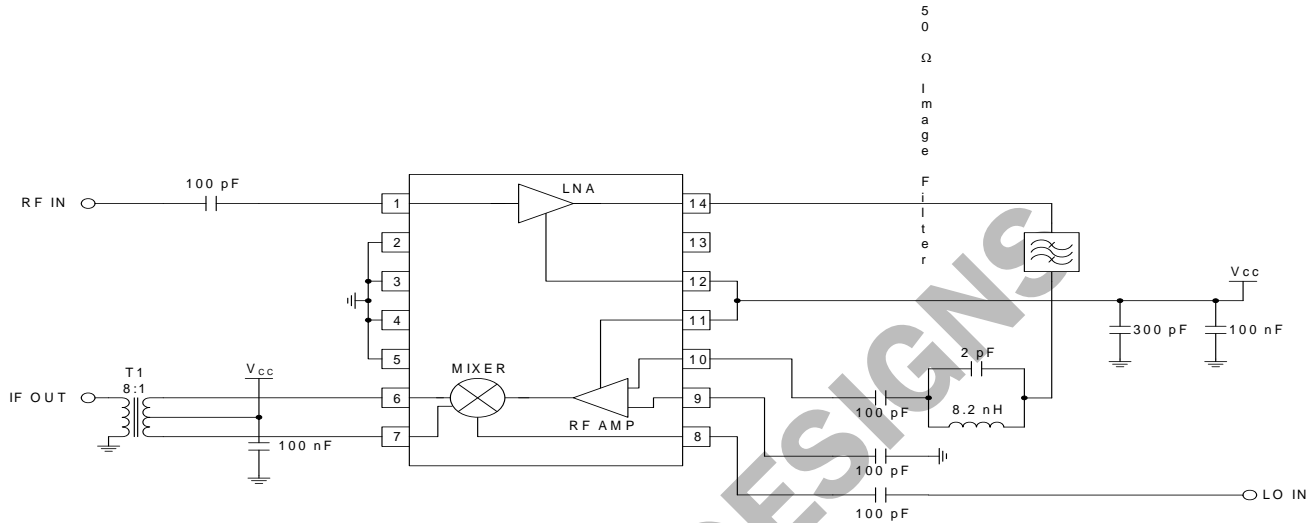
Pin	Function	Description	Interface Schematic
13	NC	No connection.	
14	LNA OUT	50Ω output. An external DC blocking capacitor is required when this pin is connected to a DC path.	

**Package Drawing**

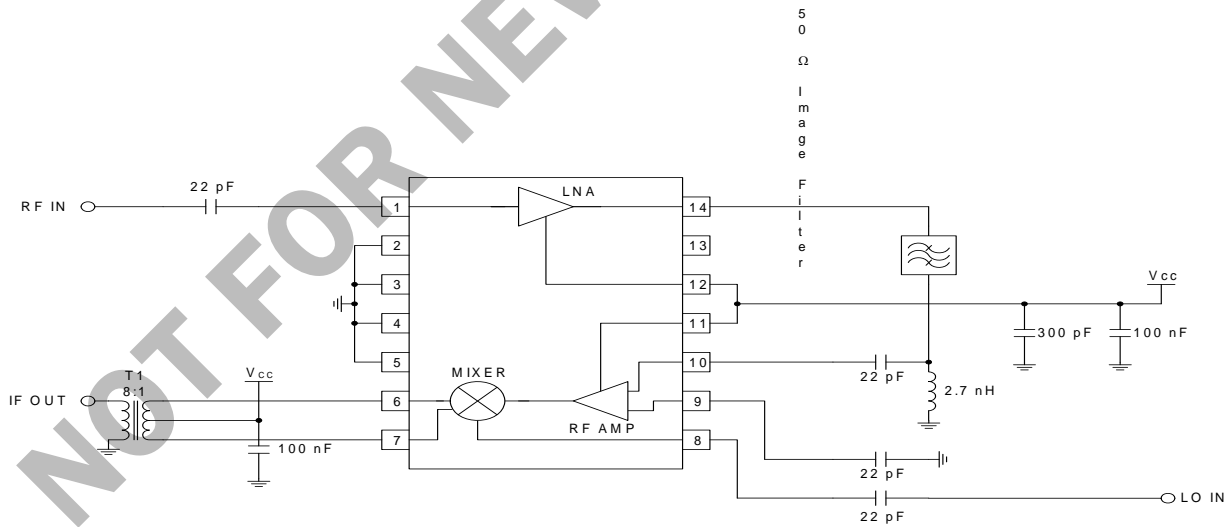


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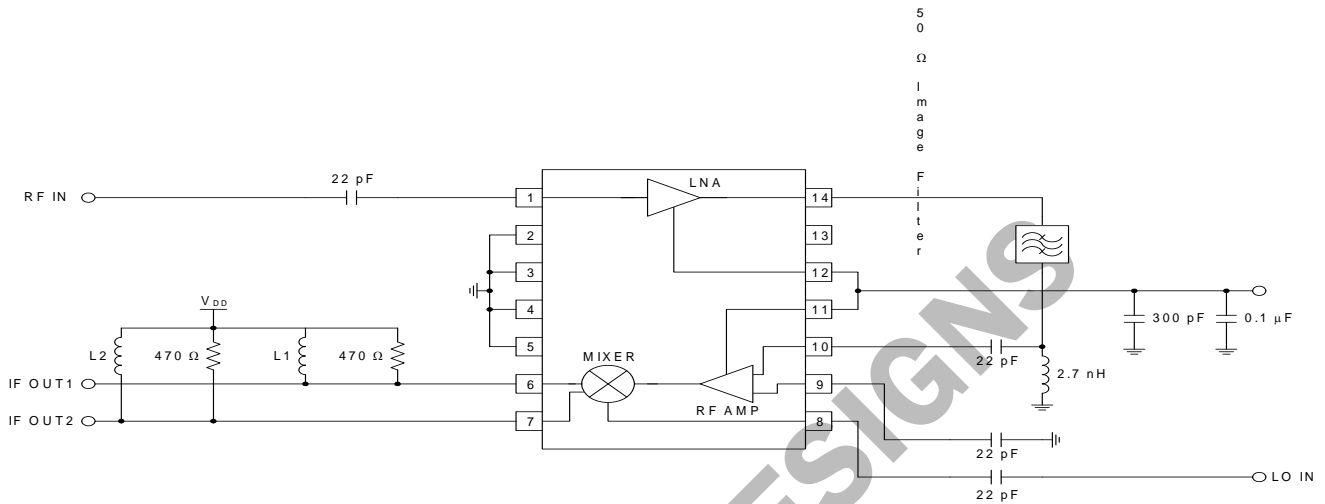
## Application Schematic 850MHz, Output Matching with Balun



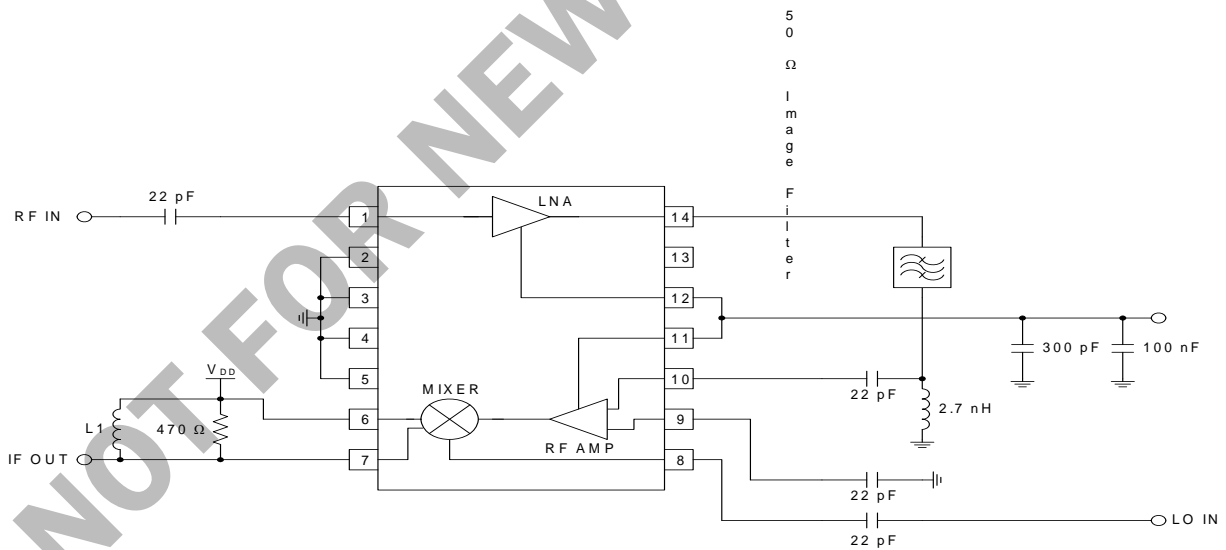
## Application Schematic 1800MHz, Output Matching with Balun



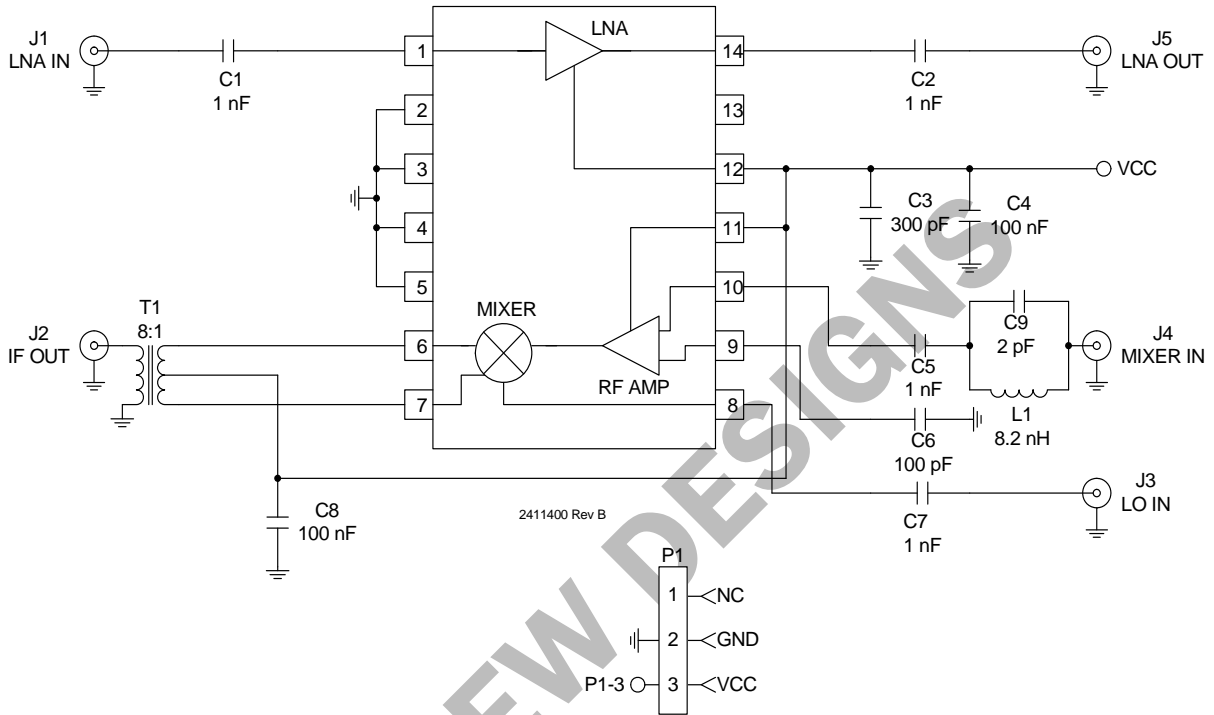
**Application Schematic**  
**1800MHz, Balanced Resistive Output Matching**



**Application Schematic**  
**1800MHz, Single-Ended Resistive Output Matching**



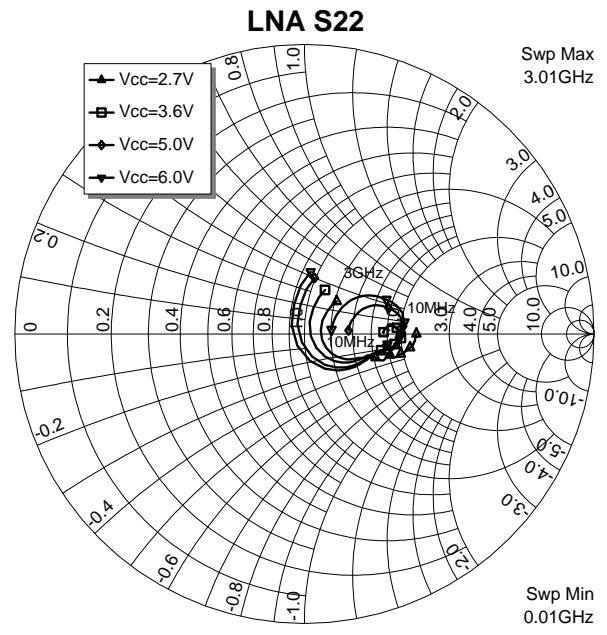
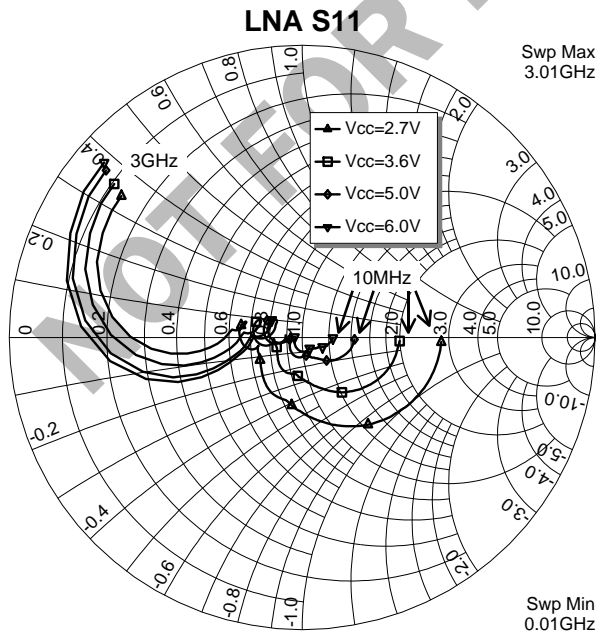
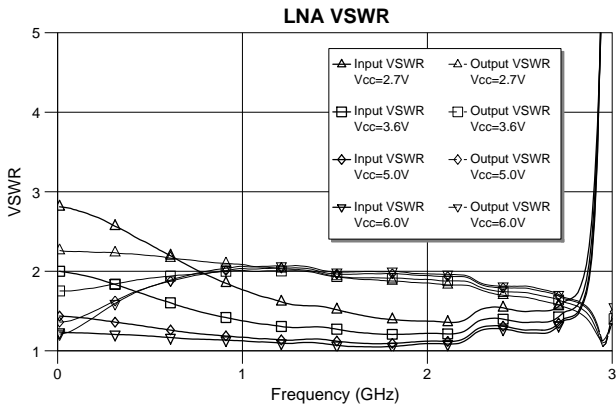
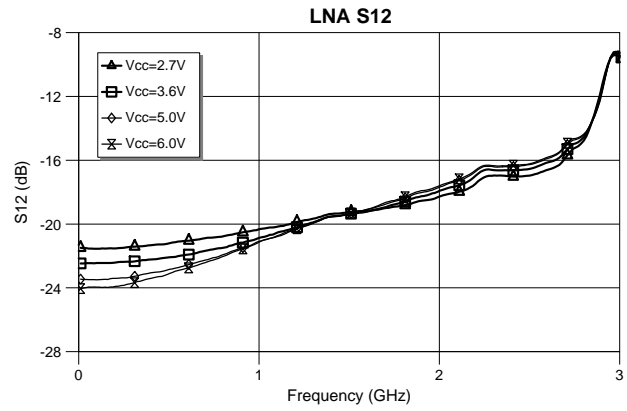
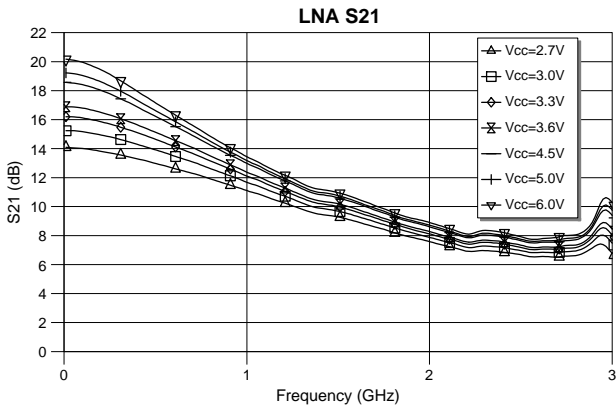
## Evaluation Board Schematic Mixer Tuned for 850MHz



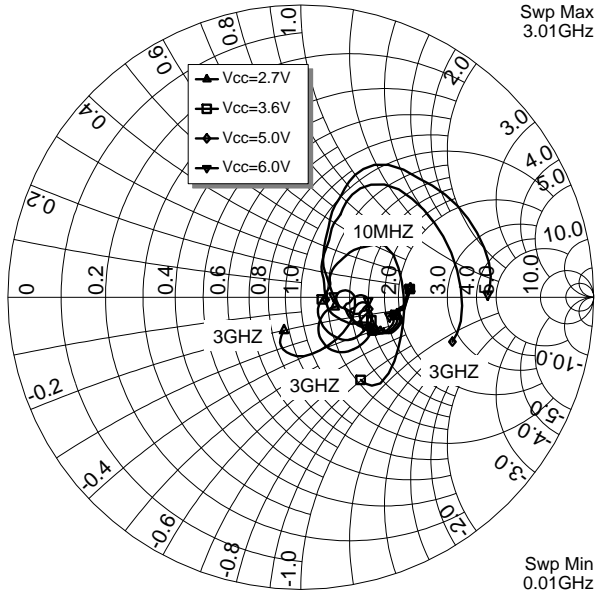
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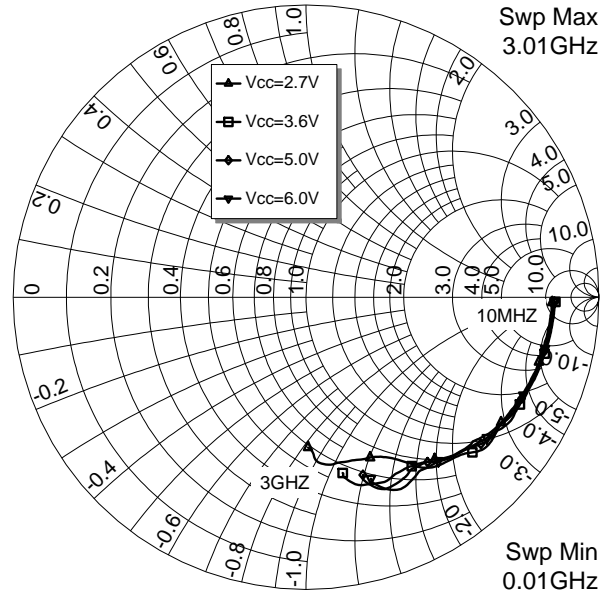




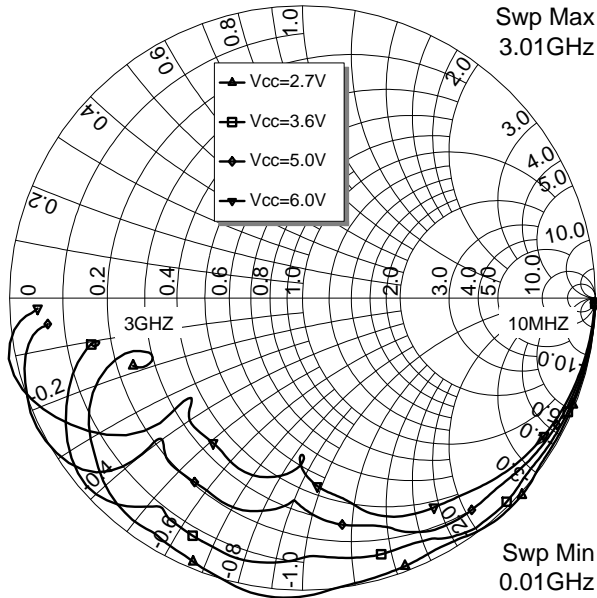
**LO Input**



**RF Input (single ended)**



**IF Output**



## RoHS\* Banned Material Content

RoHS Compliant: Yes  
 Package total weight in grams (g): 0.127  
 Compliance Date Code: 0531  
 Bill of Materials Revision: -  
 Pb Free Category: e3

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

**This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted**

\* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

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