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RF3855

3.1V LINEAR POWER AMPLIFIER

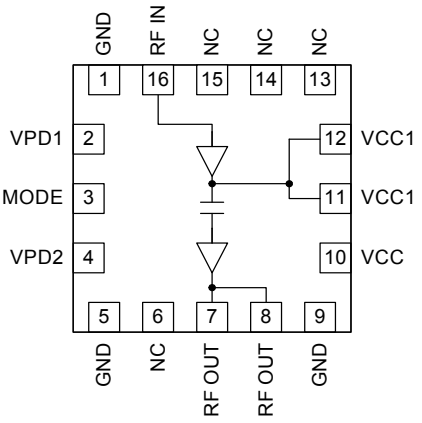
Package Style: QFN, 16-Pin, 4 x 4

Features

- Single 3.1V Supply

Applications

- L-BAND SATCOM Applications



Functional Block Diagram

Product Description

The RF3855 is a high-power, high-efficiency linear amplifier IC targeting L-BAND SATCOM Applications. The device is manufactured on an advanced Gallium Arsenide process, and has been designed for use as the final RF amplifier applications in the 1611MHz to 1618MHz band. The package is a 4mmx4mm, 16-pin QFN plastic package with backside ground.

Ordering Information

RF3855	3.1V Linear Power Amplifier

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+5.0	V_{DC}
Mode Voltage (V_{MODE})	+4.2	V_{DC}
Control Voltage (V_{REG})	+3.0	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-30 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State (V_{MODE} Low)					Case T=25°C, V_{CC}=3.1V, V_{REG}=2.90V, V_{MODE}=0V to 0.5V, Freq=1615MHz
Frequency Range	1611		1618	MHz	
Linear Gain	30	31	34	dB	
OIP3	31	34		dBm	Tone 1: 1614MHz @ +19dBm Tone 2: 1615MHz @ +19dBm
OP1dB	>22			dBm	
DC Supply					
Supply Voltage	3.0	3.1	3.6	V	
Quiescent Current	150	185	300	mA	V_{MODE}=Low=High Gain Mode
V_{REG} Current		5	10	mA	
V_{MODE} Current			1	mA	
Total Current (Power Down)			10	µA	V_{REG}=Low
V_{REG} "Low" Voltage	0		0.5	V	
V_{REG} "High" Voltage	2.75	2.85	2.95	V	
V_{MODE} "Low" Voltage	0		0.5	V	
V_{MODE} "High" Voltage	2.0		3.0	V	

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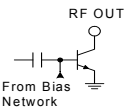
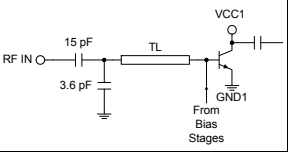
Pin	Function	Description	Interface Schematic
1	GND	This pin is internally grounded to the die flag.	
2	VREG1	Power Down control for first stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
3	MODE	For nominal operation (High Gain Mode), V_{MODE} is set LOW. When set HIGH, the driver and final are dynamically scaled to reduce the device size and as a result to reduce idle current.	
4	VREG2	Power Down control for the second stage. Regulated voltage supply for amplifier bias. In Power Down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
5	GND	Connect to ground plane via 15nH inductor. DC return for the second stage bias circuit.	
6	NC	This pin has no internal bonding; therefore, this pin can be connected to output pin 7, connected to the ground plane, or not connected. Slight tuning of the output match may be required due to stray capacitance of the pin.	
7	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the second stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1615MHz. Shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
8	RF OUT	Same as pin 7.	See pin 7.
9	GND	This pin is internally grounded to the die flag.	
10	VCC	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
11	VCC1	Power supply for first stage and interstage match. Pins 11 and 12 should be connected by a common trace where the pins contact the printed circuit board.	
12	VCC1	Same as pin 11.	
13	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
14	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
15	NC	It is recommended that these pins be connected to the ground plane for improved isolation between RF IN (pin 16) and the VCC1 pins (pins 11 and 12).	
16	RF IN	RF input. An external 15pF series capacitor is required as a DC block. In addition, the matching circuit shown is required to improve input VSWR.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

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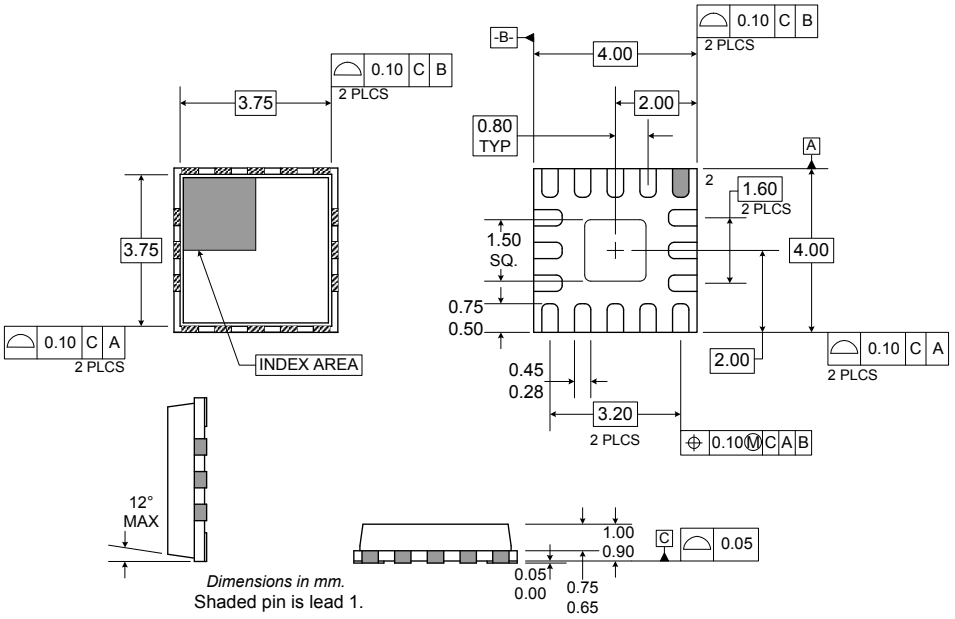
Package Drawing

Package Style: QFN, 16-Pin, 4 x 4



Dimensions in mm.
Shaded pin is lead 1.

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

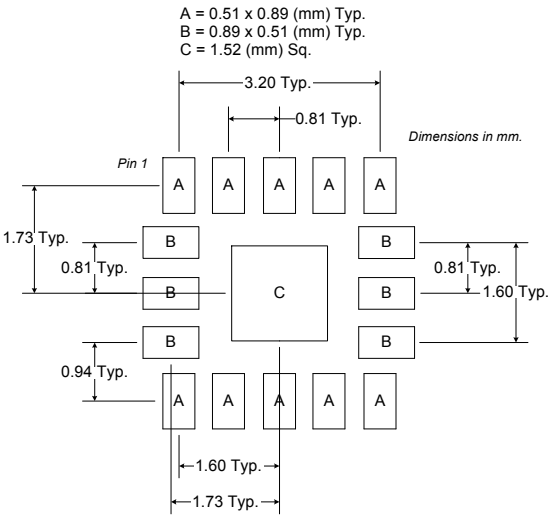


Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

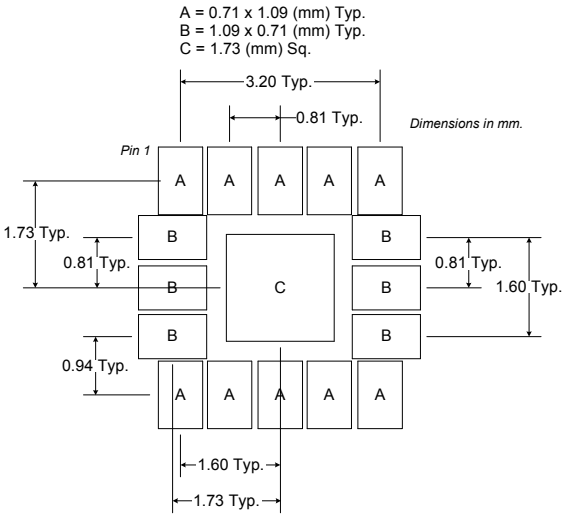

Figure 2. PCB Solder Mask (Top View)

Thermal Pad and Via Design

The PCB metal land pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.