

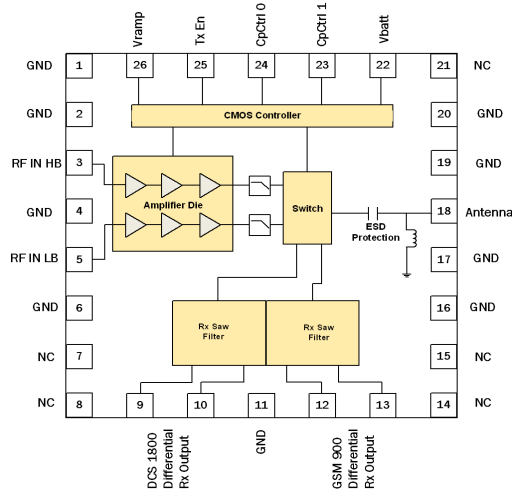


Features

- Single Module Placement (SMPL)
- Proven PowerStar® Architecture
- Integrated RX SAW Filters
- Integrated Power Flattening Circuit
- Integrated V_{RAMP} Filter
- No External Routing Simplifies Layout
- Differential RX Ports Allow Layout Flexibility
- Robust 8kV ESD Protection at Antenna Port
- V_{BATT} Tracking

Applications

- 3V Quad-Band GSM/GPRS Handsets
- EGSM900/DCS1800 Products
- GPRS Class 12 Compliant
- Portable Battery-Powered Equipment



Functional Block Diagram

Product Description

The RF7177 is a dual-band (EGSM900/DCS1800) GSM/GPRS Class 12 compliant Transmit Module with integrated Receive SAW Filters. This transmit module is the next step of integration to include a multi function CMOS controller, GaAs HBT power amplifier, pHEMT front-end antenna switch and RX SAW filters all in one package for a true single front end solution. The two RX ports are 150Ω impedance and provide a differential output to allow flexibility when interfacing with various transceiver configurations. The RF7177 continues to build upon RFMD's leading patented PowerStar® Architecture to include such features as Power Flattening Circuit, V_{RAMP} Filtering, and V_{BATT} Tracking. The highly integrated transmit module simplifies the phone design by eliminating the need for complicated control loop design, output RF spectrum, (ORFS) optimization, harmonic filtering, and component matching, all of which combine to provide best in class RF performance, solution size, and ease of implementation for cellular phone systems. The TX RF ports are 50Ω matched and the antenna port includes ESD protection circuitry which meets the stringent 8kV industry standards requiring no additional components. All of these eliminated factors help to improve the customer's product time to market.

Ordering Information

RF7177	Dual-Band EGSM900/DCS1800 TxM with Integrated Receive SAW Filters
RF7177SB	Transmit Module 5-Piece Sample Pack
RF7177PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

- | | | | |
|--|--------------------------------------|--|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input checked="" type="checkbox"/> Si CMOS | <input type="checkbox"/> RF MEMS |
| <input type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LDMOS |

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0	V
Power Control Voltage (V_{RAMP})	-0.3 to +1.8	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Output Load VSWR	20:1	
Operating Case Temperature	-20 to +85	°C
Storage Temperature	-55 to +150	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
ESD					
ESD: All Pins Excluding RX SAW Pins			1000	V	HBM, JESD22-A114
ESD: All Pins			200	V	HBM, JESD22-A114
ESD: All Pins Excluding RX SAW Pins			1000	V	CDM, JEDEC JESD22-C101
ESD: All Pins			500	V	CDM, JEDEC JESD22-C101
ESD: Antenna Port			8	kV	IEC 61000-4-2
Overall Power Control V_{RAMP}					
Power Control "ON"			1.8	V	Max. P_{OUT}
Power Control "OFF"		0.25		V	Min. P_{OUT}
V_{RAMP} Input Capacitance		15	20	pF	DC to 200kHz
V_{RAMP} Input Current			10	μ A	$V_{RAMP} = V_{RAMP, MAX}$
Power Control Range		50		dB	$V_{RAMP} = 0.25V$ to $V_{RAMP, MAX}$
Overall Power Supply					
Power Supply Voltage	3.0	3.5	4.8	V	Operating Limits
Power Supply Current		1	20	μ A	$P_{IN} < -30dBm$, TX Enable = Low, $V_{RAMP} = 0.25V$, Temp = -20 °C to +85 °C, $V_{BATT} = 4.8V$.
Overall Control Signals					
GpCtrlIO/1 "Low"	0	0	0.5	V	
GpCtrlIO/1 "High"	1.25	2.0	3.0	V	
GpCtrlIO/1 "High Current"		1	2	μ A	
TX Enable "Low"	0	0	0.5	V	
TX Enable "High"	1.25	2.0	3.0	V	
TX Enable "High Current"		1	2	μ A	
RF Port Input and Output Impedance		50		Ω	
Differential RX Output Impedance		150		Ω	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM900 Band					Nominal conditions unless otherwise stated. All unused ports are terminated. $V_{BATT}=3.5V$, $P_{IN}=3dBm$, Temp = +25 °C, TX Enable=High, $V_{RAMP}=1.8V$. TX Mode: GpCtrl1=High, GpCtrl0=Low, Duty Cycle=25%, Pulse Width = 1154 μ S
Operating Frequency Range	880		915	MHz	
Input Power	0	3	6	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (5dBm to 33dBm).
Maximum Output Power	33	33.7		dBm	Nominal conditions.
	31	33.7		dBm	$V_{BATT}=3.1V$ to 4.8V, $P_{IN}=0dBm$ to 6dBm, Temp = -20 °C to +85 °C, Duty Cycle=50%, Pulse Width = 2308mS, $V_{RAMP}\leq 1.8V$.
Minimum Power Into 3:1 VSWR	30	31.5		dBm	The measured delivered output power to the load with the mismatch loss already taken into account with 1dB variation margin. $V_{BATT}=3.5V$.
Efficiency	36	40		%	Set $V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$
2nd Harmonic		-40*	-33	dBm	$V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$. *Typical value measured from worst case harmonic frequency across the band.
3rd Harmonic		-40*	-33	dBm	$V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$. *Typical value measured from worst case harmonic frequency across the band.
7th Harmonic		-36	-28	dBm	$V_{RAMP}=V_{RAMP\ RATED}$. *Typical value measured from worst case harmonic frequency across the band. External low pass filter can be used to attenuate the higher order harmonics. (See Application Schematic for suggested filter.)
All other harmonics up to 12.75GHz		-40	-33	dBm	$V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$.
Non-harmonic Spurious up to 12.75GHz			-36	dBm	$V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$, also over all power levels (5dBm to 33dBm).
Forward Isolation 1		-60	-41	dBm	TX Enable Low, $P_{IN}=6dBm$, $V_{RAMP}=0.25V$.
Forward Isolation 2		-27	-15	dBm	TX Enable High, $P_{IN}=6dBm$, $V_{RAMP}=0.25V$.
Output Noise Power		-86	-77	dBm	925 MHz to 935 MHz. $V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$, RBW = 100 kHz.
		-86	-83	dBm	935 MHz to 960 MHz. $V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$, RBW = 100 kHz.
		-118	-87	dBm	1805 MHz to 1880 MHz. $V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}=33dBm$, RBW = 100 kHz.
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR = 12:1, all phase angles (Set $V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}\leq 33dBm$ into 50 Ω load; load switched to VSWR=12:1).
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR = 20:1, all phase angles (Set $V_{RAMP}=V_{RAMP\ RATED}$ for $P_{OUT}\leq 33dBm$ into 50 Ω load; load switched to VSWR=20:1).

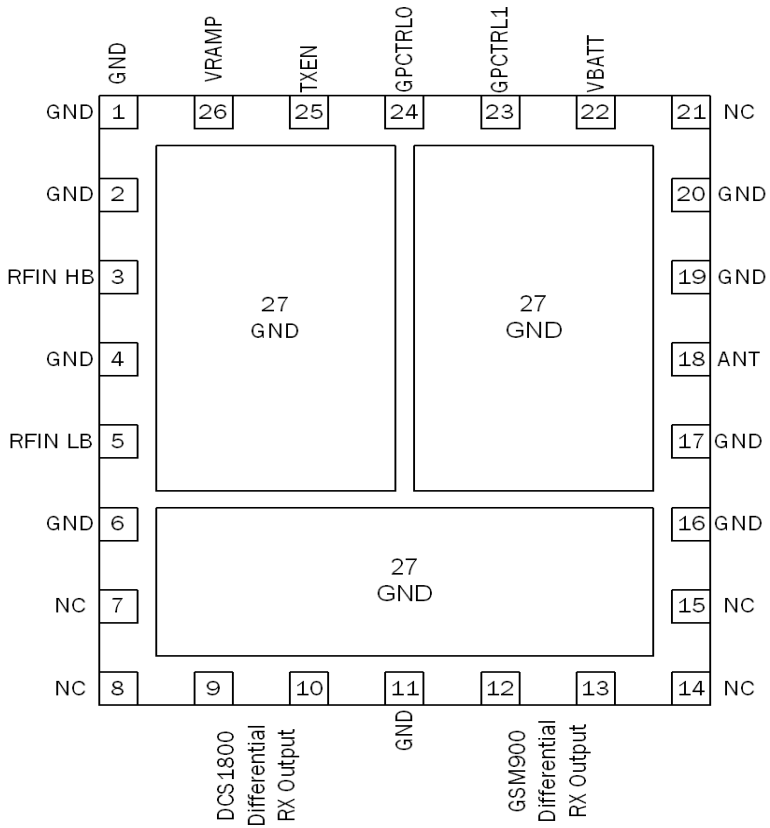
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS1800 Band					Nominal conditions unless otherwise stated. All unused ports are terminated. $V_{BATT}=3.5V$, $P_{IN}=3dBm$, Temp= $+25^{\circ}C$, TX Enable=High, $V_{RAMP}=1.8V$, TX Mode: GpCtrl1=High, GpCtrl0=High, Duty Cycle=25%, Pulse Width=1154 μS
Operating Frequency Range	1710		1785	MHz	
Input Power	0	3	6	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		1.3:1	2.5:1		Over P_{OUT} range (0dBm to 30dBm).
Maximum Output Power	30	31.5		dBm	Nominal conditions.
	28	31.5		dBm	$V_{BATT}=3.0V$ to 4.8V, $P_{IN}=0dBm$ to 6dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$, Duty Cycle=50%, Pulse Width=2308mS, $V_{RAMP}\leq 1.8V$.
Minimum Power Into 3:1 VSWR	27	28.5		dBm	The measured delivered output power to the load with the mismatch loss already taken into account with 1dB variation margin. $V_{BATT}=3.5V$.
Efficiency	32	34		%	Set $V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=30dBm$
2nd Harmonic		-40*	-33	dBm	$V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=30dBm$. *Typical value measured from worst case harmonic frequency across the band.
3rd Harmonic		-40*	-33	dBm	$V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=30dBm$. *Typical value measured from worst case harmonic frequency across the band.
4th Harmonic		-36*	-28	dBm	$V_{RAMP}=V_{RAMP RATED}$. *Typical value measured from worst case harmonic frequency across the band. External low pass filter can be used to attenuate the higher order harmonics. (See Application Schematic for suggested filter.)
All other harmonics up to 12.75GHz		-40	-33	dBm	$V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=30dBm$.
Non-harmonic Spurious up to 12.75GHz			-36	dBm	$V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=30dBm$, also over all power levels (5 dBm to 33dBm).
Forward Isolation 1		-62	-53	dBm	TX Enable Low, $P_{IN}=6dBm$, $V_{RAMP}=0.25V$.
Forward Isolation 2		-27	-15	dBm	TX Enable High, $P_{IN}=6dBm$, $V_{RAMP}=0.25V$.
Output Noise Power		-101	-77	dBm	925 MHz to 935 MHz. $V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=33dBm$, RBW=100 kHz.
		-100	-83	dBm	935 MHz to 960 MHz. $V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=33dBm$, RBW=100 kHz.
		-93	-79	dBm	1805 MHz to 1880 MHz. $V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}=33dBm$, RBW=100 kHz.
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=12:1, all phase angles (Set $V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}\leq 30dBm$ into 50 Ω load; load switched to VSWR=12:1).
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1, all phase angles (Set $V_{RAMP}=V_{RAMP RATED}$ for $P_{OUT}\leq 30dBm$ into 50 Ω load; load switched to VSWR=20:1).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX Section					All parameters tested to Nominal Conditions unless otherwise stated. V _{BATT} =3.5V, P _{IN} =3dBm, Temp=+25°C. TXEN=High, V _{RAMP} =Low (0.25V) See logic table for RX State. Duty Cycle=25%, Pulse Width=1154µs.
EGSM900					RX Freq=925MHz to 960MHz
VSWR		2.5:1	3.0:1	dB	
Insertion Loss		2.7	3.4	dB	Nominal Conditions: see above.
			4	dB	Extreme Conditions: V _{BATT} =3.0V to 4.8V, Temp=-20°C to 85°C, P _{IN} =0dBm to 6dBm
Pass Band Ripple		0.5	1.0	dB	
Phase Balance	-10		+10	°	
Amplitude Balance	-1		+1	dB	
Attenuation	40	60		dB	Freq=0MHz to 880MHz
	30	60		dB	Freq=880MHz to 905MHz
	20	30		dB	Freq=905MHz to 915MHz
	25	30		dB	Freq=980MHz to 1025MHz
	33	45		dB	Freq=1025MHz to 2880MHz
	25	50		dB	Freq=2880MHz to 6000MHz
	25	40		dB	Freq=6GHz to 12.75GHz
DCS1800					RX Freq=1805MHz to 1880MHz
VSWR		2.5:1	3.0:1	dB	
Insertion Loss		2.8	3.5	dB	Nominal Conditions: see above.
			4.0	dB	Extreme Conditions: V _{BATT} =3.0V to 4.8V, Temp=-20°C to 85°C, P _{IN} =0dBm to 6dBm
Pass Band Ripple		0.5	1.0	dB	
Phase Balance	-12		+12	dB	
Amplitude Balance	-1.5		+1.5	dB	
Attenuation	35	40		dB	Freq=0MHz to 1300MHz
	25	35		dB	Freq=1300MHz to 1705MHz
	13	18		dB	Freq=1705MHz to 1785MHz
	19	25		dB	Freq=1920MHz to 1980MHz
	20	30		dB	Freq=1980MHz to 3000MHz
	25	45		dB	Freq=3000MHz to 5000MHz
	20	45		dB	Freq=5000MHz to 6000MHz
	20	40		dB	Freq=6GHz to 12.75GHz

TX ENABLE	GpCtrl1	GpCtrl0	TX Module Mode
0	0	0	Low Power Mode (Standby)
0	1	0	RX DCS1800
0	1	1	RX EGSM900
1	1	0	EGSM900 TX Mode
1	1	1	DCS1800 TX Mode

Pin	Function	Description
1	GND	Ground.
2	GND	Ground.
3	RF IN HB	RF input to the EGSM900 band.
4	GND	Ground.
5	RF IN LB	RF input to the DCS1800 band.
6	GND	Ground.
7	NC	No connection.
8	NC	No connection.
9	DCS1800	Differential RX output.
10	DCS1800	Differential RX output.
11	GND	Ground.
12	GSM900	Differential RX output.
13	GSM900	Differential RX output.
14	NC	No connection.
15	NC	No connection.
16	GND	Ground.
17	GND	Ground.
18	ANTENNA	RF Output to Antenna.
19	GND	Ground.
20	GND	Ground.
21	NC	No connection.
22	VBATT	Power Supply for the module.
23	CPCTRL 1	Logic Control Pin, refer to logic table for mode of operation.
24	CPCTRL 0	Logic Control Pin, refer to logic table for mode of operation.
25	TX EN	PA transmit enable signal, refer to logic table for mode of operation.
26	VRAMP	Power control voltage from the baseband DAC.

Pin Out



Theory of Operation

Overview

The RF7177 is a dual band (EGSM900/DCS1800) GSM/GPRS Transmit Module with integrated Receive SAW Filters.

This transmit module is the next step of integration adding the receive SAW Filters along with a multi function CMOS controller, GaAs HBT power amplifier, pHEMT front end antenna switch all in one package for a true single front end solution. The integrated RX SAW filters further simplify the phone design by eliminating the need for additional component placements and circuit matching.

The RF7177 continues to build upon RFMD's leading patented PowerStar® Architecture to include such features as Power Flattening Circuit, V_{RAMP} Filtering, and V_{BATT} Tracking. The integrated power control loop can be driven directly from the baseband DAC to provide a very predictable power output which enables handset manufacturers to achieve simple and efficient phone calibration in production.

Features

Power Flattening Circuit

When a mismatch is presented to the antenna of the phone, the output impedance presented to the PA also varies resulting in variation of output power and current. This can compromise the PA's ability to maintain the minimum output power required for calls and to limit the total radiated power (TRP), to meet the requirements of governmental agencies and cellular service providers.

The PFC sets a reference voltage into 50 ohms and the feedback loops corrects for impedance variation reducing the power and current variation into mismatch conditions.

V_{RAMP} Filtering:

The Vramp control voltage is received from the Baseband DAC. The DAC signal is usually in the form of a staircase waveform related to the DAC bit resolution and the timing of the power steps. The staircase waveform usually requires some filtering to smooth out the waveform and reduce any unwanted spectral components showing up in the switching spectra of the RF output signal. A simple RC filter maybe integrated into the Baseband, Transmit module or with discrete component between the two.

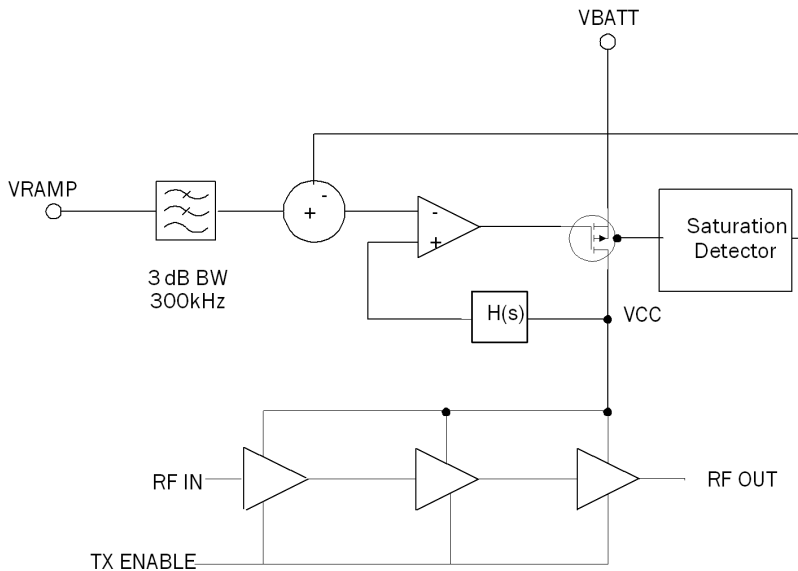
V_{BATT} Tracking / Vramp Limiter

This circuit monitors the relationship of the battery voltage and V_{RAMP}/V_{CC} used to control the PA. At low V_{BATT} levels the FET pass-device which controls V_{CC} can enter into a saturation region which can increase switching transients. The saturation detection circuit automatically monitors the battery voltage and produces a correction so that V_{RAMP} is reduced, thus preventing the power control loop from reaching saturation and inducing switching transients.

Mode of Operation: Saturated GMSK

In GSM mode, the GMSK modulation is a constant envelope and the useful data is entirely included in the phase of the signal. Since the constant envelope is not sensitive to amplitude non-linearities caused by the PA, the amplifier can operate in saturation mode (deep class AB or class C) for optimum efficiency. The basic circuit diagram is shown in the Figure 2.

The control circuit receives a DAC voltage (V_{RAMP}) to set the required output power for the phone. The PowerStar I architectures multiplies the V_{RAMP} voltage level and regulates it at the collector (V_{CC}) of all three stages of the amplifier, holding the stages in saturation. The base bias is fixed at a point that is at least deep class AB or class C. By holding the PA in saturation, performance sensitivity is essentially eliminated to temperature, frequency, voltage and input drive level ensuring robust performance within the ETSI power vs time mask.



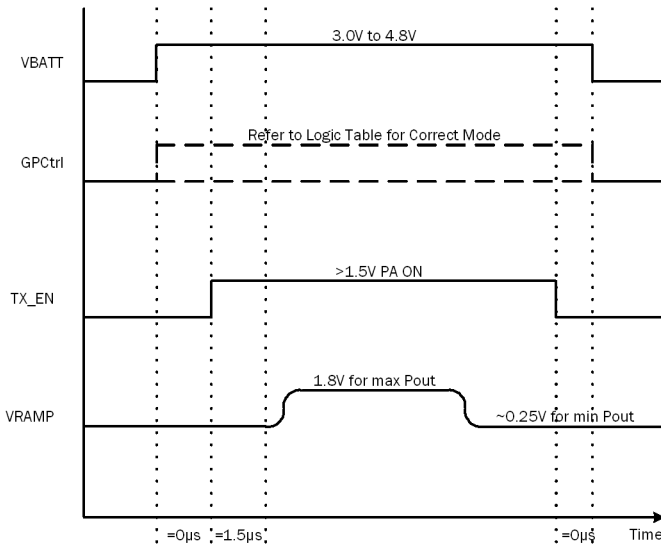
The regulation of power is demonstrated in Equation 1. The equation shows that load impedance affects output power, but to a lesser degree than the V_{CC} supply variations. Since the architecture regulates V_{CC} , the dominant cause of power variation is eliminated. The control loop provides a very linear relationship between V_{RAMP} and P_{OUT} .

$$P_{OUT_{dBm}} = 10 \log \frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R_L \cdot 10^{-3}}$$

The RF signal applied at the RFIN pin must be a constant amplitude signal and should be high enough to saturate the amplifier in the GSM mode. The input power (P_{IN}) range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier and will increase the minimum output power.

Power On (Timing) Sequence

In the Power-On Sequence, there are some important set-up times associated with the control signals of the TxM. Refer to the logic table for control signal functions. One of the critical relationships is the settling time between TXEN going high and when V_{RAMP} can begin to increase. This time is often referred to as the "pedestal" and is required so that the internal power control loop and bias circuitry can settle after being turned on. The PowerStar® architecture usually requires approximately 1 - 2 μ s for proper settling of the power control loop.



GMSK Power On Sequence:

1. Apply VBATT
2. Apply GPCtrl
3. Apply minimum VRAMP ($\sim 0.25V$)
4. Apply TX_EN
5. Apply VRAMP for desired output power

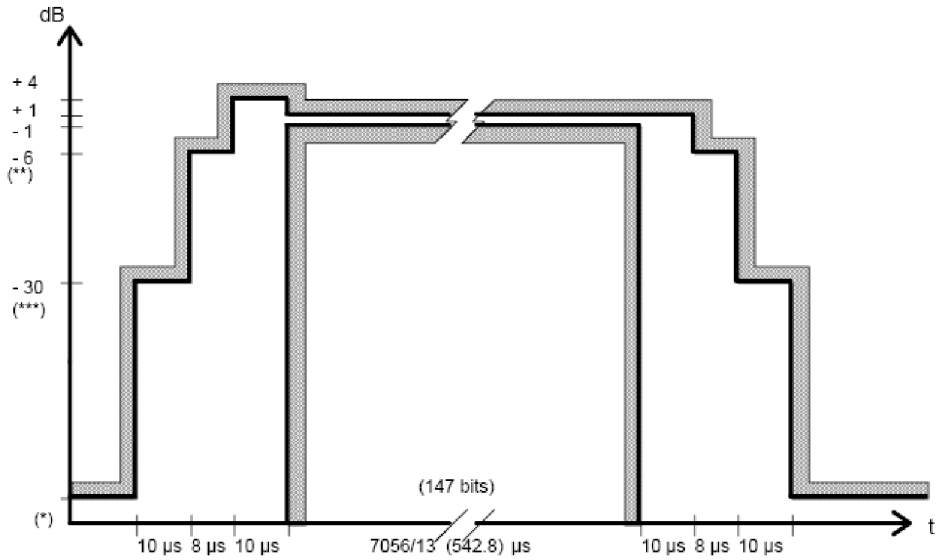
RFIN can be applied at any time. For good transient response it must be applied before power ramp begins.

The Power Down Sequence is the reverse order of the Power On Sequence.

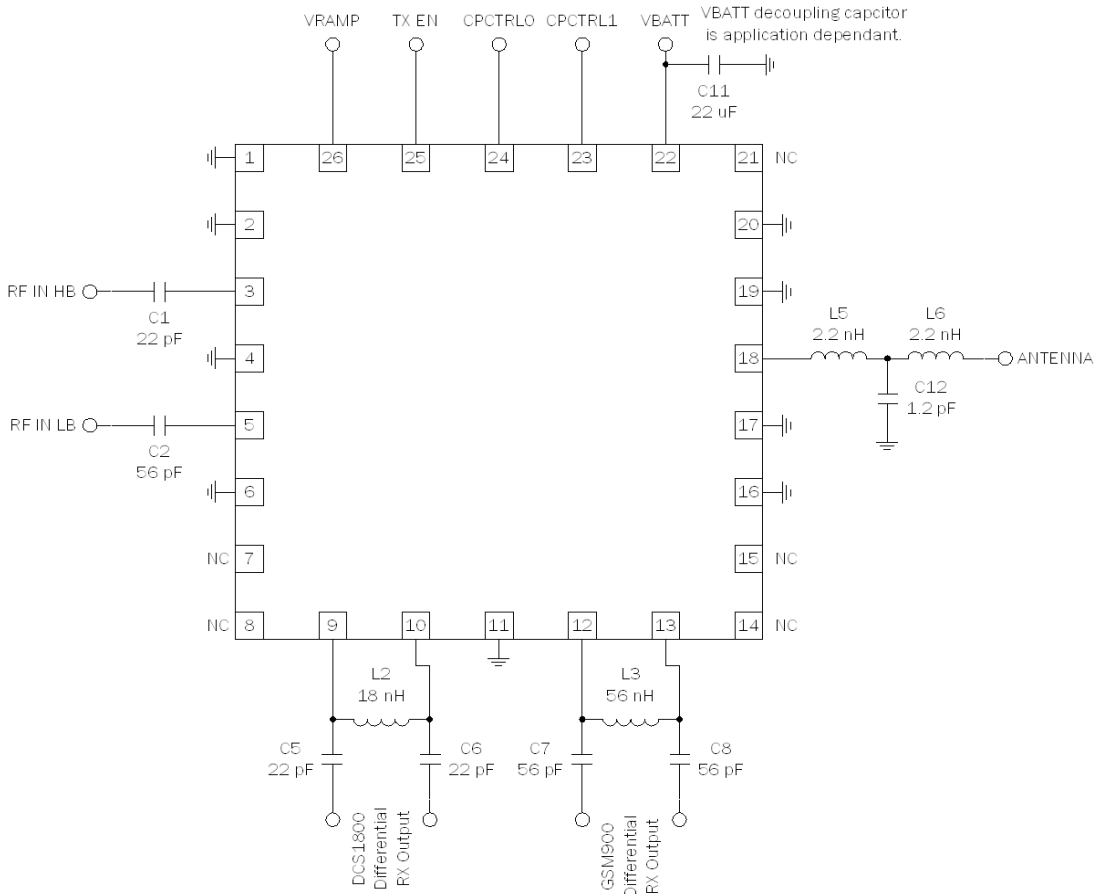
Power Ramping

The V_{RAMP} waveform must be created such that the output power falls into the ETSI power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus V_{RAMP} response of the power amplifier. The PowerStar® control loop is very capable of meeting switching transient requirements with the proper raised cosine waveform applied to the V_{RAMP} input. Ramps usually fall within the 12 - 14 μ s time to control switching transients at high power levels. Faster ramps usually have a steeper transition creating higher transients. Slower ramps may have difficulty meeting the time mask. Optimization needs to include all power levels as the time mask requirements change with P_{OUT} levels.

The diagram below is the ETSI time mask for a single GSM timeslot.



Application Schematic



Notes:

RF LB/HB inputs and antenna output traces are 50Ω impedance.

RX ports are differential pairs of 150Ω impedance.

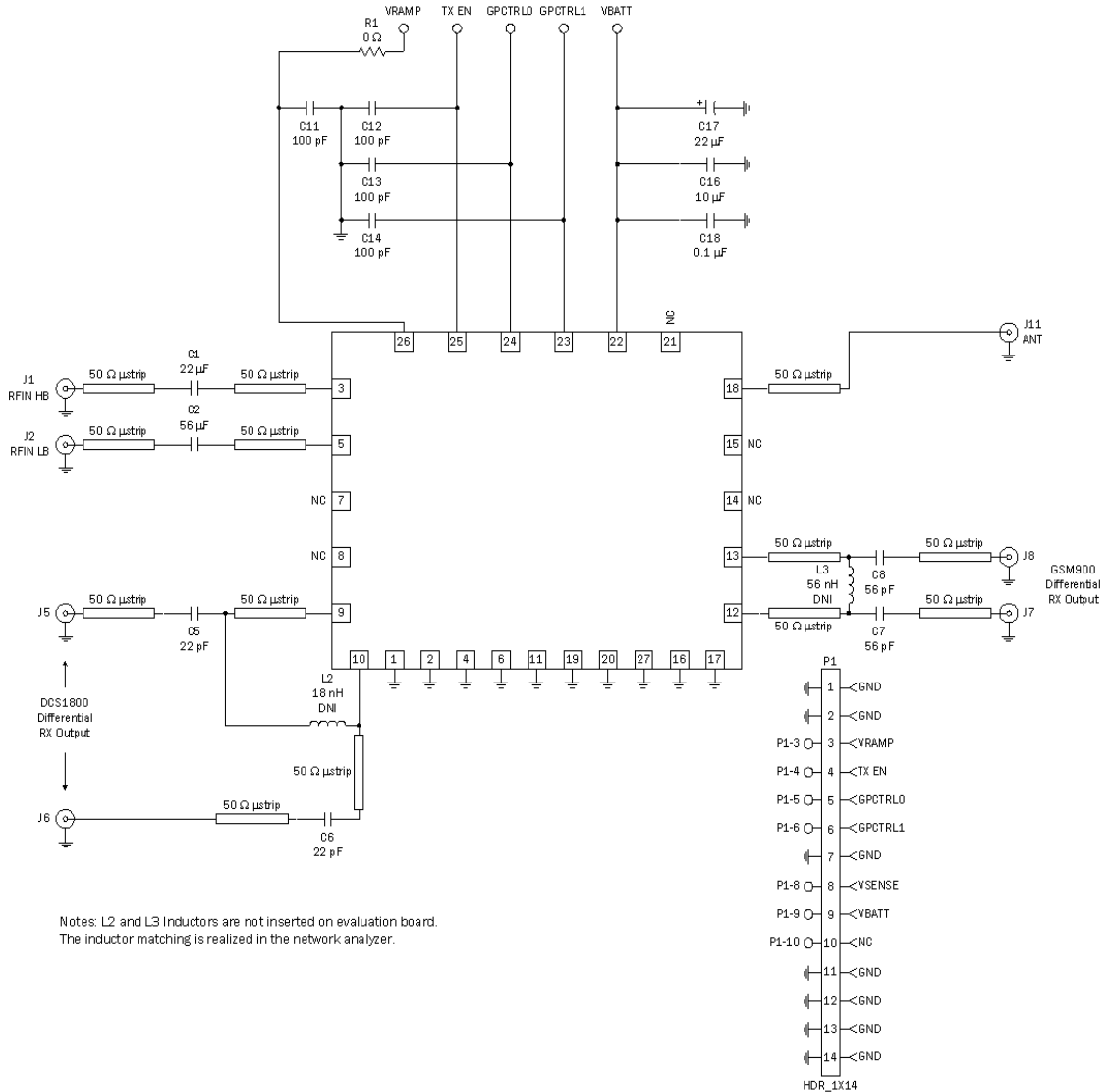
VBATT capacitor value may change depending on application.

The values listed for the RX differential port matching are suggested values only and may require optimization depending on application and phone board circuitry.

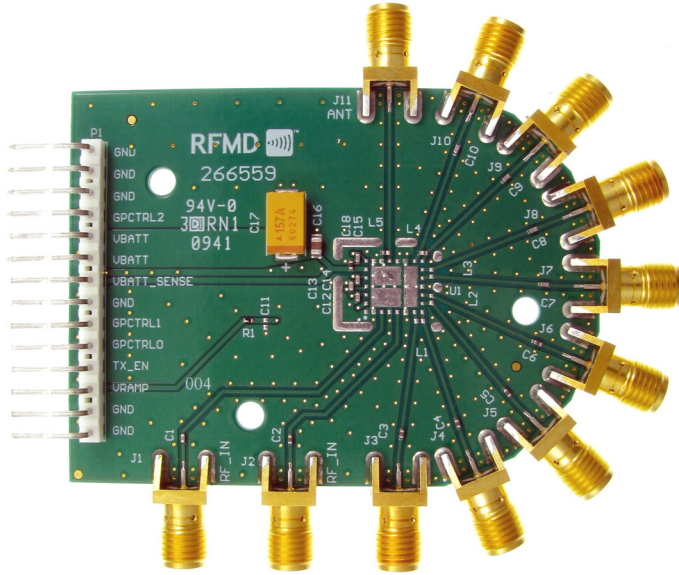
If placing an attenuation network on the input to the power amplifier, ensure that it is positioned on the transceiver side of the capacitor C1 (or C2) to prevent adversely affecting the base biasing of the power amplifier.

For control of higher order HB harmonics, a low-pass filter is required on the ANT output. The values listed in this application schematic are suggested only and depend on the particular application, as they are heavily dependent on the phone circuit layout.

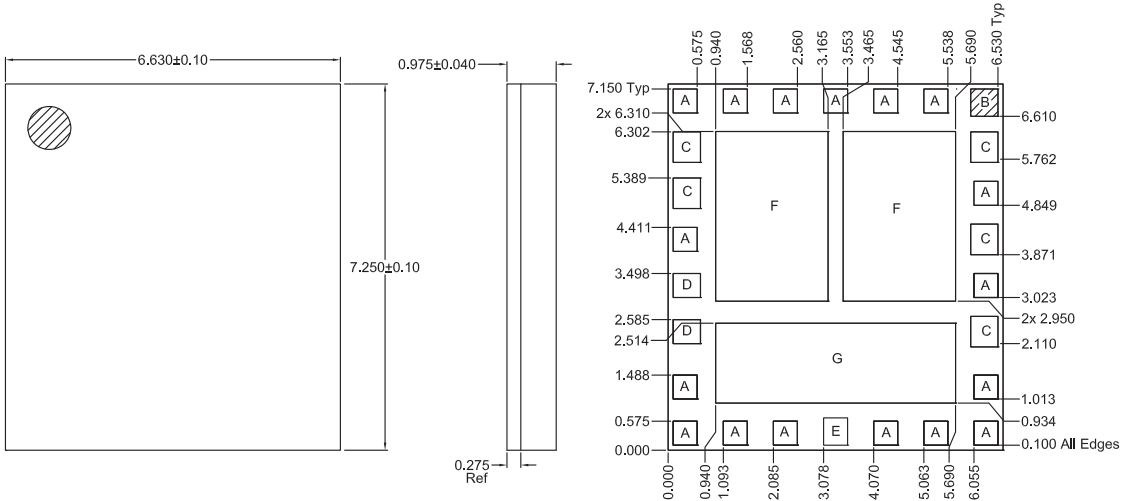
Evaluation Board Schematic



Evaluation Board Layout



Package Drawing



Notes:

1. Shaded area represents Pin 1 location

- A = 0.475 mm Sq Typ
- B = 0.540 mm Sq Typ
- C = 0.540 x 0.605 mm Typ
- D = 0.540 x 0.475 mm
- E = 0.475 x 0.540 mm
- F = 2.225 x 3.360 mm Typ
- G = 4.750 x 1.580 mm

YY indicates year, WW indicates work week, and Trace Code is a sequential number assigned at device assembly.

PCB Design Requirements

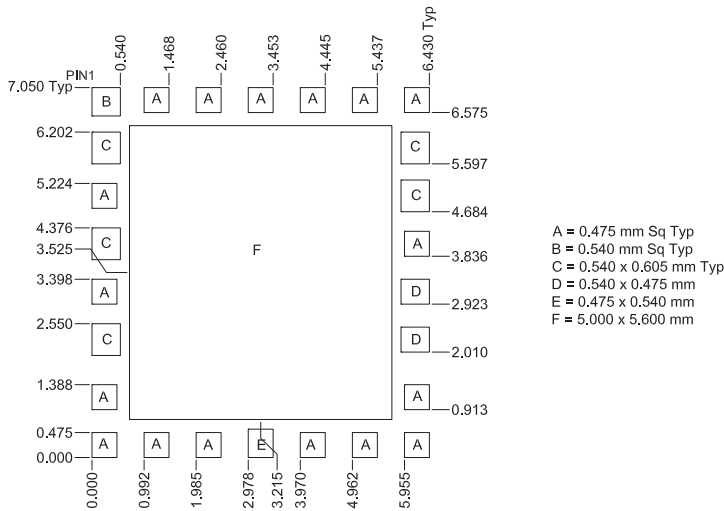
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

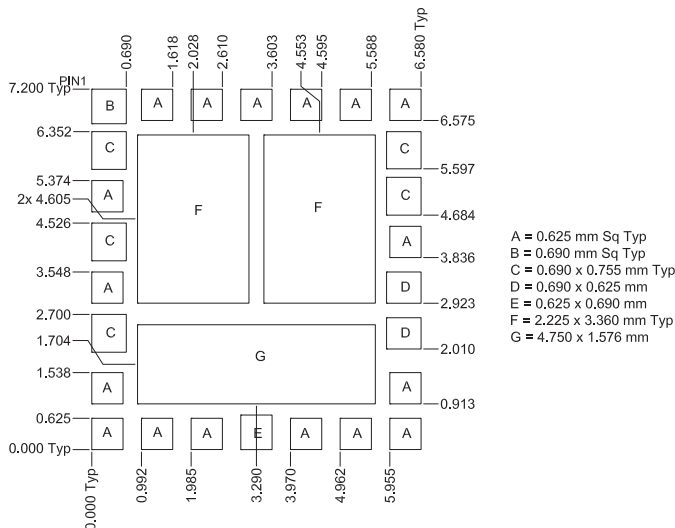
PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

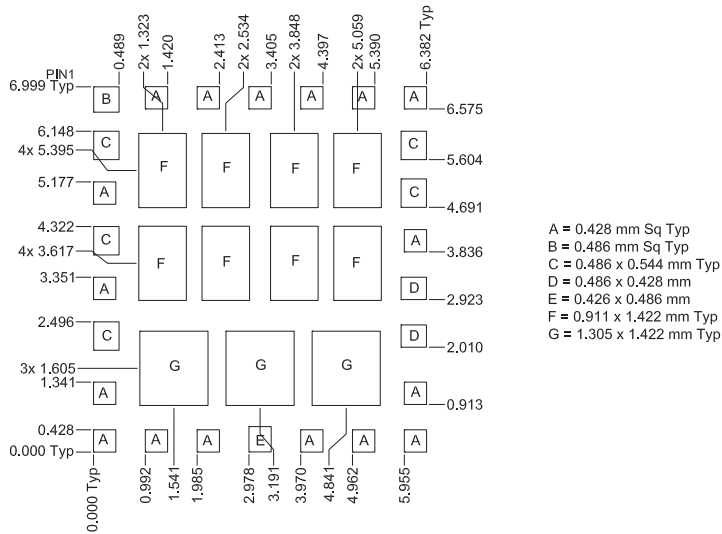
PCB Metal Land



Solder Mask Pattern



Stencil Pattern



Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125 °C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF7178TR13	13 (330)	4 (102)	16	8	Single	2500
RF7178TR7	7 (178)	2.4 (61)	12	8	Single	750

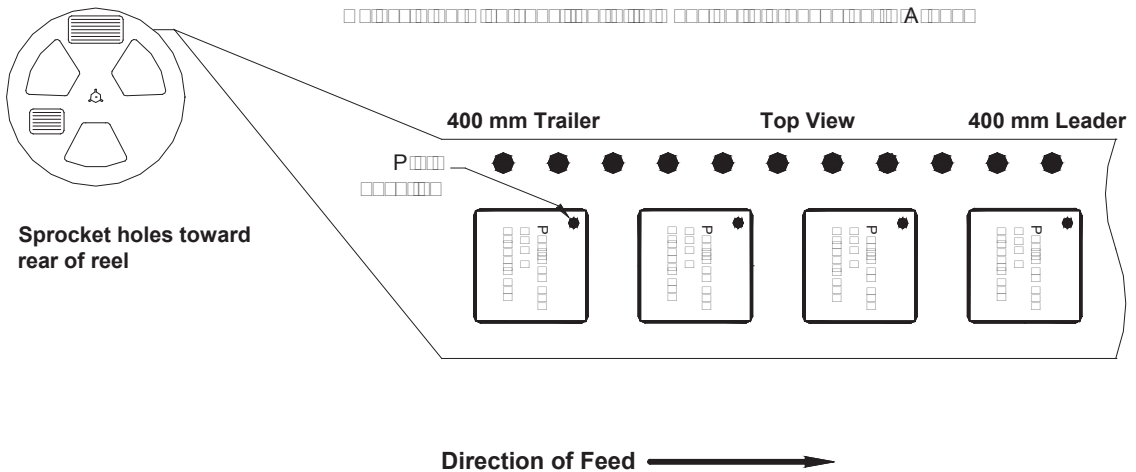


Figure 1. 6.63mmx7.25mmx1.0mm (Carrier Tape Drawing with Part Orientation)

RoHS* Banned Material Content

RoHS Compliant: Yes
 Package total weight in grams (g): 0.121
 Compliance Date Code: -
 Bill of Materials Revision: -
 Pb Free Category: e4

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment

