



**Package Style: Laminate, 24-Pin, 5mm x 5mm x 1mm**

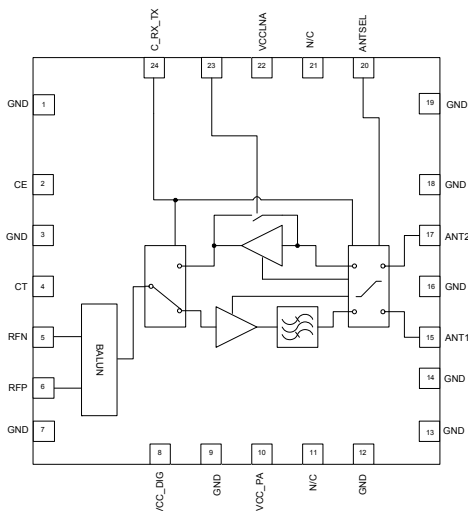


## Features

- Tx Output Power=23dBm
- Integrated RF Front End Module with Balun, PA, filter, LNA with Bypass mode and DP2T switch.
- Single Bidirectional Differential Transceiver interface.
- Voltage range=2.0 to 3.6V.

## Applications

- ZigBee® 802.15.4 Based Systems for Remote Monitoring and Control
- 2.4GHz ISM Band Applications
- AA Battery Operation
- Smart Meters for Energy Management



Functional Block Diagram

## Product Description

The RFFM6201 integrates a complete solution in a single Front End Module (FEM) for WiFi and ZigBee applications in the 2.4GHz band. This FEM integrates the PA plus harmonic filter in the transmit path. The RFFM6201 also integrates a Low Noise Amplifier (LNA) with bypass mode and a balun. The RFFM6201 provides a single balanced TDD access for Rx and Tx paths along with two ports on the output for connecting a diversity solution or a test port. The device is provided in a 5mm x 5mm x 1mm, 24 pin laminate package.

## Ordering Information

RFFM6201	3.3V Front End Module for AMR systems in the 2.4GHz to 2.5GHz Band
RFFM6201SQ	Standard 25 piece bag
RFFM6201SR	Standard 100 piece reel
RFFM6201TR13	Standard 2500 piece reel
RFFM6201PCK-410	Fully assembled evaluation board and 5 loose pieces

## Optimum Technology Matching® Applied

<input type="checkbox"/> GaAs HBT	<input type="checkbox"/> SiGe BiCMOS	<input checked="" type="checkbox"/> GaAs pHEMT	<input type="checkbox"/> GaN HEMT
<input type="checkbox"/> GaAs MESFET	<input type="checkbox"/> Si BiCMOS	<input type="checkbox"/> Si CMOS	<input type="checkbox"/> BIFET HBT
<input checked="" type="checkbox"/> InGaP HBT	<input type="checkbox"/> SiGe HBT	<input type="checkbox"/> Si BJT	<input type="checkbox"/> LDMOS

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## Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	5.0	V
DC Supply Current	300	mA
Maximum Tx Input Power	+5	dBm
Maximum Rx Input Power	+5	dBm
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
ESD, HBM RF Pins	1000	V
ESD, HBM All Other Pins	500	V
ESD, CDM All Pins	500	V
MSL	MSL3	

**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Conditions</b>					Specifications must be met across supply voltage, control voltage, and temperature ranges unless otherwise specified.
V <sub>BATT</sub>	2	3.3	3.6	V	
Full operating temp range	-40	25	85	°C	
Z <sub>0</sub>		50		Ω	
Off mode current (All controls LOW)		0.5	1	μA	
Current sourced through CT pin			18	mA	
Voltage drop from CT pin to RFN/RFP			0.1	V	
<b>Tx Path</b>					
Frequency	2405		2480	MHz	
Input Return Loss	10			dB	
Balanced input impedance		100		Ω	
Amplitude Imbalance	-1		1	dB	
Phase Imbalance	-15		15	deg	
Output Return Loss	10			dB	
Transmit Path Gain	22	25		dB	At rated power
Gain flatness	-0.8		0.8	dB	
Rated Output Power		23		dBm	Nominal Conditions (V <sub>BATT</sub> = 3.3V, 25 °C)
	22				V <sub>BATT</sub> = 3.0V to 3.6V, all conditions
	20			dBm	V <sub>BATT</sub> to 2.7V, all temperatures
	18			dBm	V <sub>BATT</sub> to 2.0V, all temperatures
Supply current		170	190	mA	At rated power, nominal conditions (V <sub>BATT</sub> = 3.3V, 25 °C), 802.15.4 QPSK
		180	200	mA	At rated power, 3.0V to 3.6V, all conditions, 802.15.4 QPSK
Thermal Resistance		TBD		°C/W	3.6V <sub>CC</sub> ; P <sub>OUT</sub> = 23dBm; Control Voltage = V <sub>CC</sub> -0.2V; T <sub>REF</sub> = 85 °C

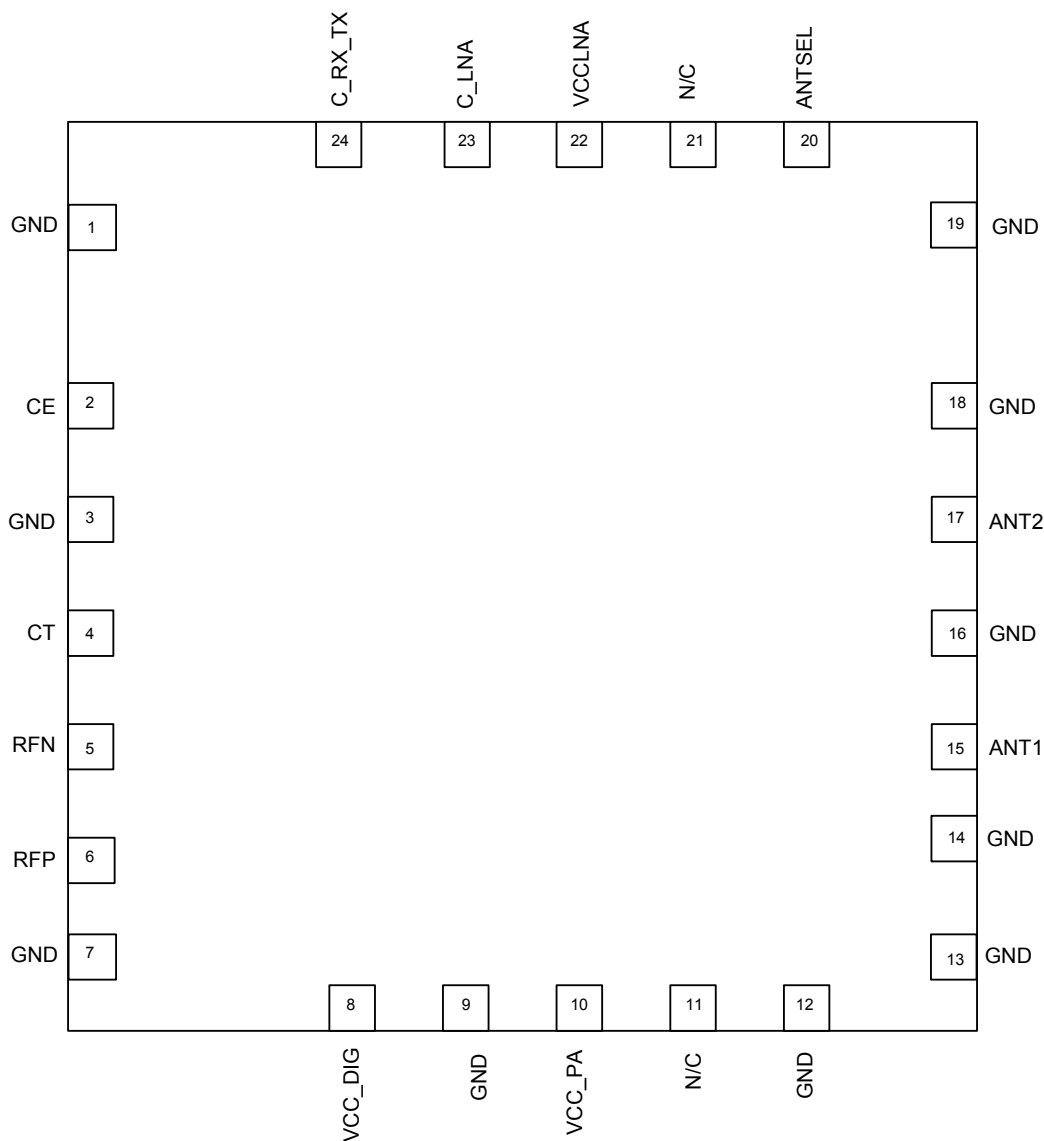
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Tx Path (continued)					
2nd harmonic level		-45	-42	dBm/MHz	At rated power, 802.15.04 OQPSK
3rd harmonic level		-45	-42	dBm/MHz	At rated power, 802.15.04 OQPSK
4rd harmonic level		-45	-42	dBm/MHz	At rated power, 802.15.04 OQPSK
5th harmonic level		-45	-42	dBm/MHz	At rated power, 802.15.04 OQPSK
VSWR Stability and load mismatch susceptibility	4:1				
VSWR No damage	8:1				
Gain settling time		1	10	μS	
Amplitude imbalance	-1		1	dB	
Phase imbalance	-15		15	deg	
Rx Path to LNA Mode					
Frequency	2405		2480	MHz	
Gain	9.5	11.5	13.5	dB	
Noise Figure		2.5	3	dB	
Current		5		mA	
IIP3		4		dBm	
Gain flatness	-0.5		0.5	dB	
Input return loss	12	15		dB	
Output return loss	12			dB	Pins 5, 6 (RFN, RFP) 100Ω differential
Balanced output impedance		100		Ω	
Amplitude imbalance	-1		1	dB	
Phase imbalance	-15		15	deg	
Rx Path to Bypass Mode					
Frequency	2405		2480	MHz	
In-band attenuation/noise figure		5	6	dB	SW 1dB, Bypass 2.5dB, Balun 1.5dB
Current		50		μA	
IIP3	12	20		dBm	
Gain flatness	-0.5		0.5	dB	
Input return loss	12	15		dB	
Output return loss	12			dB	
Amplitude imbalance	-1		1	dB	
Phase imbalance	-15		15	deg	
Maximum input power	10			dB	
Antenna Switch					
RF-to-Control Isolation	50			dB	
RF-to-ANT Isolation	17	20		dB	
RF-to-RF Isolation	18	20		dB	
T/R switching time			1	μS	
Logic					
Logic Level "High"	V <sub>BATT</sub> - 0.3	V <sub>BATT</sub> - 0.2	V <sub>BATT</sub>	V	
Logic Level "Low"	0		0.2	V	
Input Source Current Logic Level "High"		100	200	μA	
Input Source Current Logic Level "Low"			1	μA	

Mode	Control Logic			
	CE	C_RX_TX	C_LNA	ANTSEL
TX to ANT1	High	High	Low	Low
TX to ANT2	High	High	Low	High
RX to ANT1 LNA	High	Low	Low	Low
RX to ANT2 BYP	High	Low	High	Low
RX to ANT2 LNA	High	Low	Low	High
RX to ANT2 BYP	High	Low	High	High
Power Down	Low	Low	Low	Low

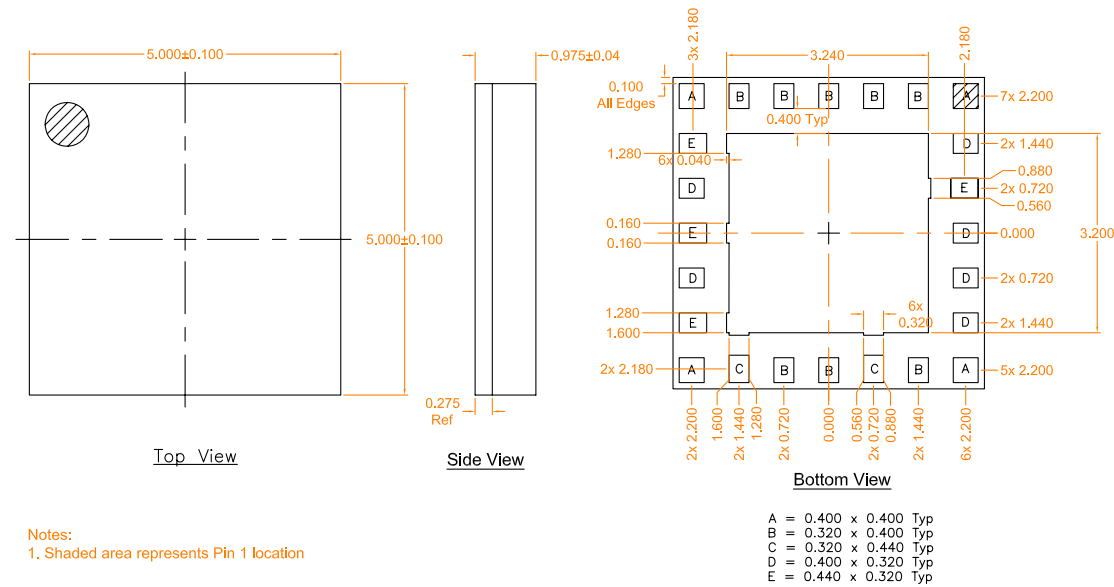
### Pin Names and Description

Pin	Function	Description
1	GND	Ground.
2	CE	Control voltage pin for chip enable. See logic table.
3	GND	Ground.
4	CT	Center rap for passing DC voltage to RFN/RFP pins that connect to TXVR SoIC.
5	RFN	Differential bi-directional RF port. Matched to 50Ω single-ended, 100Ω differential.
6	RFP	Differential bi-directional RF port. Matched to 50Ω single-ended, 100Ω differential.
7	GND	Ground.
8	VCC_DIG	Voltage supply pin for Tx power amplifier.
9	GND	Ground.
10	VCC_PA	Voltage supply pin for Tx power amplifier.
11	N/C	Not connected.
12	GND	Ground.
13	GND	Ground.
14	GND	Ground.
15	ANT1	Antenna port 1. Matched 50Ω and DC blocked internally.
16	GND	Ground.
17	ANT2	Antenna port 2. Matched 50Ω and DC blocked internally.
18	GND	Ground.
19	GND	Ground.
20	ANTSEL	Control pin for antenna selection. See logic table.
21	N/C	Not connected.
22	VCC_LNA	Voltage supply pin for Rx low noise amplifier.
23	C_LAN	Control voltage pin for LNA/bypass modes. See logic table.
24	C_RX_TX	Control voltage pin for Tx/Rx modes. See logic table.

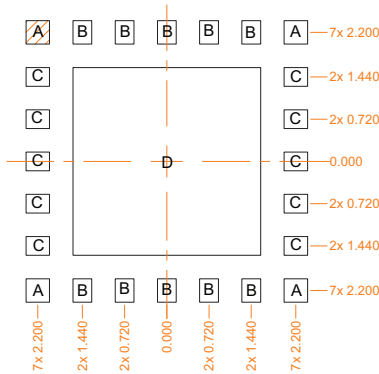
**Pin Out**



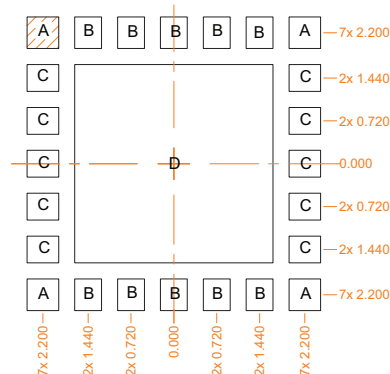
Package Drawing



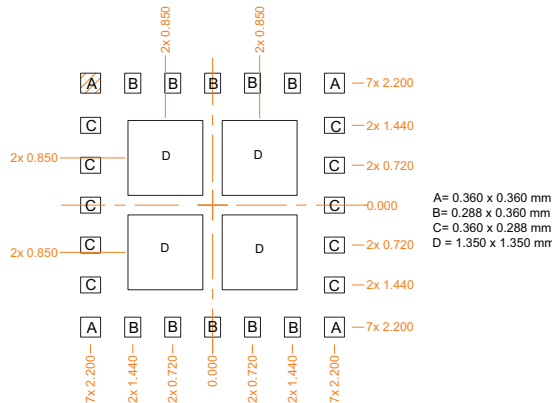
## PCB Patterns



PCB METAL LAND PATTERN  
Top View



PCB SOLDER MASK LAND PATTERN  
Top View



PCB STENCIL PATTERN  
Top View

### Notes:

1. Thermal vias for center slug "D" should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, power dissipation and electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout (gerber files are available upon request).
2. Shaded areas represents pin 1 location.

## Application Schematic

