

64Mb (4M x 16 bit) U t RAM

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Document Title

4Mx16 bit Page Mode Uni-Transistor Random Access Memory

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial - Design target	November 7, 2006	Preliminary
1.0	Finalized - Deleted PAR (Partial Refresh) & DPD (Deep Power Down) mode - Changed the name of A6 pin from \overline{PS} to DNU (Do not use) - Updated DC value	December 12, 2006	Final
2.0	Revised - Changed the ball out 'A6' (from DNU to Vcc)	February 7, 2006	Final

K1S6416BCD

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4M x 16 bit Page Mode Uni-Transistor Random Access Memory

GENERAL DESCRIPTION

The K1S6416BCD is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

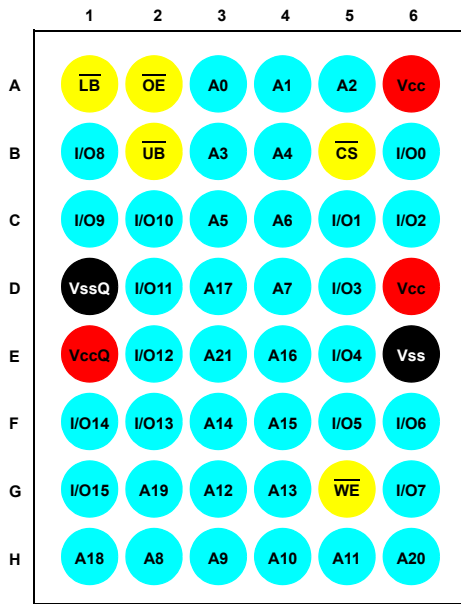
FEATURES

- Process technology: CMOS
- Organization: 4M x 16 bit
- Power supply voltage: 1.7V~1.95V
- 4-Page Read
- Three state outputs
- Supports power saving modes
 - Internal TCSR (Temperature Compensated Self Refresh)

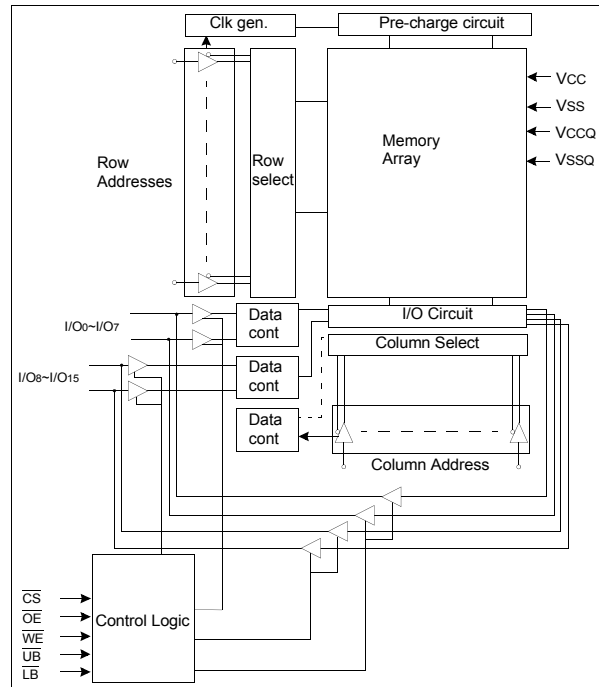
PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed (trc)	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max.)	Operating (I _{CC2P} , Max.)	
K1S6416BCD-I	Industrial(-40~85°C)	1.7V~1.95V	70ns	180μA < 85°C 120μA < 40°C	40mA	48-FBGA-6.00x8.00

PIN DESCRIPTIONS & FUNCTION BLOCK DIAGRAM



48-FBGA: Top View(Ball Down)



Name	Function	Name	Function
\overline{CS}	Chip Select Inputs	Vcc/Vccq	Power Supply(core / I/O)
\overline{OE}	Output Enable Input	Vss/Vssq	Ground
\overline{WE}	Write Enable Input	\overline{UB}	Upper Byte(I/O8~15)
A0~A21	Address Inputs	\overline{LB}	Lower Byte(I/O0~7)
I/O0~I/O15	Data Inputs/Outputs		

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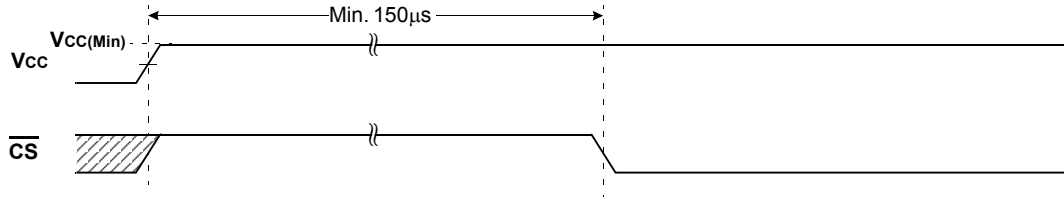
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POWER UP SEQUENCE

During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power ($V_{CC \text{ min.}} = 1.7V$) for a minimum $150\mu s$ with $\overline{CS} = \text{high}$.

TIMING WAVEFORM OF POWER UP



FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O0~7	I/O8~15	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means "Don't care". X should be low or high state.

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ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V _{ss}	V _{IN} , V _{OUT}	-0.2 to V _{CCQ} +0.3V	V
Power supply voltage relative to V _{ss}	V _{CC} , V _{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V _{CC}	1.7	1.8	1.95	V
Power supply voltage(I/O)	V _{CCQ}	1.7	1.8	1.95	V
Ground	V _{SS} , V _{SSQ}	0	0	0	V
Input high voltage	V _{IH}	V _{CCQ} -0.4	-	V _{CCQ} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.

2. Overshoot: V_{CCQ}+1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.

3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

CAPACITANCE

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

1. Freq.=1MHz, T_A=25°C

2. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CCQ}	-1	-	1	μA	
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CCQ}	-1	-	1	μA	
Average Operating Current(Async)	I _{CC2}	Cycle time=70ns, I _{IO} =0mA ²⁾ , 100% duty, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	-	-	40	mA	
	I _{CC2P}	Cycle time=t _{RC} +3t _{PC} , I _{IO} =0mA ²⁾ , 100% duty, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	-	-	40	mA	
Output Low Voltage	V _{OL}	I _{OL} =0.2mA	-	-	0.2	V	
Output High Voltage	V _{OH}	I _{OH} =-0.2mA	1.4	-	-	V	
Standby Current(CMOS)	I _{SB1} ¹⁾	$\overline{CS} \geq V_{CCQ} - 0.2V$, Other inputs=V _{SS} or V _{CCQ}	< 40°C	-	-	120	μA
			< 85°C	-	-	180	μA

1. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize Refresh cycle below 40°C.

2. I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.

AC OPERATING CONDITIONS

TEST CONDITIONS

(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CCQ}-0.2V

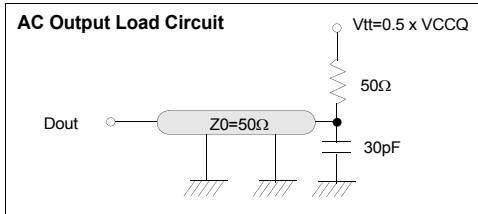
Input rising and falling time: 3ns

Input and output reference voltage: 0.5 x V_{CCQ}

Output load: C_L=30pF

V_{CC}: 1.7V~1.95V

T_A: -40°C~85°C



AC CHARACTERISTICS

Parameter List		Symbol	Speed		Units
			Min	Max	
Asynch. Read	Read Cycle Time	t _{RC}	70	-	ns
	Page Read Cycle Time	t _{PC}	25	-	ns
	Address Access Time	t _{AA}	-	70	ns
	Page Access Time	t _{PA}	-	20	ns
	Chip Select to Output	t _{CO}	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	35	ns
	\overline{UB} , \overline{LB} Access Time	t _{BA}	-	70	ns
	Chip Select to Low-Z Output	t _{LZ}	5	-	ns
	\overline{UB} , \overline{LB} Enable to Low-Z Output	t _{BLZ}	5	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t _{CHZ}	0	12	ns
	\overline{UB} , \overline{LB} Disable to High-Z Output	t _{BHZ}	0	12	ns
	Output Disable to High-Z Output	t _{OHZ}	0	10	ns
	Output Hold	t _{OH}	5	-	ns
Asynch. Write	Write Cycle Time	t _{WC}	70	-	ns
	Chip Select to End of Write	t _{CW}	60	-	ns
	Address Set-up Time to Beginning of Write	t _{AS}	0	-	ns
	Address Valid to End of Write	t _{AW}	60	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	t _{BW}	60	-	ns
	Write Pulse Width	t _{WP}	55 ¹⁾	-	ns
	\overline{WE} High Pulse Width	t _{WHP}	5	-	ns
	Write Recovery Time	t _{WR}	0	-	ns
	Data to Write Time Overlap	t _{DW}	30	-	ns
	Data Hold from Write Time	t _{DH}	0	-	ns

1. t_{WP}(min)=70ns for continuous write without CS toggling longer than 2.5us
 2. The High-Z timings measure a 100mV transition from either VOH or VOL toward V_{CCQ} x 0.5
 3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either VOH or VOL.

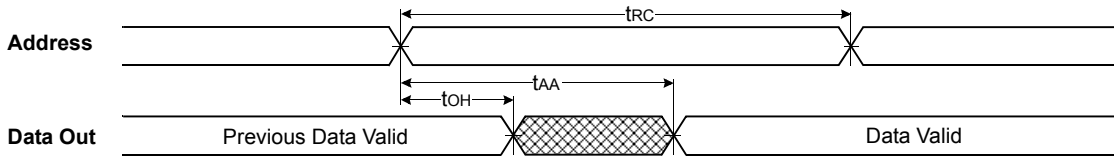
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TIMING WAVEFORMS

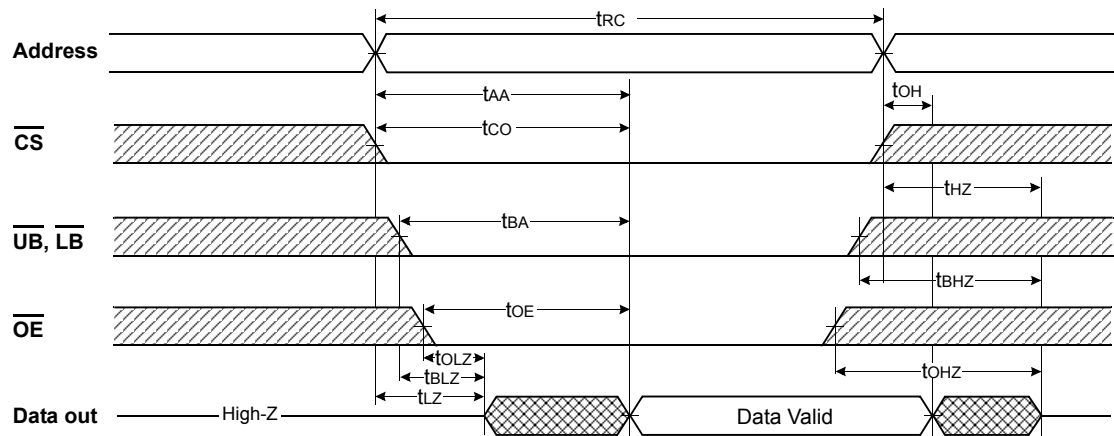
TIMING WAVEFORM OF READ CYCLE(1)

(Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)

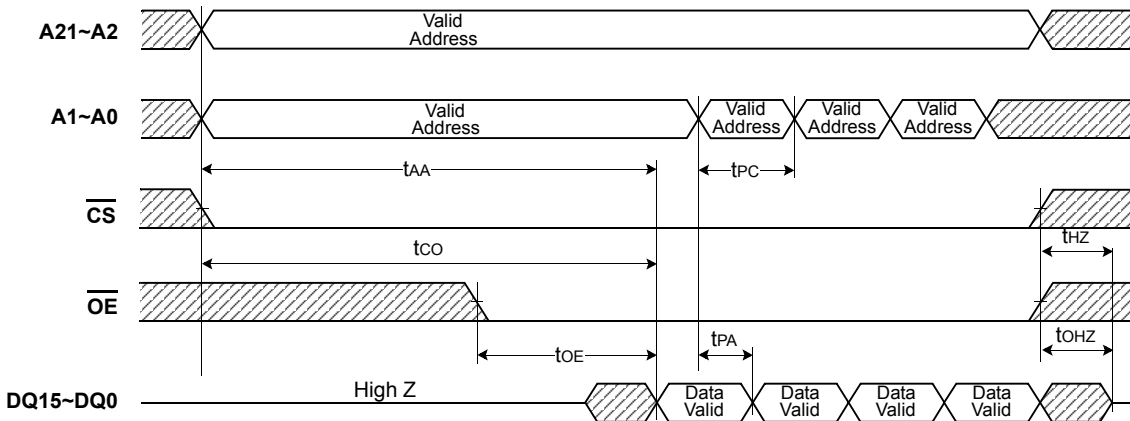


TIMING WAVEFORM OF READ CYCLE(2)

($\overline{WE}=V_{IH}$)



TIMING WAVEFORM OF PAGE CYCLE (READ ONLY)



(READ CYCLE)

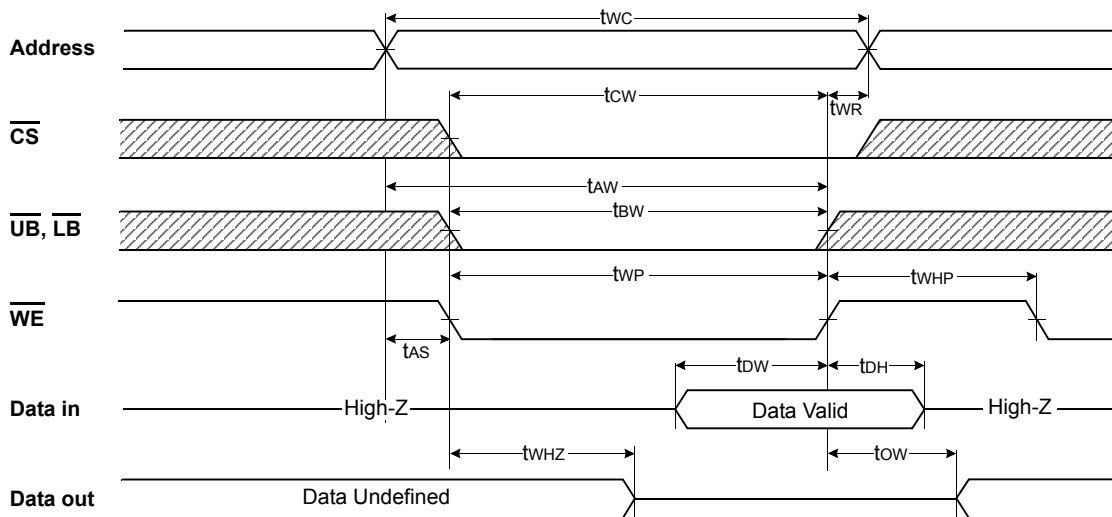
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. $t_{OE}(\text{max})$ is met only when \overline{OE} becomes enabled after $t_{AA}(\text{max})$.
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 2.5 μ s, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 2.5 μ s.

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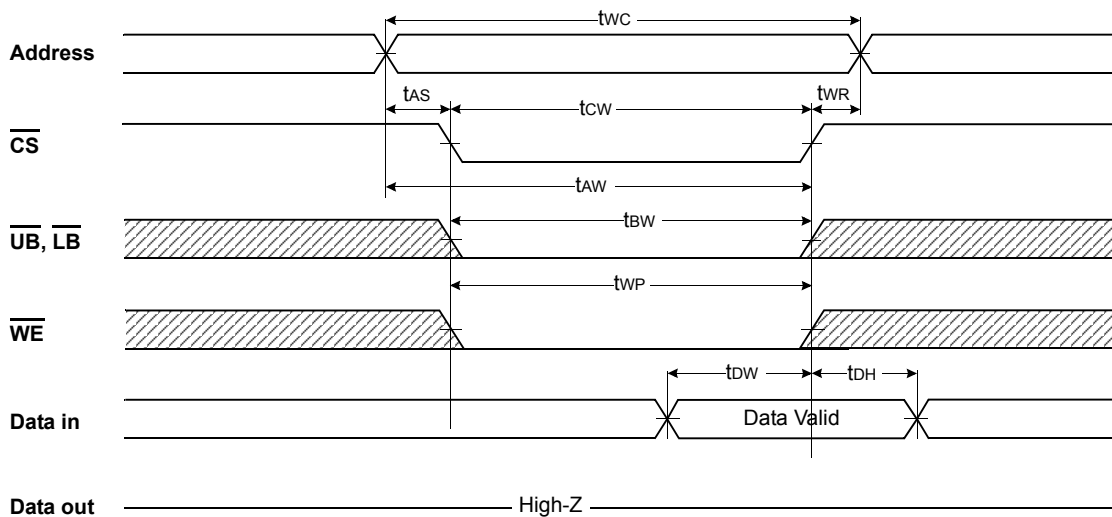
TIMING WAVEFORM OF WRITE CYCLE(1)

(WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2)

(CS Controlled)



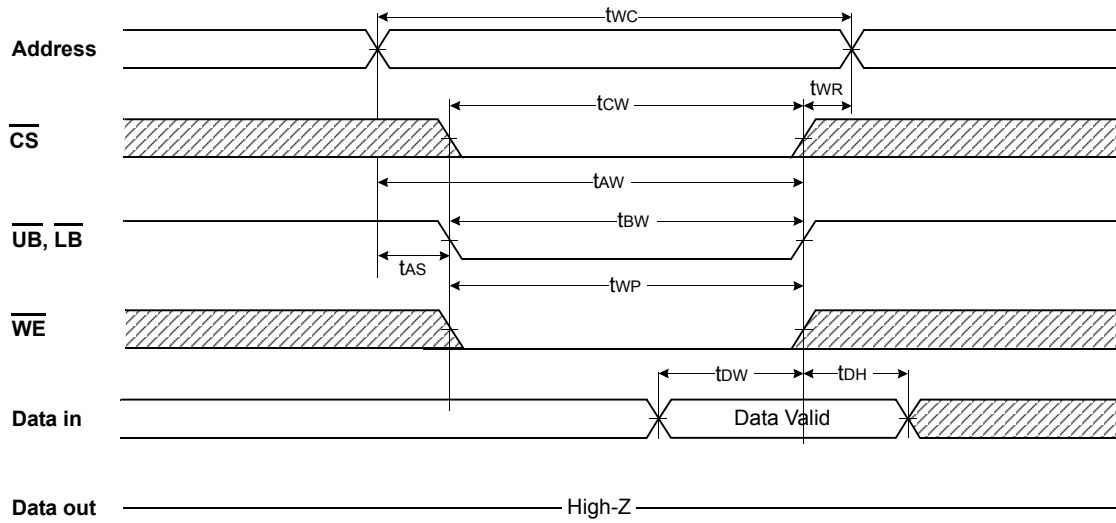
1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. In asynchronous write cycle, Clock and \overline{ADV} signals are ignored.
6. Condition for continuous write operation over 50 times : $t_{WP}(\min)=70ns$

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TIMING WAVEFORM OF WRITE CYCLE(3)

(\overline{UB} , \overline{LB} Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.

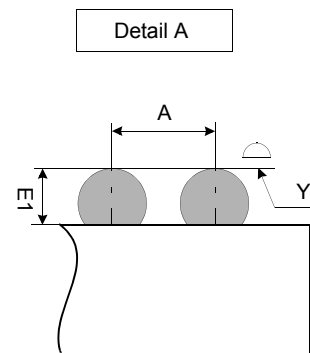
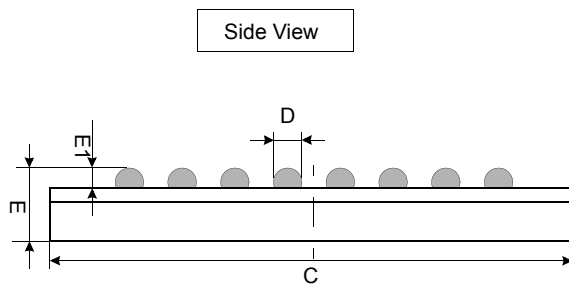
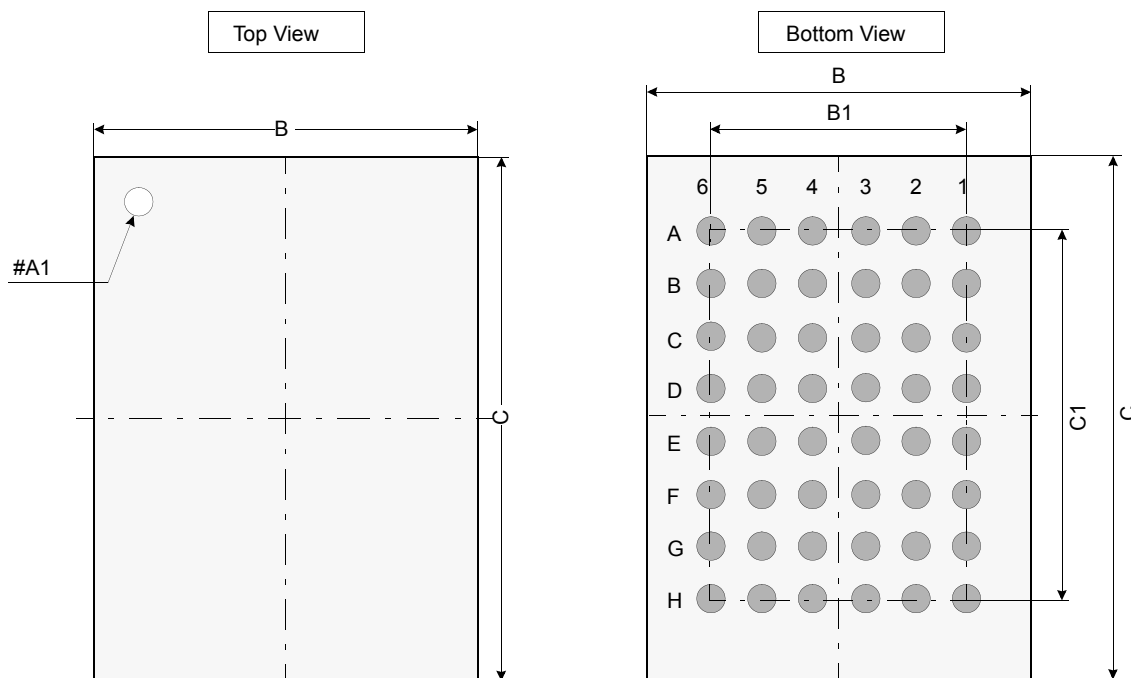
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PACKAGE DIMENSION

48 BALL FINE PITCH BGA(0.75mm ball pitch)

Unit: millimeters



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	-	1.00
E1	0.25	-	-
Y	-	-	0.10

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity