

128Mbit GDDR SDRAM

**Revision 1.2
November 2006**

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K4D263238I-UC

128M GDDR SDRAM

Revision History

Revision	Month	Year	History
0.0	September	2005	- <i>Target Spec</i> - Defined target specification
0.1	October	2005	- Added current spec
1.0	October	2005	- Finalized SPEC
1.1	January	2006	- Modified ICC6 value from 7mA to 10mA
1.2	November	2006	- Corrected typo

K4D263238I-UC

128M GDDR SDRAM

1M x 32Bit x 4 Banks Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL

FEATURES

- 2.5V ± 5% power supply for device operation
- 2.5V ± 5% power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
 - Read latency 3 (clock)
 - Burst length (2, 4, 8 and Full page)
 - Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- Write Interrupted by Read function
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- 100pin TQFP package
- Maximum clock frequency up to 250MHz
- Maximum data rate up to 500Mbps/pin

ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D263238I-UC40	250MHz	500Mbps/pin	SSTL_2	100 TQFP
K4D263238I-UC50	200MHz	400Mbps/pin		

K4D263238I-QC is the Leaded package part number.

GENERAL DESCRIPTION

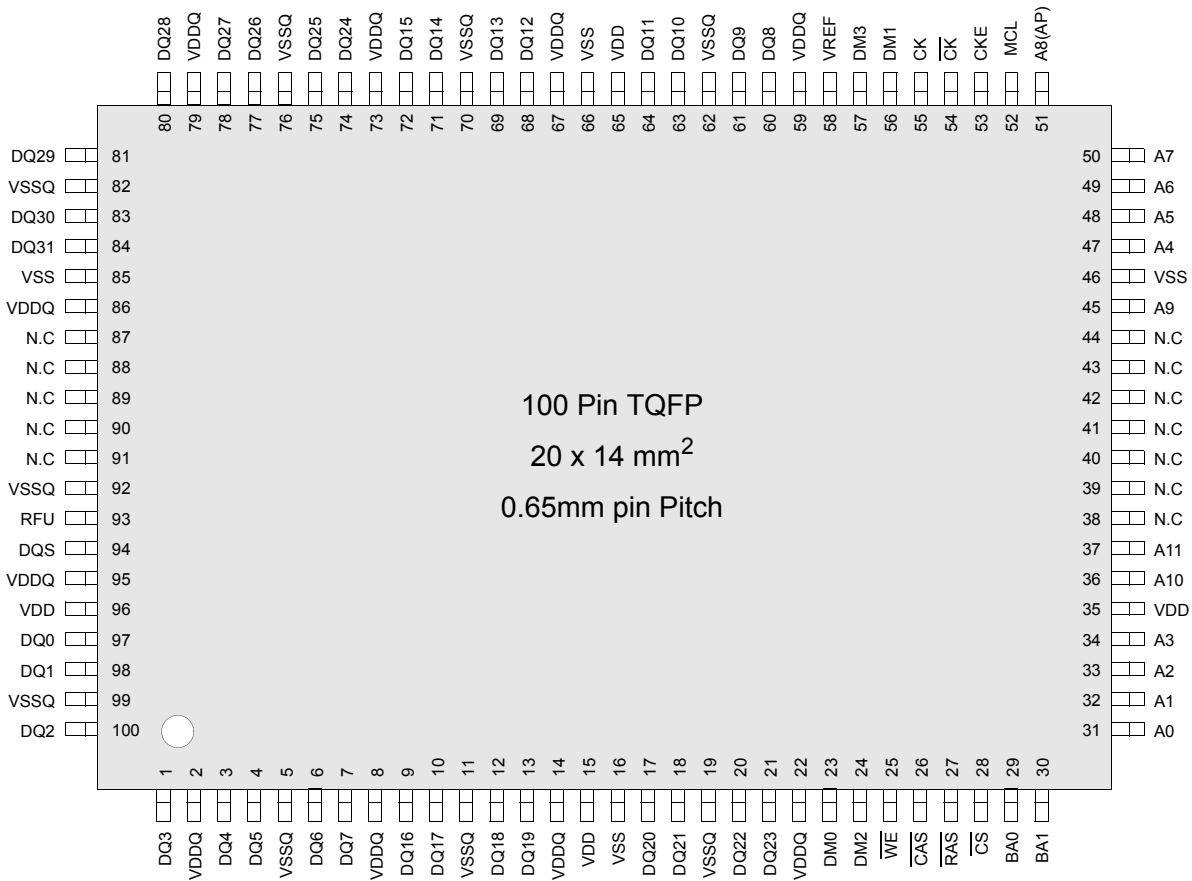
FOR 1M x 32Bit x 4 Bank DDR SDRAM

The K4D263238I is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 1,048,576 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 2.0GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

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PIN CONFIGURATION (Top View)



PIN DESCRIPTION

CK, $\overline{\text{CK}}$	Differential Clock Input	BA0, BA1	Bank Select Address
CKE	Clock Enable	A0 ~A11	Address Input
$\overline{\text{CS}}$	Chip Select	DQ0 ~ DQ31	Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe	VDD	Power
$\overline{\text{CAS}}$	Column Address Strobe	VSS	Ground
$\overline{\text{WE}}$	Write Enable	VDDQ	Power for DQ's
DQS	Data Strobe	VSSQ	Ground for DQ's
DMi	Data Mask	MCL	Must Connect Low
RFU	Reserved for Future Use		

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INPUT/OUTPUT FUNCTIONAL DESCRIPTION

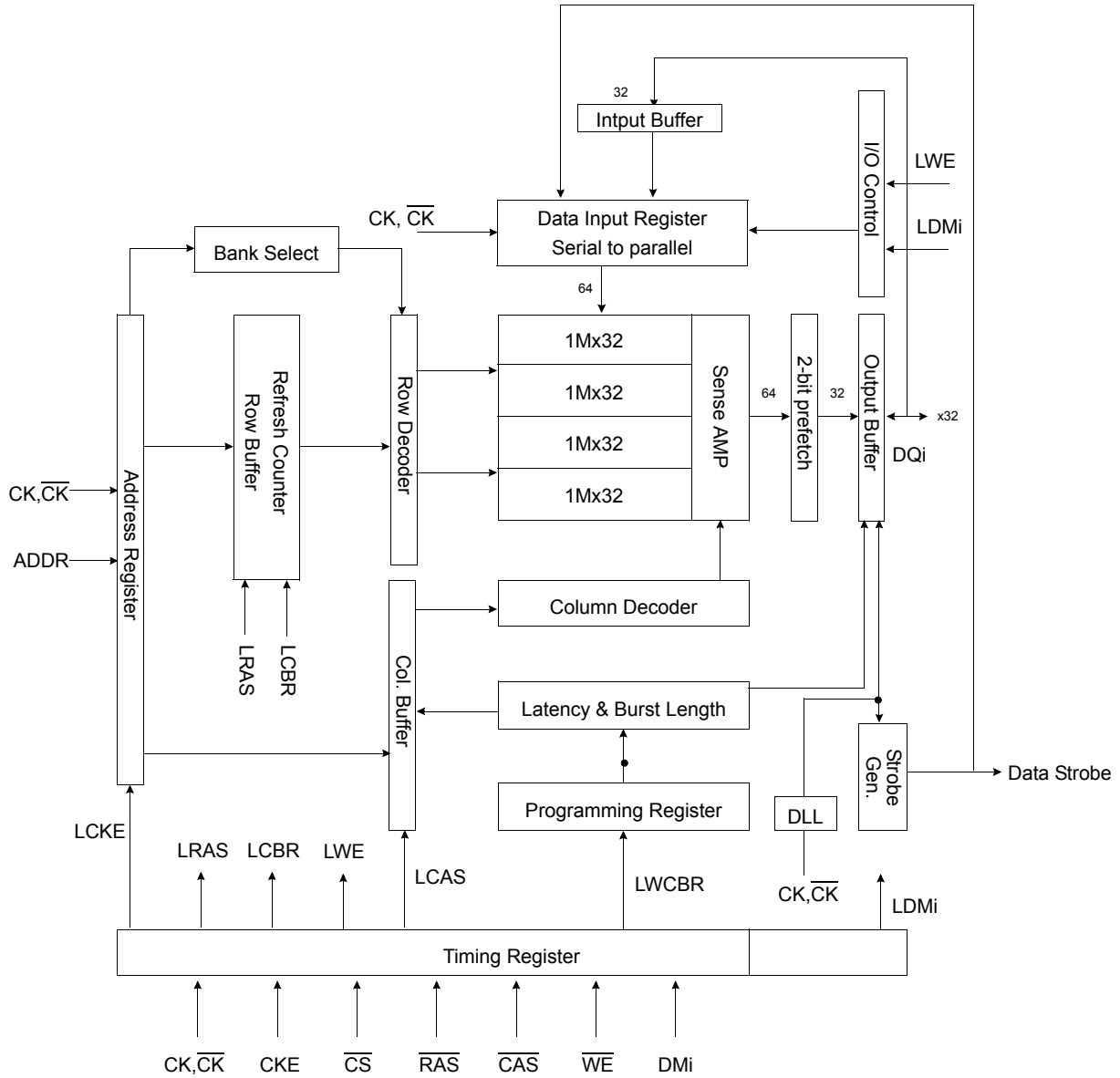
Symbol	Type	Function
CK, \overline{CK}^{*1}	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
\overline{CS}	Input	\overline{CS} enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
\overline{RAS}	Input	Latches row addresses on the positive going edge of the CK with \overline{RAS} low. Enables row access & precharge.
\overline{CAS}	Input	Latches column addresses on the positive going edge of the CK with \overline{CAS} low. Enables column access.
\overline{WE}	Input	Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active.
DQS	Input/Output	Data input and output are synchronized with both edge of DQS.
DM0 ~ DM3	Input	Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM0 for DQ0 ~ DQ7, DM1 for DQ8 ~ DQ15, DM2 for DQ16 ~ DQ23, DM3 for DQ24 ~ DQ31.
DQ0 ~ DQ31	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA0, BA1	Input	Selects which bank is to be active.
A0 ~ A11	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA7. Column address CA8 is used for auto precharge.
VDD/VSS	Power Supply	Power and ground for the input buffers and core logic.
VDDQ/VSSQ	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Power Supply	Reference voltage for inputs, used for SSTL interface.
MCL	Must Connect Low	Must connect Low

*1 : The timing reference point for the differential clocking is the cross point of CK and \overline{CK} .
For any applications using the single ended clocking, apply VREF to \overline{CK} pin.

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BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



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FUNCTIONAL DESCRIPTION

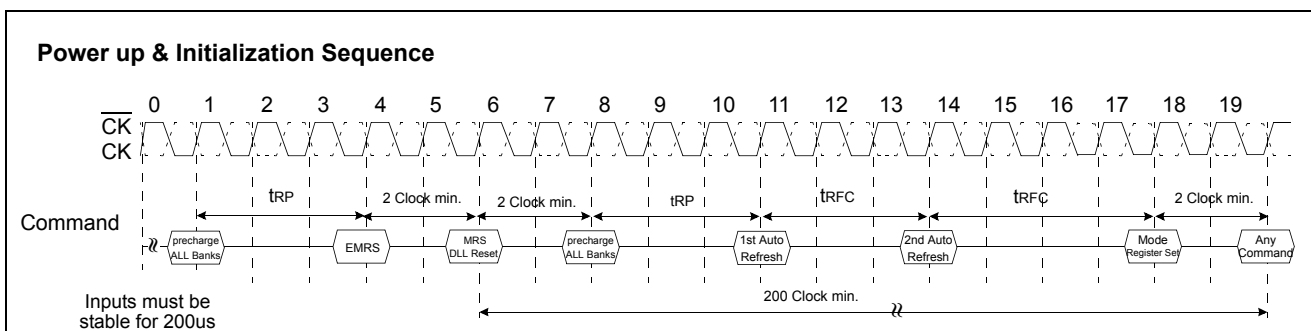
• Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
 - Apply VDD before VDDQ .
 - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,CK), apply NOP and take CKE to be high.
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL
- *1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.
- *1,2 7. Issue precharge command for all banks of the device.
8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

*2 Sequence of 6&7 is regardless of the order.



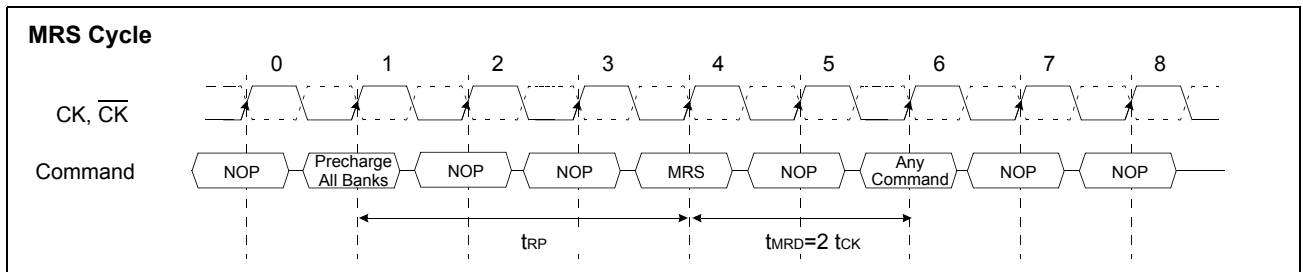
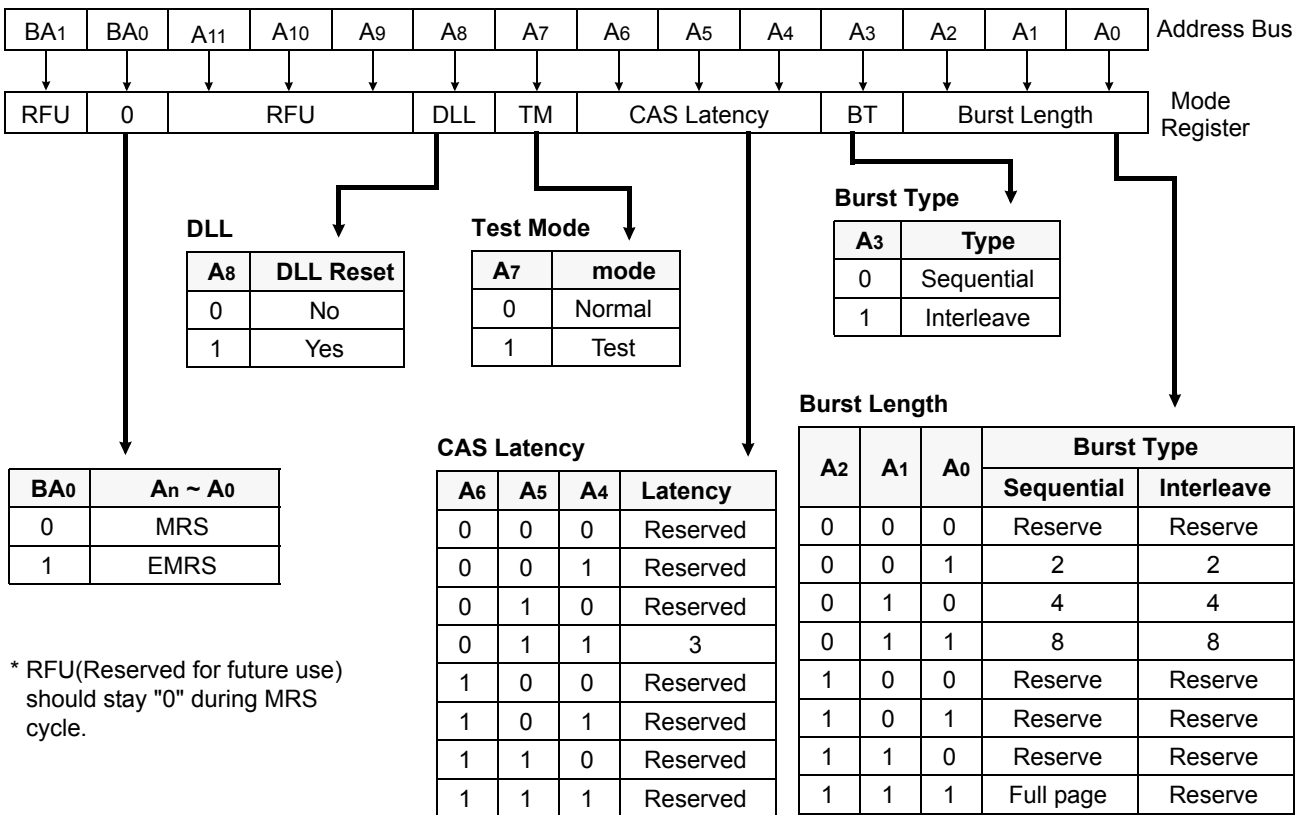
*** When the operating frequency is changed, DLL reset should be required again.
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.**

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MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on CS, RAS, CAS and WE (The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 and BA0, BA1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7,A8, BA0 and BA1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



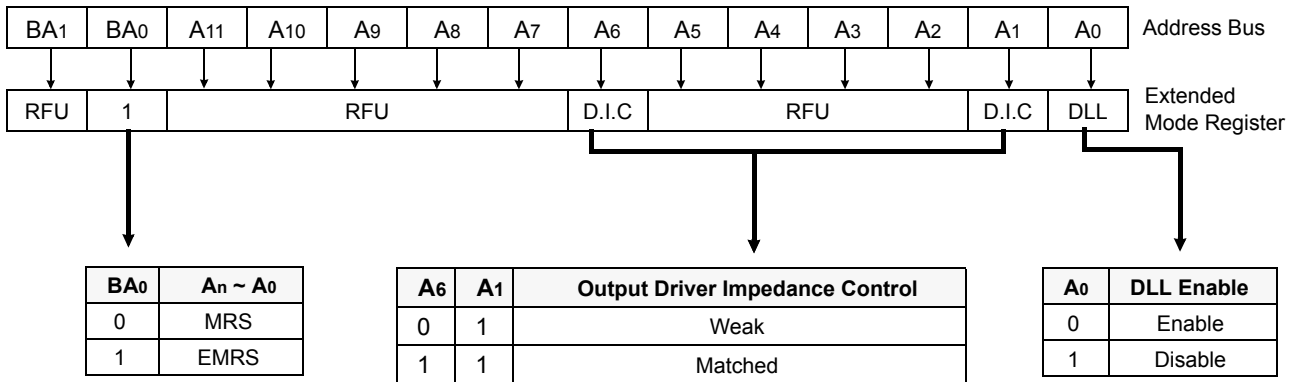
*1: MRS can be issued only at all banks precharge state.
 *2: Minimum t_{RP} is required to issue MRS command.

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EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extend mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A11 and BA1 in the same cycle as \overline{CS} , \overline{RAS} , \overline{CAS} and \overline{WE} going low are written in the extended mode register. A1 and A6 are used for setting driver strength to weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



* RFU(Reserved for future use) should stay "0" during EMRS cycle.

Figure 7. Extend Mode Register set

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	VDD	-1.0 ~ 3.6	V
Voltage on VDD supply relative to Vss	VDDQ	-0.5 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	1.8	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	VDD	2.375	2.50	2.625	V	1
Output Supply voltage	VDDQ	2.375	2.50	2.625	V	1
Reference voltage	VREF	0.49*VDDQ	-	0.51*VDDQ	V	2
Termination voltage	V _{tt}	VREF-0.04	VREF	VREF+0.04	V	3
Input logic high voltage	V _{IH}	VREF+0.15	-	VDDQ+0.30	V	4
Input logic low voltage	V _{IL}	-0.30	-	VREF-0.15	V	5
Output logic high voltage	V _{OH}	V _{tt} +0.76	-	-	V	I _{OH} =-15.2mA
Output logic low voltage	V _{OL}	-	-	V _{tt} -0.76	V	I _{OL} =+15.2mA
Input leakage current	I _{IL}	-5	-	5	uA	6
Output leakage current	I _{OL}	-5	-	5	uA	6

Note :

- Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
- V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed ± 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed ± 25mV for DC error and an additional ± 25mV for AC noise.
- V_{tt} of the transmitting device must track V_{REF} of the receiving device.
- V_{IH}(max.)= V_{DDQ} +1.5V for a pulse and it which can not be greater than 1/3 of the cycle rate.
- V_{IL}(min.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
- For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD} is acceptable. For all other pins that are not under test V_{IN}=0V.

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DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, TA=0 to 65°C)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-40	-50		
Operating Current (One Bank Active)	I _{CC1}	Burst Lenth=2 t _{RC} ≥ t _{RC} (min) I _{OL} =0mA, t _{CC} = t _{CC} (min)	199	187	mA	1
Precharge Standby Current in Power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min)	10	10	mA	
Precharge Standby Current in Non Power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(min)$, t _{CC} = t _{CC} (min).	48	43	mA	
Active Standby Current power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), t _{CC} = t _{CC} (min)	78	66	mA	
Active Standby Current in in Non Power-down mode	I _{CC3N}	CKE ≥ V _{IH} (min), $\overline{CS} \geq V_{IH}(min)$, t _{CC} = t _{CC} (min) .	153	133	mA	
Operating Current (Burst Mode)	I _{CC4}	I _{OL} =0mA ,t _{CC} = t _{CC} (min), Page Burst, All Banks activated.	412	358	mA	
Refresh Current	I _{CC5}	t _{RC} ≥ t _{RFC} (min)	168	144	mA	2
Self Refresh Current	I _{CC6}	CKE ≤ 0.2V	10		mA	

- Note:** 1. Measured with outputs open.
2. Refresh period is 32ms.

AC INPUT OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}/ V_{DDQ}=2.5V± 5%, TA=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V _{IH}	V _{REF} +0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V _{IL}	-	-	V _{REF} -0.35	V	
Clock Input Differential Voltage; CK and \overline{CK}	V _{ID}	0.7	-	V _{DDQ} +0.6	V	1
Clock Input Crossing Point Voltage; CK and \overline{CK}	V _{IX}	0.5*V _{DDQ} -0.2	-	0.5*V _{DDQ} +0.2	V	2

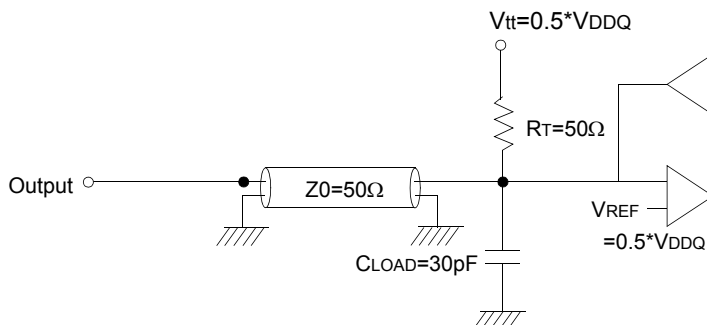
- Note :** 1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK}
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same

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AC OPERATING TEST CONDITIONS ($V_{DD}/V_{DDQ}=2.5V\pm 5\%$, $T_A= 0$ to $65^\circ C$)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	$0.50*V_{DDQ}$	V	
CK and \overline{CK} signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	$V_{REF}+0.35/V_{REF}-0.35$	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

CAPACITANCE ($V_{DD}=2.5V$, $T_A= 25^\circ C$, $f=1MHz$)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, \overline{CK})	C_{IN1}	1.0	5.0	pF
Input capacitance($A_0\sim A_{11}$, $BA_0\sim BA_1$)	C_{IN2}	1.0	4.0	pF
Input capacitance (CKE, CS, RAS, CAS, \overline{WE})	C_{IN3}	1.0	4.0	pF
Data & DQS input/output capacitance(DQ0~DQ31)	C_{OUT}	1.0	6.0	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	1.0	6.0	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	$0.1 + 0.01$	μF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	$0.1 + 0.01$	μF

- Note :**
- V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
 - V_{SS} and V_{SSQ} pins are separated each other
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

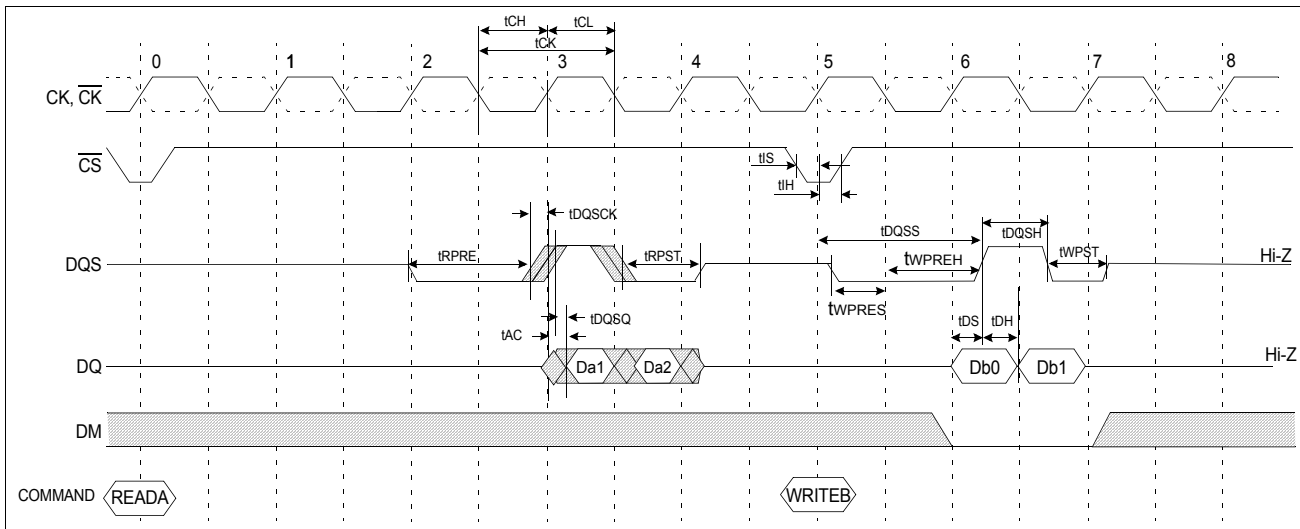
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AC CHARACTERISTICS

Parameter	Symbol	-40		-50		Unit	Note	
		Min	Max	Min	Max			
CK cycle time	CL=3	tCK	4.0	10	5.0	10	ns	
CK high level width		tCH	0.45	0.55	0.45	0.55	tCK	
CK low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK		tDQSCK	-0.6	0.6	-0.7	+0.7	ns	
Output access time from CK		tAC	-0.6	0.6	-0.7	+0.7	ns	
Data strobe edge to Dout edge		tDQSQ	-	0.4	-	+0.45	ns	1
Read preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.85	1.15	0.8	1.2	tCK	
DQS-In setup time		tWPRES	0	-	0	-	ns	
DQS-in hold time		tWPREH	0.35	-	0.25	-	tCK	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	
DQS-In high level width		tDQSH	0.4	0.6	0.4	0.6	tCK	
DQS-In low level width		tDQSL	0.4	0.6	0.4	0.6	tCK	
Address and Control input setup		tIS	0.9	-	1.0	-	ns	
Address and Control input hold		tIH	0.9	-	1.0	-	ns	
DQ and DM setup time to DQS		tDS	0.4	-	0.45	-	ns	
DQ and DM hold time to DQS		tDH	0.4	-	0.45	-	ns	
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1
Data output hold time from DQS		tQH	tHP-0.4	-	tHP-0.45	-	ns	1

Simplified Timing @ BL=2, CL=3



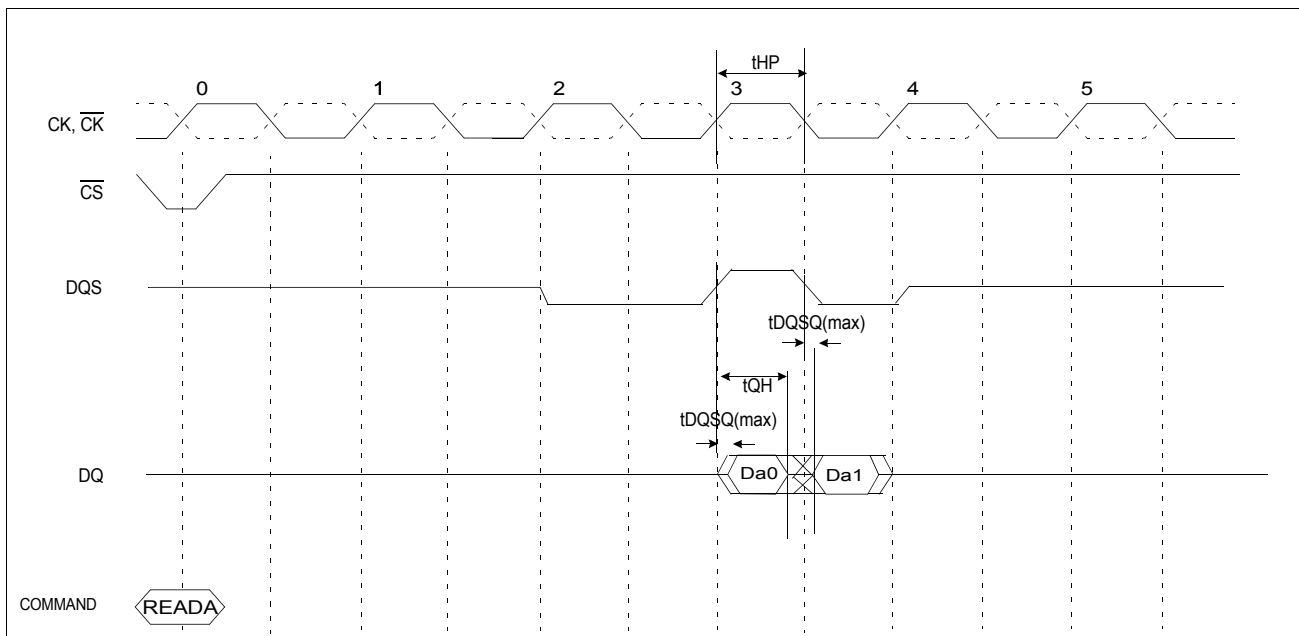
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Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(t_{DV}) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of $t_{DV}(=0.35t_{CK})$ artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, t_{QH} which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces t_{DV}
- $t_{QHmin} = t_{HP}-X$ where
 - . t_{HP} =Minimum half clock period for any given cycle and is defined by clock high or clock low time(t_{CH}, t_{CL})
 - . X =A frequency dependent timing allowance account for $t_{DQSQmax}$

t_{QH} Timing (CL3, BL2)



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AC CHARACTERISTICS (I)

Parameter	Symbol	-40		-50		Unit	Note
		Min	Max	Min	Max		
Row cycle time	tRC	15	-	12	-	tCK	
Refresh row cycle time	tRFC	17	-	14	-	tCK	
Row active time	tRAS	10	100K	8	100K	tCK	
RAS to CAS delay for Read	tRCDRD	5	-	4	-	tCK	
RAS to CAS delay for Write	tRCDWR	3	-	2	-	tCK	
Row precharge time	tRP	5	-	4	-	tCK	
Row active to Row active	tRRD	3	-	2	-	tCK	
Last data in to Row precharge	tWR	3	-	2	-	tCK	1
Last data in to Read command	tCDLR	2	-	2	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	tCK	
Auto precharge write recovery + Pre-charge	tDAL	8	-	6	-	tCK	
Exit self refresh to read command	tXSR	200	-	200	-	tCK	
Power down exit time	tPDEX	1tCK+tIS	-	1tCK+tIS	-	ns	
Refresh interval time	tREF	-	7.8	-	7.8	us	

Note :1 For normal write operation, even numbers of Din are to be written inside DRAM

(Unit : Number of Clock)

AC CHARACTERISTICS (II)

K4D263238I-UC40

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
250MHz (4.0ns)	3	15	17	10	5	3	5	3	8	tCK
200MHz (5.0ns)	3	12	14	8	4	2	4	2	6	tCK

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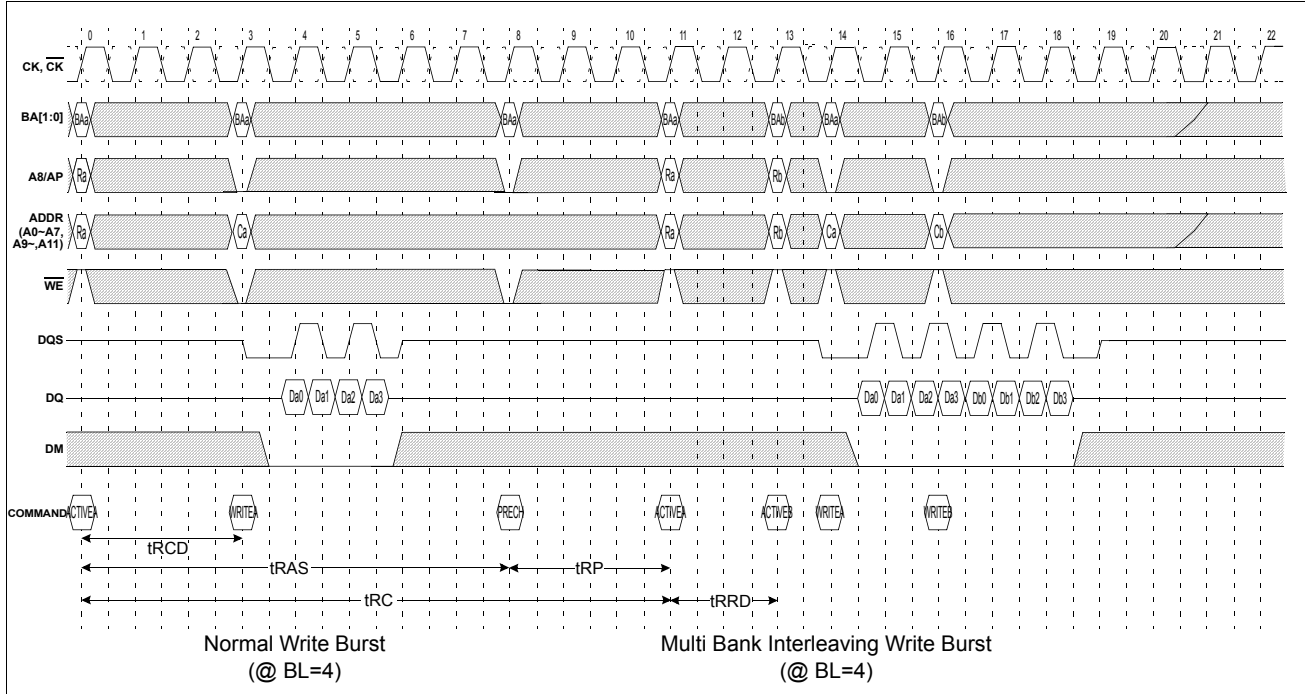
Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
200MHz (5.0ns)	3	12	14	8	4	2	4	2	6	tCK
183MHz (5.5ns)	3	12	14	8	4	2	4	2	6	tCK
166MHz (6.0ns)	3	10	12	7	3	2	3	2	5	tCK

* 183/166MHz were supported in K4D263238I-UC50

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128M GDDR SDRAM

Simplified Timing(2) @ BL=4, CL=3



K4D263238I-UC

128M GDDR SDRAM

PACKAGE DIMENSIONS (TQFP)

Dimensions in Millimeters

