64Mbit DDR SDRAM

512K x 32Bit x 4 Banks
Double Data Rate Synchronous DRAM
with Bi-directional Data Strobe and DLL

Revision 1.1

February 2001

Revision History

Revision 1.1 (February 1, 2001)
• Removed K4D62323HA-QC50

Revision 1.0 (August 16, 2000)

Revision 0.5 (July 12, 2000)
• Removed Block Write function. Accordingly pin number 52 must be connected to low (MCL only)
• Removed Write Interrupted by Read function.
• Changed I_{CC1}/I_{CC2N}/I_{CC3N}/I_{CC5} of K4D62323HA-* in "DC Characteristics" table.
• Changed VIH/VIL of AC operating conditions from $V_{REF}\pm$ 0.31 to $V_{REF}\pm$ 0.35

Revision 0.4 (May 18, 2000) - *Preliminary Spec*
• Changed tCDLR from 1tCK to 2tCK
• Changed tDOSCK/tAC of K4D62323HA-QC50/55 from +/-0.6ns to 0.75ns
• Replaced tDV with tOH in accordance with JEDEC
• Changed DC operating conditions
  - V_{REF} from 1.15V(min)/1.35V(max) to 0.49*V_{DDQ}/0.51*V_{DDQ}
  - V_{IH}/V_{IL} from V_{REF}+0.18(min)/V_{REF}-0.18(max) to V_{REF}+0.15(min)/V_{REF}-0.15(max)
• Changed VIH/VIL of AC operating conditions from $V_{REF}\pm$ 0.35 to $V_{REF}\pm$ 0.31

Revision 0.3 (March 17, 2000)
• Define DC spec.

Revision 0.2 (February 17, 2000)
• Add K4D62323HA-QC50
• Removed K4D62323HA-QC66
• Changed tRCD and tRP of K4D62323HA-QC55/60 from 4tCK to 3tCK
• Removed tHZQ and tDIPW from the spec.
• Changed tWPST from 0.25tCK to 0.4/0.6tCK
• Changed tDQSCK and tAC of K4D62323HA-QC55 from 0.75ns to 0.6ns
• Changed tCDLR from 2tCK to 1tCK

Revision 0.1 (January 6, 2000) - *Target Spec*
• Defined Target Specification

512K x 32Bit x 4 Banks Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL

FEATURES

- 3.3V ±5% power supply for device operation
- 2.5V ±5% power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - -. Read latency 3 (clock)
  - -. Burst length (2, 4, 8 and Full page)
  - -. Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 16ms refresh period (2K cycle)
- 100pin TQFP package
- Maximum clock frequency up to 183MHz
- Maximum data rate up to 366Mbps/pin

ORDERING INFORMATION

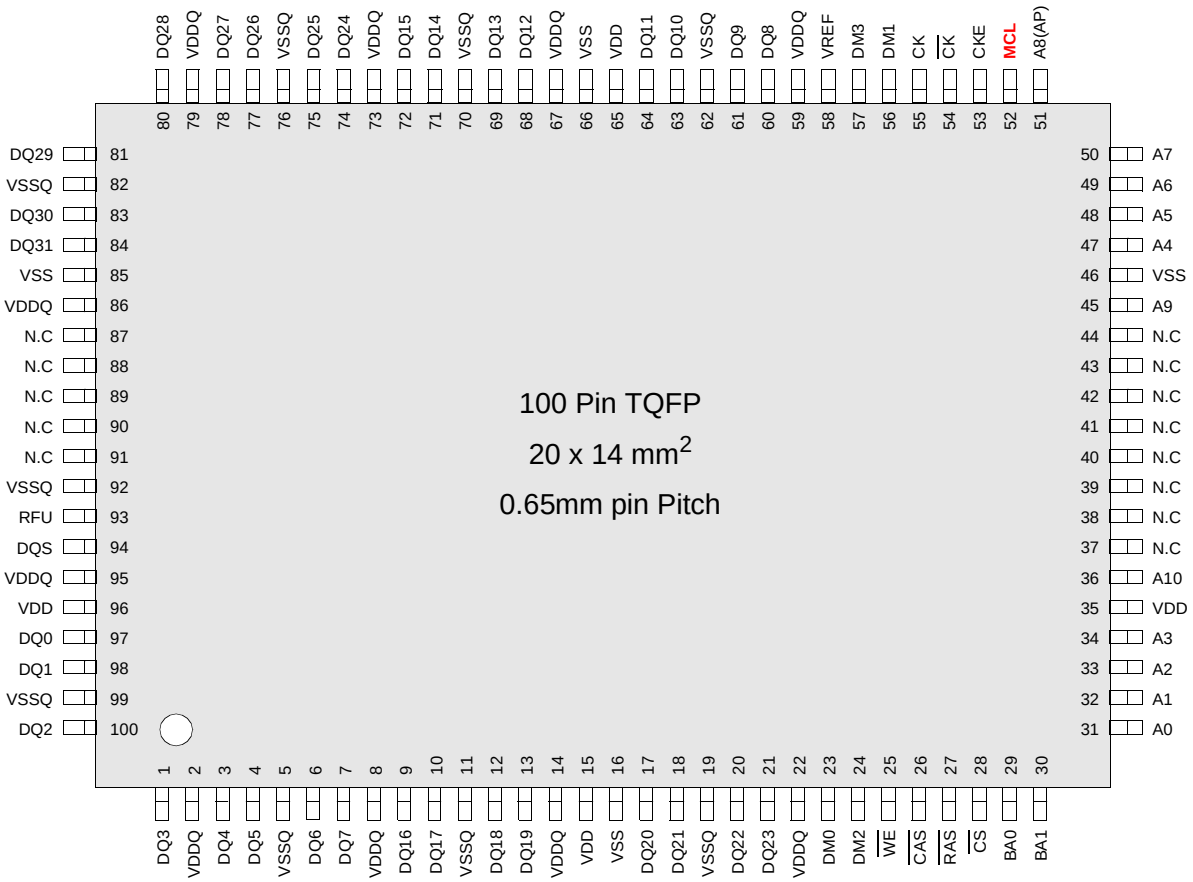
Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D62323HA-QC55	183MHz	366Mbps/pin	SSTL_2	100 TQFP
K4D62323HA-QC60	166MHz	333Mbps/pin		
K4D62323HA-QC70	143MHz	286Mbps/pin		

GENERAL DESCRIPTION

FOR 512K x 32Bit x 4 Bank DDR SDRAM

The K4D62323H is 67,108,864 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 524,288 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1.5GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION (Top View)



PIN DESCRIPTION

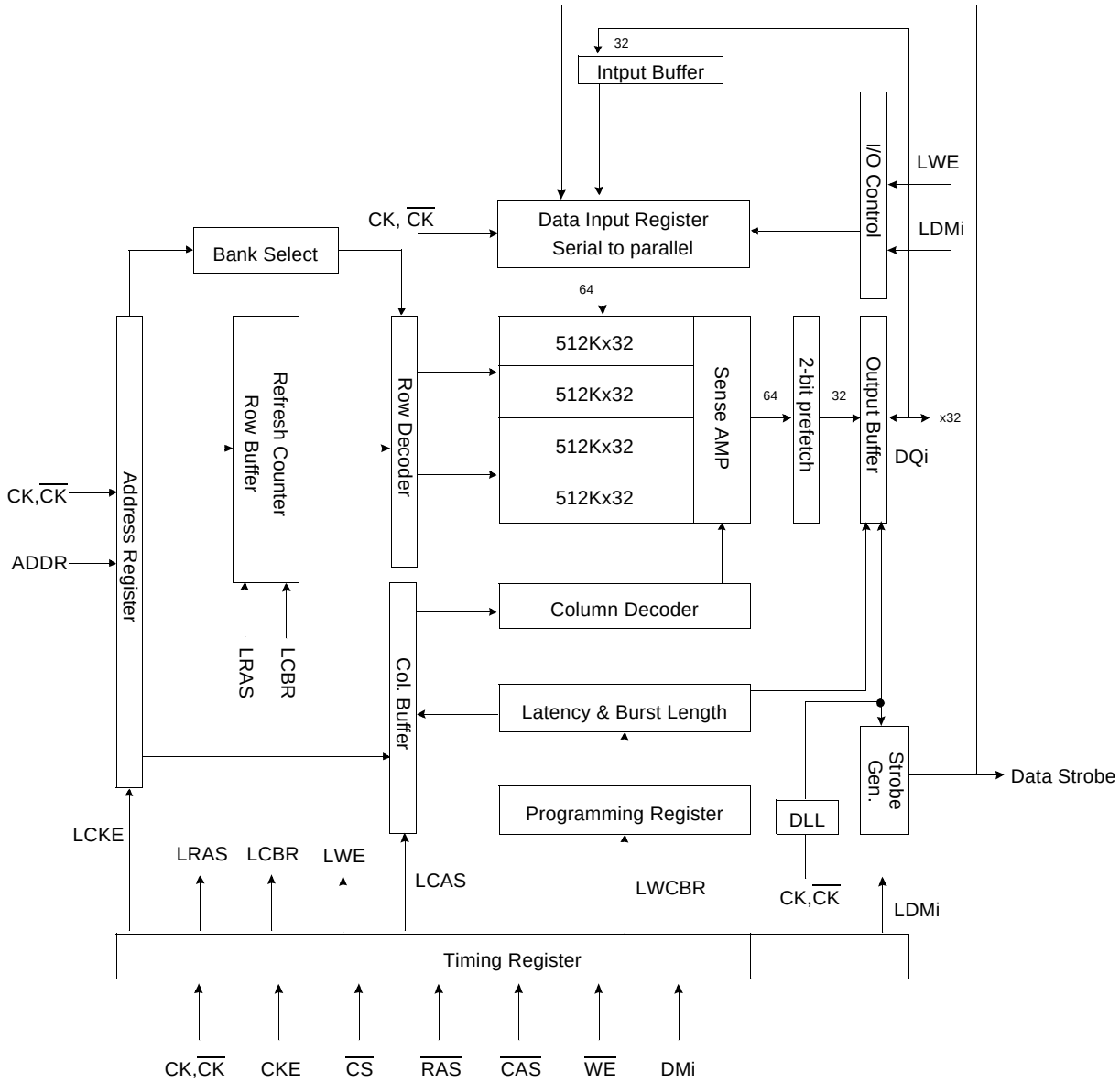
CK,$\overline{CK}$	Differential Clock Input	BA_0, BA_1	Bank Select Address
CKE	Clock Enable	A_0 ~A_{10}	Address Input
$\overline{CS}$	Chip Select	DQ_0 ~ DQ_{31}	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	V_{DDQ}	Power for DQ′s
DQS	Data Strobe	V_{SSQ}	Ground for DQ′s
DM0~DM3	Data Mask	MCL	Must Connect Low
RFU	Reserved for Future Use	-	-

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$*1	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Latches row addresses on the positive going edge of the CK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Input	Latches column addresses on the positive going edge of the CK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Input	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQS	Input/Output	Data input and output are synchronized with both edge of DQS.
DM_0 ~ DM_3	Input	Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM_0 for DQ_0 ~ DQ_7, DM_1 for DQ_8 ~ DQ_{15}, DM_2 for DQ_{16} ~ DQ_{23}, DM_3 for DQ_{24} ~ DQ_{31}.
DQ_0 ~ DQ_{31}	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA_0, BA_1	Input	Selects which bank is to be active.
A_0 ~ A_{10}	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA_0 ~ RA_{10}, Column addresses : CA_0 ~ CA_7. Column address CA_8 is used for auto precharge.
V_{DD}/V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ}/V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
MCL	MCL	Must connect to low

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{CK}$.
For any applications using the single ended clocking, apply V_{REF} to $\overline{CK}$ pin.

BLOCK DIAGRAM (512Kbit x 32I/O x 4 Bank)



FUNCTIONAL DESCRIPTION

• Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
   - Apply VDD before VDDQ .
   - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,$\overline{CK}$), apply NOP and take CKE to be high.
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL

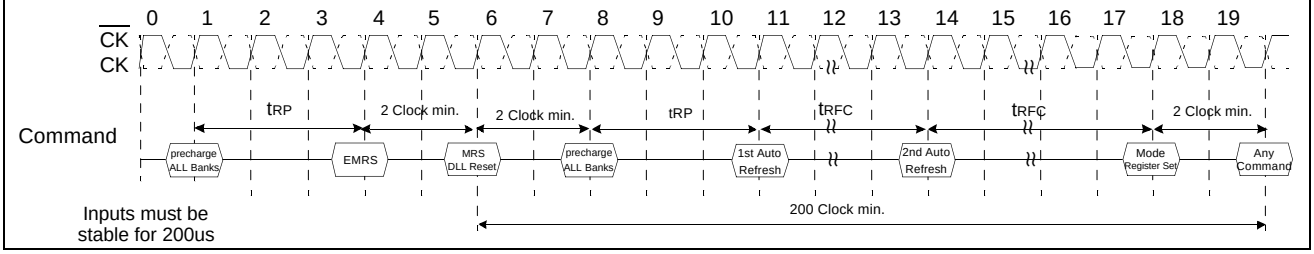
*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.

*1,2 7. Issue precharge command for all banks of the device.

8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

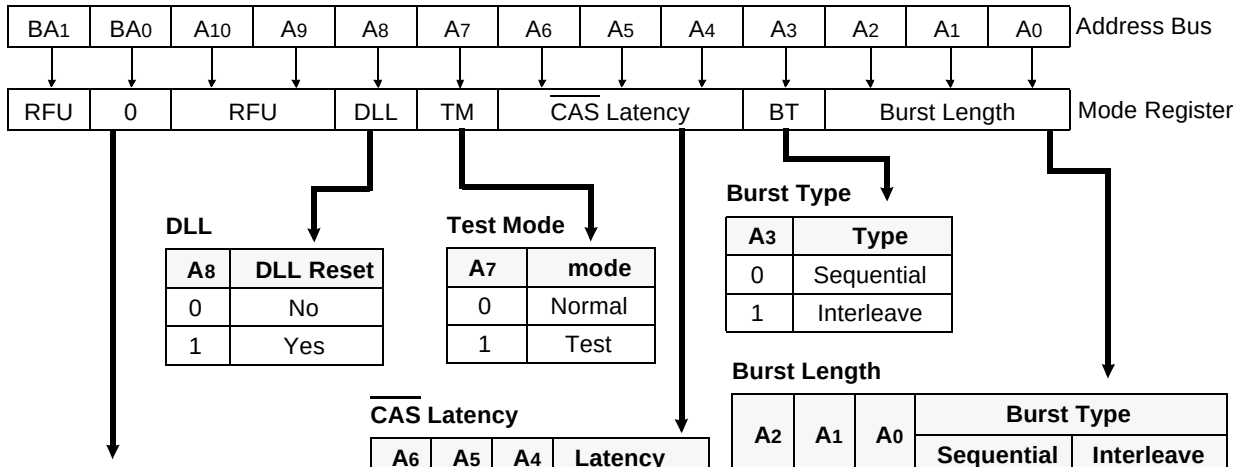
*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.
*2 Sequence of 6&7 is regardless of the order.

Power up & Initialization Sequence



MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on CS, RAS, CAS and WE(The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{10} and BA_0, BA_1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, CAS latency(read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_8 is used for DLL reset. A_7,A_8, BA_0 and BA_1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



DLL

A_8	DLL Reset
0	No
1	Yes

Test Mode

A_7	mode
0	Normal
1	Test

Burst Type

A_3	Type
0	Sequential
1	Interleave

BA_0	A_n ~ A_0
0	MRS
1	EMRS

* RFU(Reserved for future use) should stay "0" during MRS cycle.

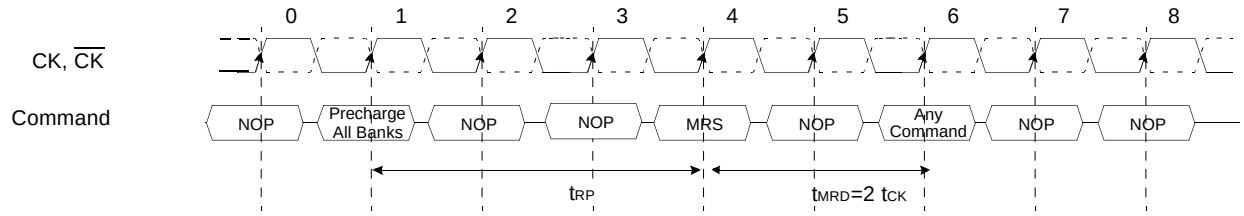
CAS Latency

A_6	A_5	A_4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	Reserve
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

Burst Length

A_2	A_1	A_0	Burst Type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full page	Reserve

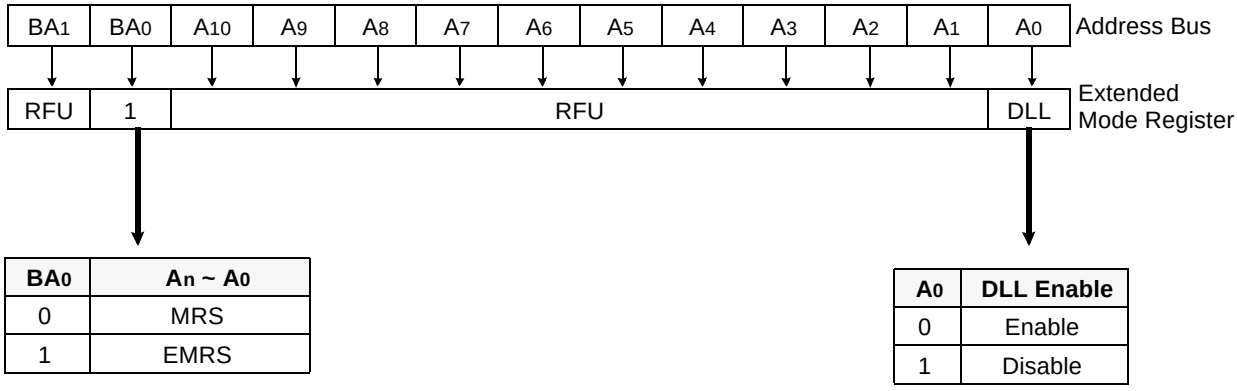
MRS Cycle



*1 : MRS can be issued only at all banks precharge state.
*2 : Minimum t_{RP} is required to issue MRS command.

EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL. The default value of the extended mode register is not defined, therefore the extened mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A10 and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



BA0	An ~ A0
0	MRS
1	EMRS

A0	DLL Enable
0	Enable
1	Disable

* RFU(Reserved for future use) should stay "0" during EMRS cycle.

Figure 7. Extend Mode Register set

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.6	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	3.135	3.3	3.465	V	1
Output Supply voltage	V_{DDQ}	2.375	2.50	2.625	V	1
Reference voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V	2
Termination voltage	Vtt	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
Input logic high voltage	V_{IH}	V_{REF}+0.15	-	V_{DDQ}+0.30	V	
Input logic low voltage	V_{IL}	-0.30	-	V_{REF}-0.15	V	4
Output logic high voltage	V_{OH}	Vtt+0.76	-	-	V	I_{OH}=-15.2mA
Output logic low voltage	V_{OL}	-	-	Vtt-0.76	V	I_{OL}=+15.2mA
Input leakage current	I_{IL}	-5	-	5	uA	5
Output leakage current	I_{OL}	-5	-	5	uA	5

Note :
1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed ± 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed ± 25mV for DC error and an additional ± 25mV for AC noise.
3. V_{tt} of the transmitting device must track V_{REF} of the receiving device.
4. V_{IL}(min.)= -1.5V AC(pulse width ≤ 5ns).
5. For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD}+0.3V is acceptable. For all other pins that are not under test V_{IN}=0V.

DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, T_A=0 to 65°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-55	-60	-70		
Operating Current (One Bank Active)	I_{CC1}	Burst Lenth=2 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA, t_{CC}= t_{CC}(min)	330	330	300	mA	1
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	60			mA	
Precharge Standby Current in Non Power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}= t_{CC}(min)	155	150	140	mA	
Active Standby Current power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	95			mA	
Active Standby Current in in Non Power-down mode	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}=t_{CC}(min)	195	190	185	mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA ,t_{CC}= t_{CC}(min), Page Burst, All Banks activated	430	410	370	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RFC}$(min)	430	410	350	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	4			mA	

Note : 1. Measured with outputs open.
2. Refresh period is 16ms.

AC INPUT OPERATING CONDITIONS

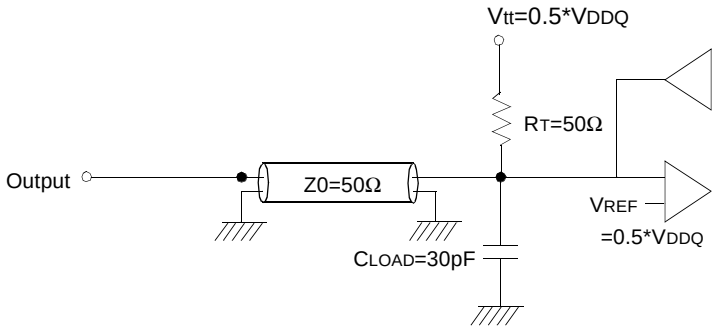
Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}=3.3V± 5%, V_{DDQ}=2.5V± 5%, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V_{IH}	V_{REF}+0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V_{IL}	-	-	V_{REF}-0.35	V	
Clock Input Differential Voltage ; CK and $\overline{CK}$	V_{ID}	0.7	-	V_{DDQ}+0.6	V	1
Clock Input Crossing Point Voltage ; CK and $\overline{CK}$	V_{IX}	0.5*V_{DDQ}-0.2	-	0.5*V_{DDQ}+0.2	V	2

Note : 1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same

AC OPERATING TEST CONDITIONS (V_{DD}=3.3V±0.15V, T_A= 0 to 65°C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	0.50*V_{DDQ}	V	
CK and $\overline{CK}$ signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.35/V_{REF}-0.35	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

CAPACITANCE (V_{DD}=3.3V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0~A_{10}, BA_0~BA_1)	C_{IN1}	2.5	4.5	pF
Input capacitance (CK, $\overline{CK}$,CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN2}	2.5	5.0	pF
Data & DQS input/output capacitance(DQ_0~DQ_{31})	C_{OUT}	2.5	5.5	pF
Input capacitance(DM0 ~ DM3)	C_{IN3}	2.5	5.5	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

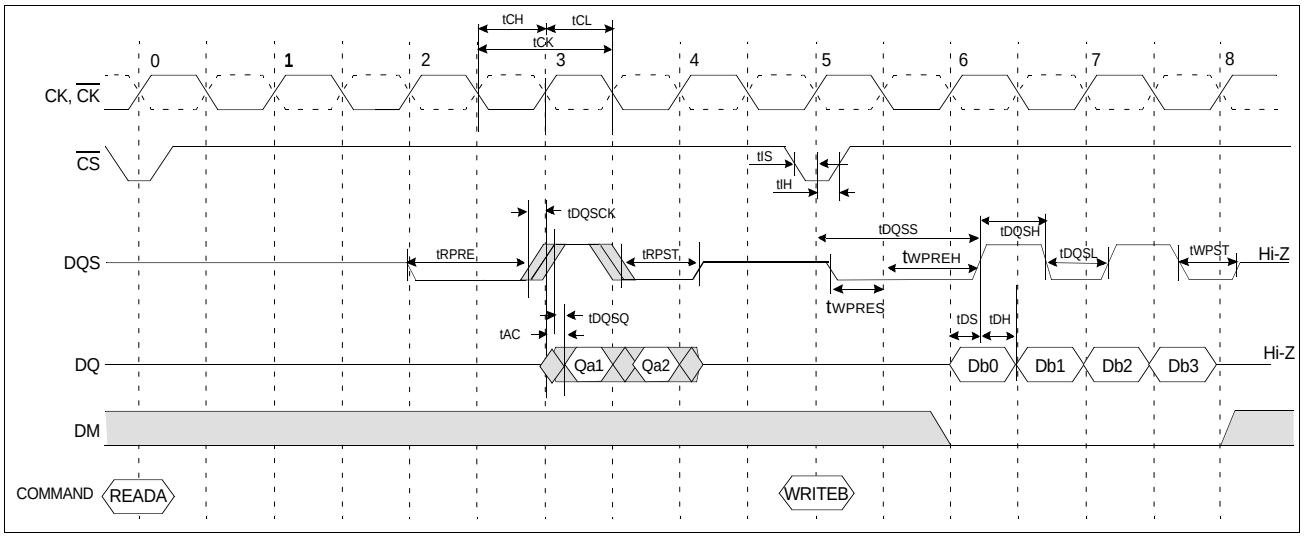
Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 + 0.01	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 + 0.01	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

AC CHARACTERISTICS

Parameter		Symbol	-55		-60		-70		Unit	Note
			Min	Max	Min	Max	Min	Max		
CK cycle time	CL=3	tCK	5.5	8	6	8	7	8	ns	
CK high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK		tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns	
Output access time from CK		tAC	-0.75	+0.75	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to output data edge		tDQSQ	-	0.5	-	0.5	-	0.5	ns	1
Read preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-In setup time		tWPRES	0	-	0	-	0	-	ns	
DQS-in hold time		tWPREH	0.25	-	0.25	-	0.25	-	tCK	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-In high level width		tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-In low level width		tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Address and Control input setup time		tIS	1.2	-	1.2	-	1.2	-	ns	
Address and Control input hold time		tIH	0.9	-	0.9	-	0.9	-	ns	
DQ and DM setup time to DQS		tDS	0.5	-	0.5	-	0.5	-	ns	
DQ and DM hold time to DQS		tDH	0.5	-	0.5	-	0.5	-	ns	
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1
Output DQS valid window		tQH	tHP-0.75ns	-	tHP-0.75ns	-	tHP-0.75ns	-	ns	1

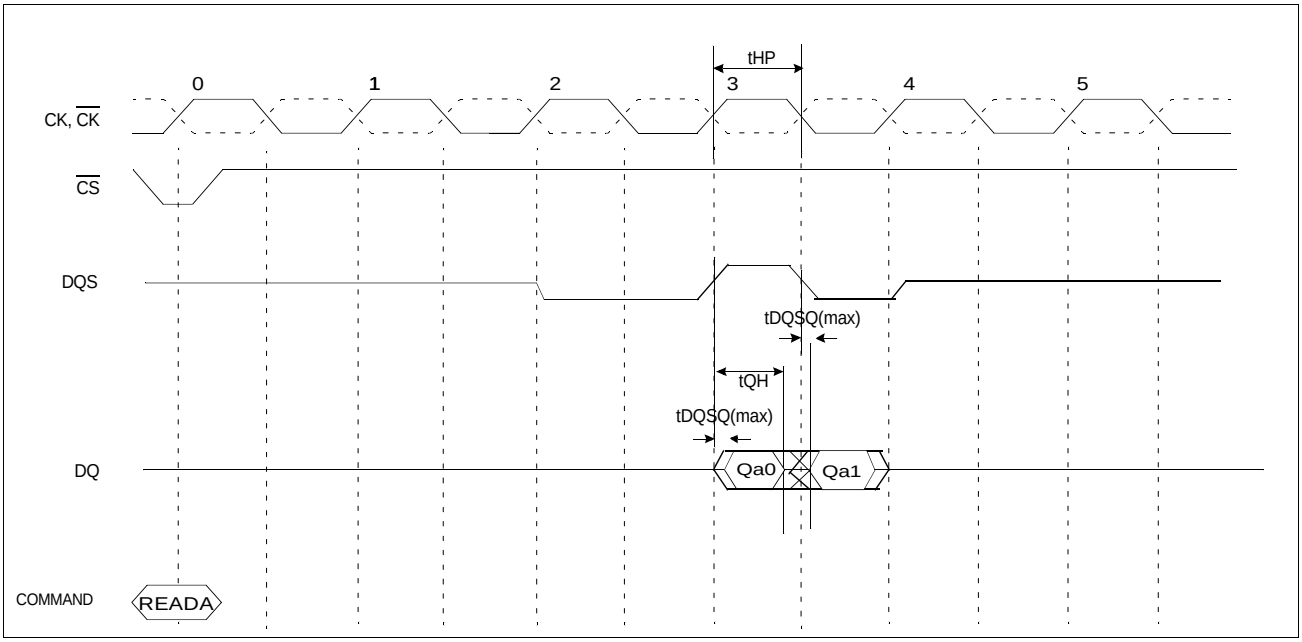
Simplified Timing @ BL=2, CL=3



Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output vaild window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is difined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
  . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)
  . X=A frequency dependent timing allowance account for tDQSQmax

tQH Timing (CL3, BL2)

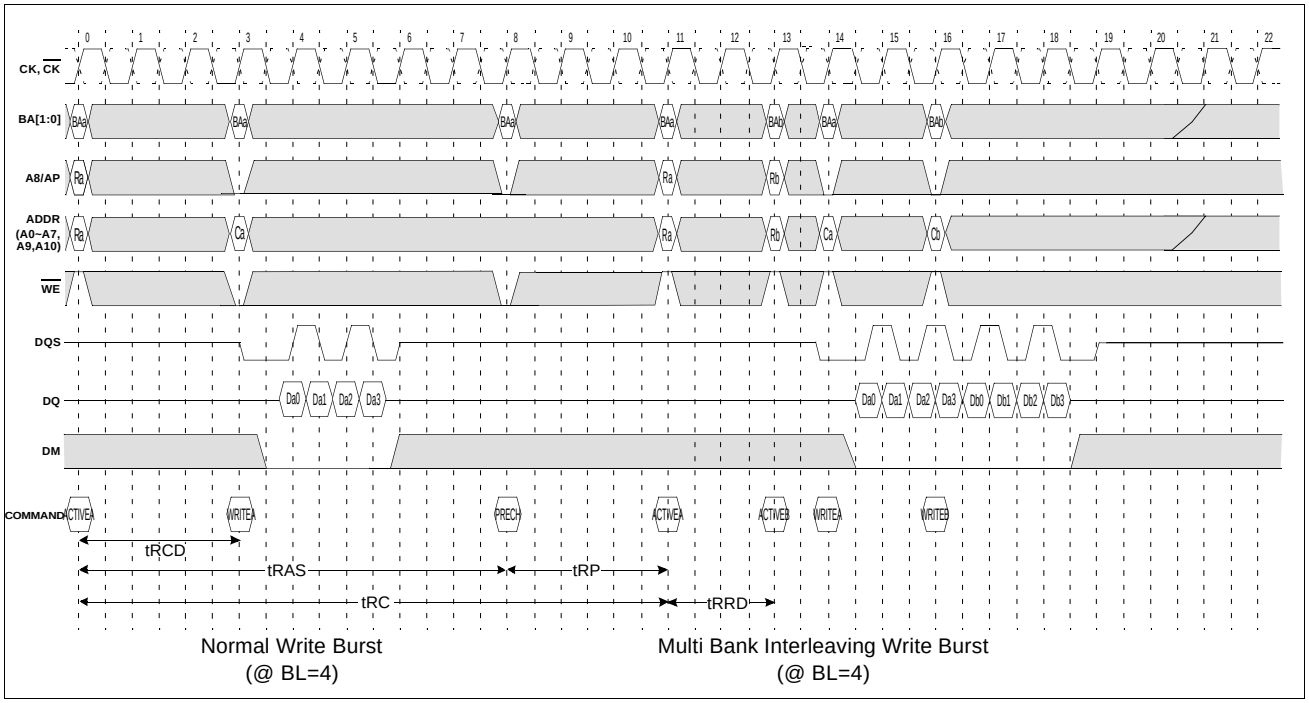


AC CHARACTERISTICS

Parameter	Symbol	-55		-60		-70		Unit	Note
		Min	Max	Min	Max	Min	Max		
Row cycle time	tRC	60.5		60		70		ns	
Refresh row cycle time	tRFC	71.5		72		84		ns	
Row active time	tRAS	44	100K	42	100K	49	100K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD	22		18		21		ns	
Row precharge time	tRP	16.5		18		21		ns	
Row active to Row active delay	tRRD	11		12		14		ns	
Last data in to Row precharge	tWR	2		2		2		tCK	1
Last data in to Read command delay	tCDLR	2		2		2		tCK	1
Col. address to Col. address delay	tCCD	1		1		1		tCK	
Mode register set cycle time	tMRD	2		2		2		tCK	
Power down exit time	tPEDX	1tCK+tIS		1tCK+tIS		1tCK+tIS		ns	
Self refresh exit to active command delay	tXSA	71.5		72		84		ns	
Self refresh exit to read command delay	tXSR	200			200			tCK	
Auto precharge write recovery + Precharge	tDAL	5		5		5		tCK	
Refresh interval time	tREF	7.8		7.8		7.8		us	

1. Note : For normal write operation, even numbers of Din are to be written inside DRAM

Simplified Timing(2) @ BL=4, CL=3

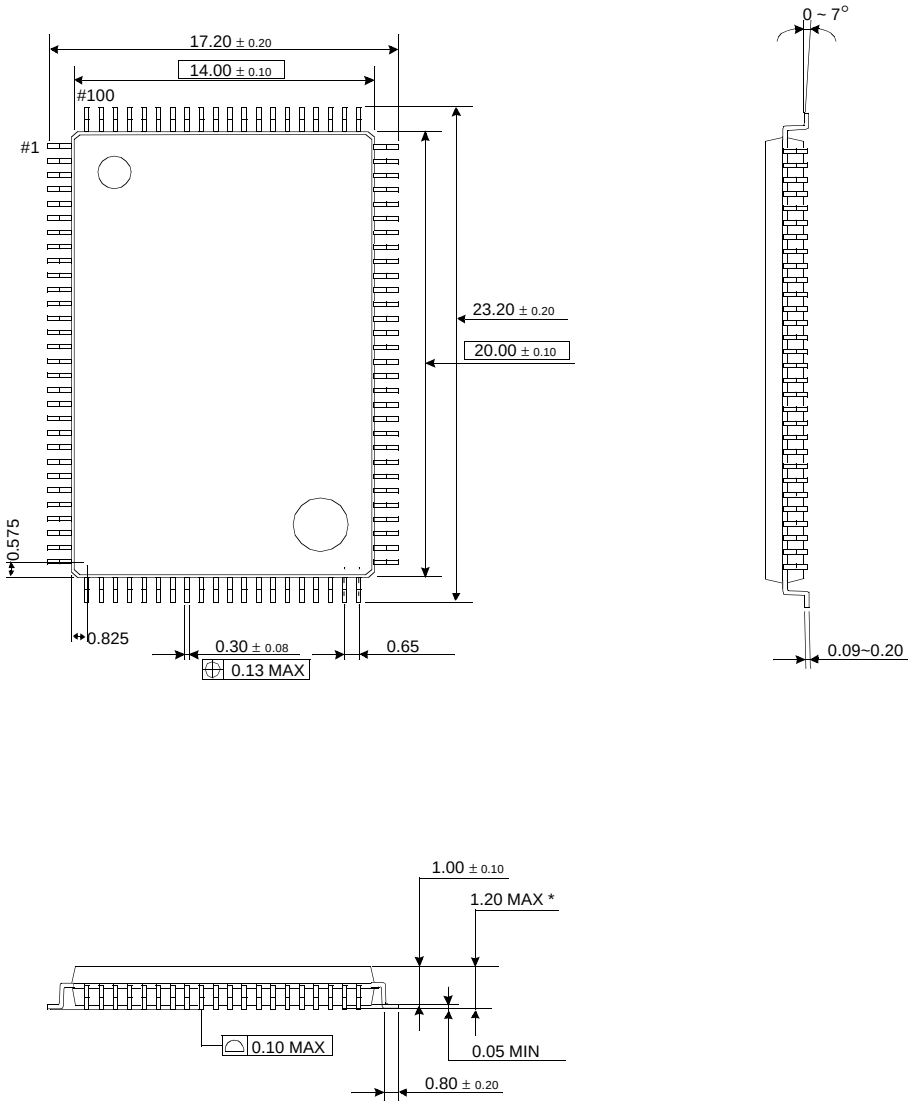


Normal Write Burst (@ BL=4)

Multi Bank Interleaving Write Burst (@ BL=4)

PACKAGE DIMENSIONS (TQFP)

Dimensions in Millimeters



Device Operation & Timing Diagram

BURST MODE OPERATION

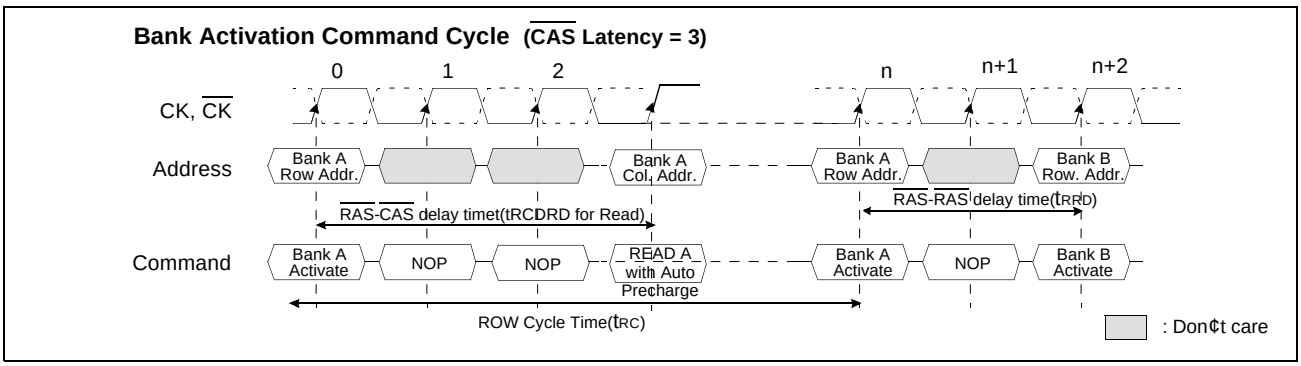
Burst mode operation is used to provide a constant flow of data to memory locations(write cycle), or from memory locations(read cycle). There are two parameters that define how the burst mode operates. These parameters including burst sequence and burst length are programmable and determined by address bits A_0 ~ A_3 during the Mode Register Set command. The burst type is used to define the sequence in which the burst data will be delivered or stored to the DDR SDRAM. Two types of burst sequences are supported, sequential and interleaved. See the below table. The burst length controls the number of bits that will be output after a read command, or the number of bits to be input after a write command. The burst length can be programmed to have values of 2, 4, 8 or Full page. For the full page operation, the starting address must be an even number.and burst is wrap-around at the end of burst.

BURST LENGTH AND SEQUENCE

Burst Length	Starting Address(A_2, A_1, A_0)	Sequential Mode	Interleave Mode
2	xx0	0, 1	0, 1
	xx1	1, 0	1, 0
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BANK ACTIVATION COMMAND

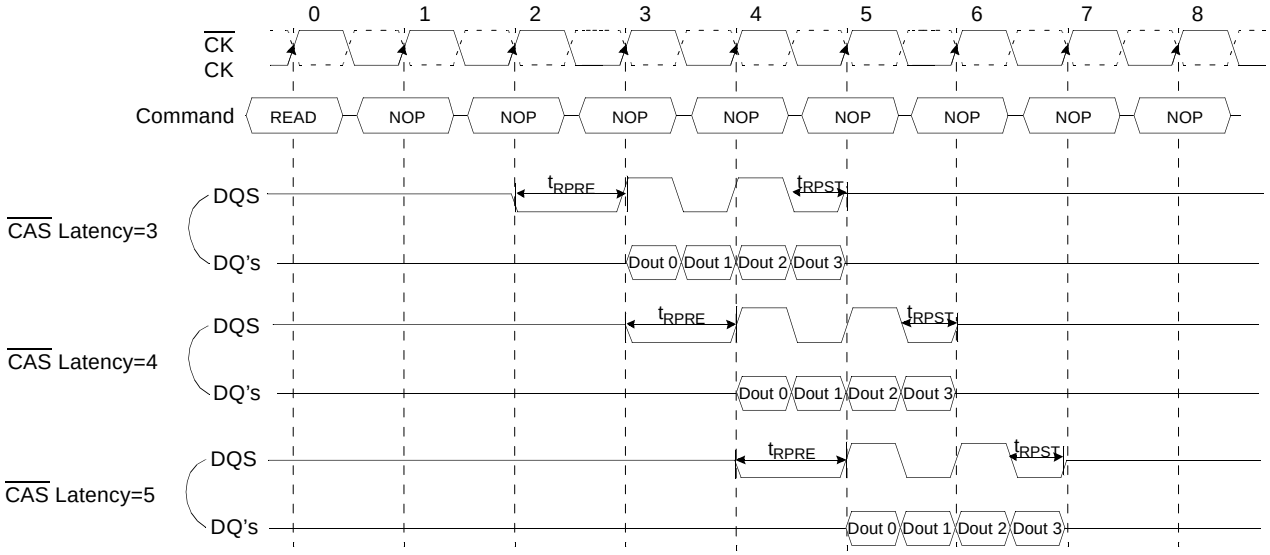
The Bank Activation command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The DDR SDRAM has four independent Banks, so two Bank Select addresses(BA_0, BA_1) are supported. The Bank Activation command must be applied before any Read or Write operation is executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time(t_{RCDRD} / t_{RCDWR} min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(t_{RRD} min).



BURST READ OPERATION

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the Burst read command is issued by asserting $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs (A_0~A_7) determine the starting address for the Burst. The Mode Register sets type of burst(sequential or interleave) and burst length(2, 4, 8, Full page). The first output data is available after the $\overline{CAS}$ Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe adopted by DDR SDRAM until the burst length is completed.

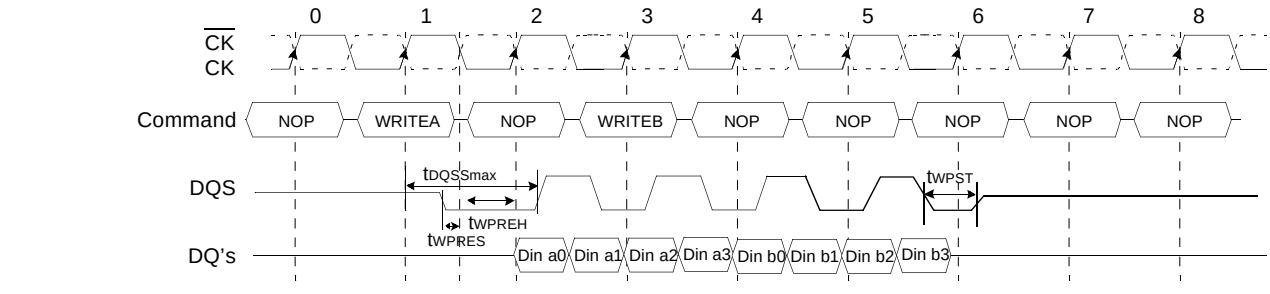
< Burst Length=4, $\overline{CAS}$ Latency= 3,4,5 >



BURST WRITE OPERATION

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. There is no real write latency required for burst write cycle. The first data for burst write cycle must be applied at the first rising edge of the data strobe enabled after t_{DQSS} from the rising edge of the clock that the write command is issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

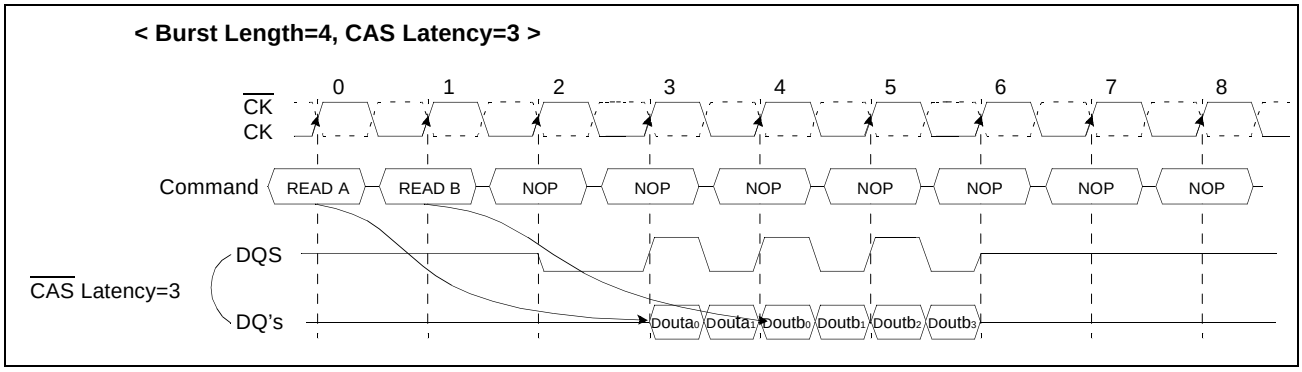
< Burst Length=4 >



BURST INTERRUPTION

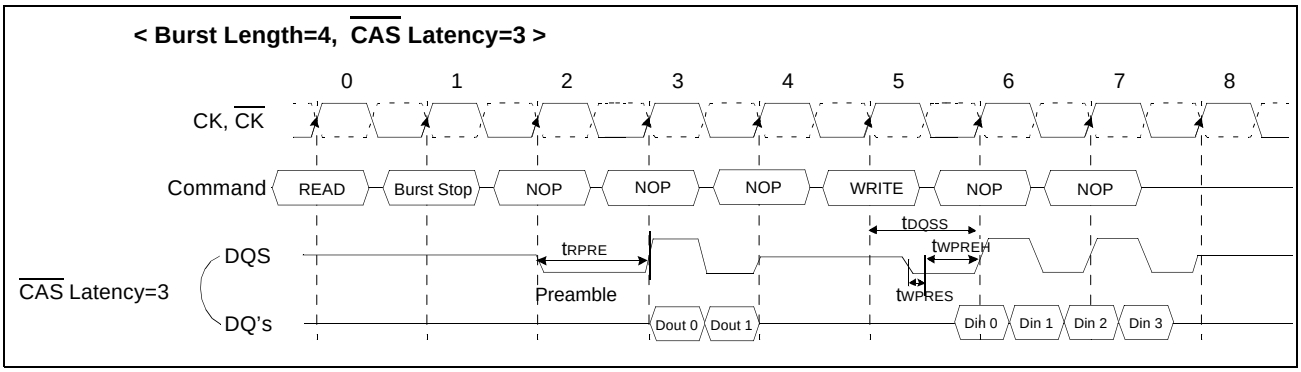
Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. Read to Read interval is minimum 1 tck.



Read Interrupted by Burst stop & a Write

To interrupt a burst read with a write command, Burst stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state at least one clock cycle before the Write command is initiated. Refe to the below for the READ to WRITE latency without the burst stop between Read and Write command.



Read to write command latency at no burst stop between read and write command.

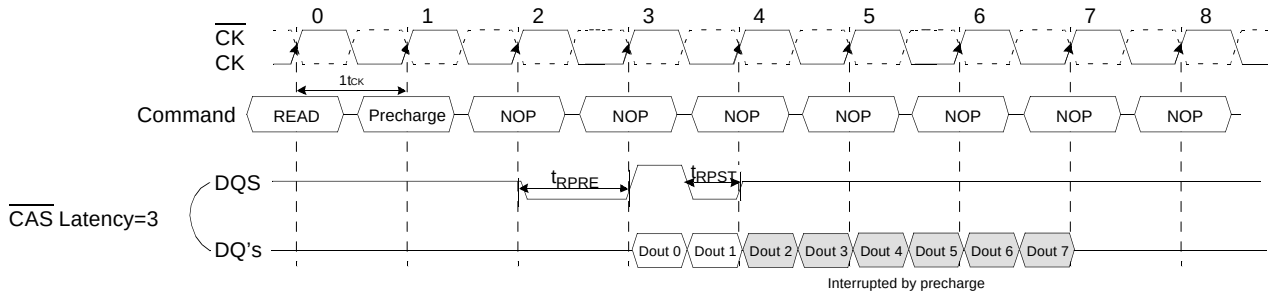
	CL3	CL4	CL5
BL2	5	6	7
BL4	6	7	8
BL8	8	9	10

(Clock)

Read Interrupted by a Precharge

A Burst Read operation can be interrupted by precharge of the same bank. The minimum 1 clock cycle is required for the read to precharge interval. A precharge command to output disable latency is equivalent to the CAS latency.

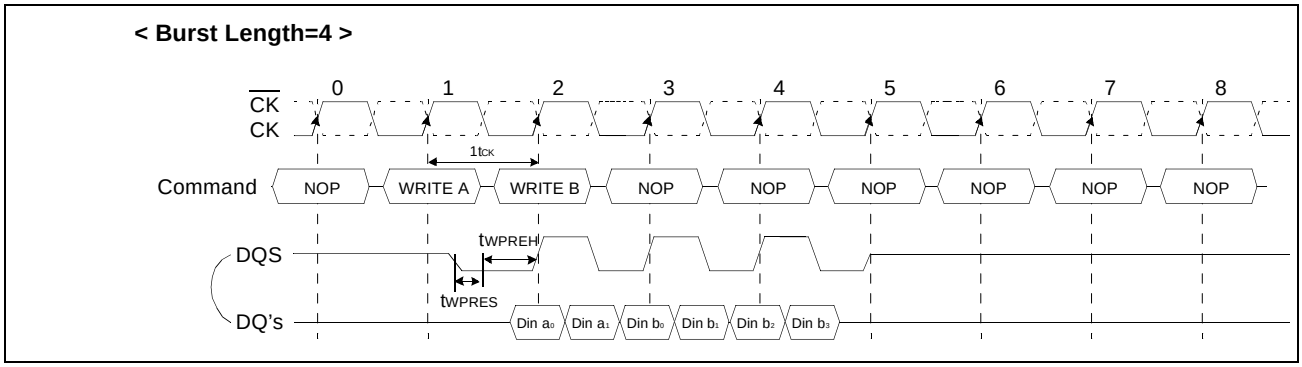
< Burst Length=8, $\overline{CAS}$ Latency=3 >



Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by the new Write Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

< Burst Length=4 >

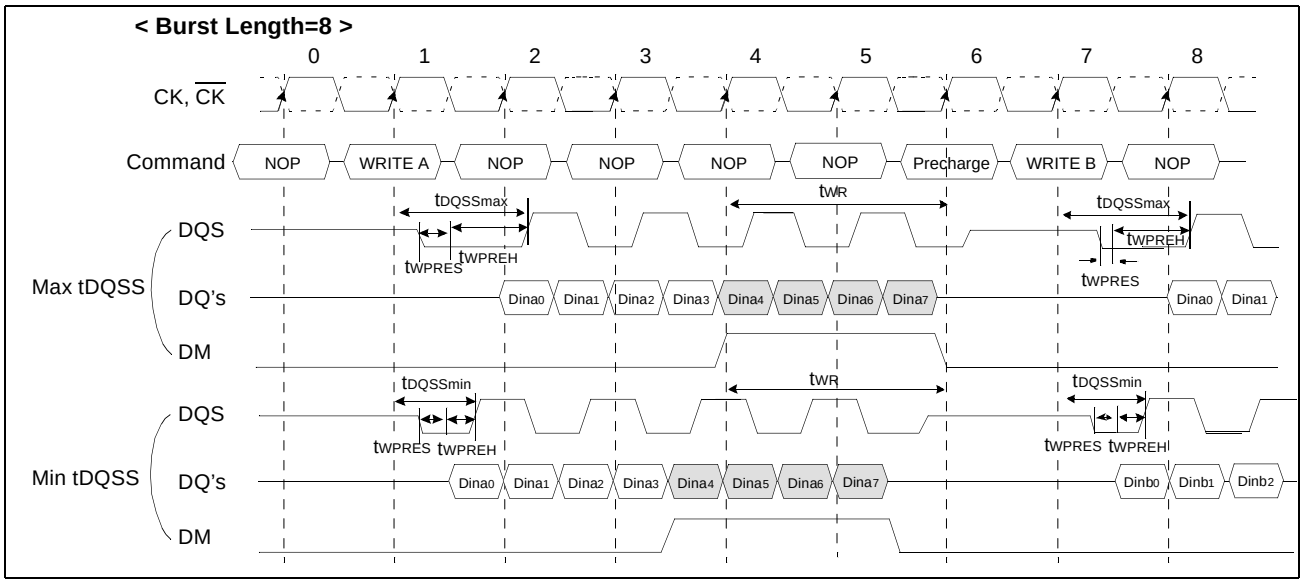


Write Interrupted by a Read & DM

- Write Interrupted by a Read function is not supported .

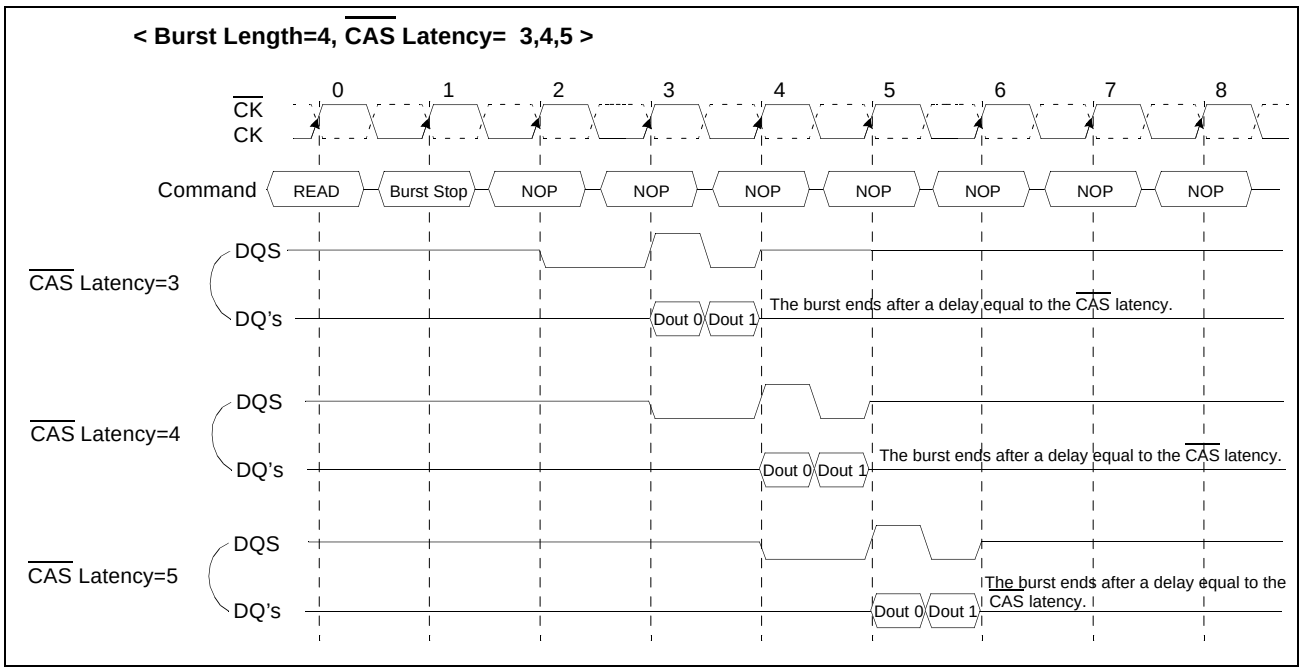
Write Interrupted by a Precharge & DM

A Burst Write operation can be interrupted before completion of the burst by a precharge of the same bank. A Write Recovery time(tWR) is required before a Precharge command to finish the Write operation. When Precharge command is asserted, any residual data from the burst write cycle must be masked by DM.



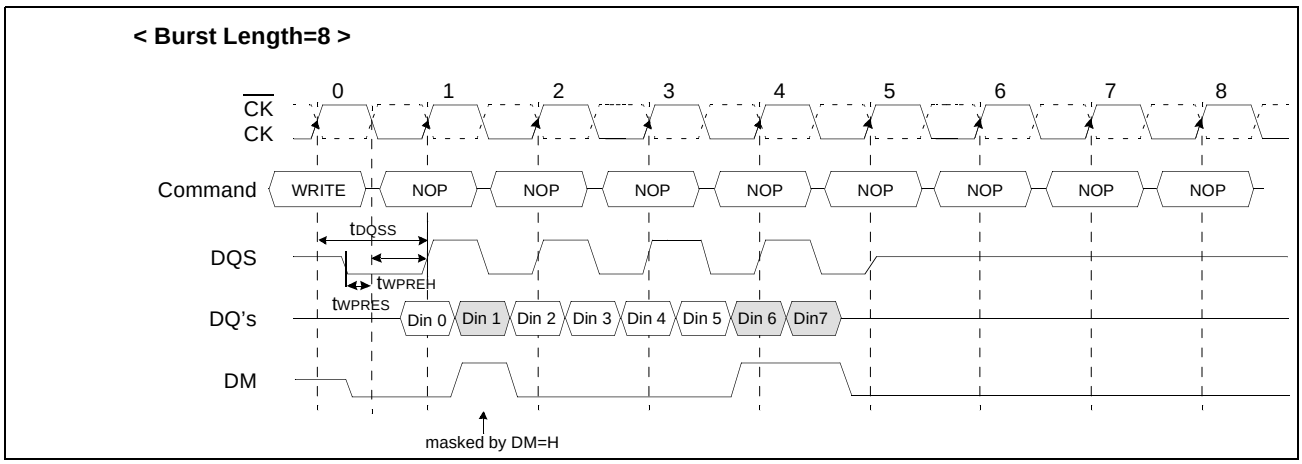
BURST STOP COMMAND

The Burst stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock only . The Burst Stop command has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a burst read cycle, both the data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ Latency set in the Mode Register. The Burst Stop command, however, is not supported during a write burst operation.



DM FUNCTION

The DDR SDRAM has a Data mask function that can be used in conjunction with data Write cycle only, not Read cycle. When the Data Mask is activated (DM high) during write operation the write data is masked immediately(DM to Data-mask Latency is zero).
DM must be issued at the rising edge or the falling edge of Data Strobe instead of a clock edge.

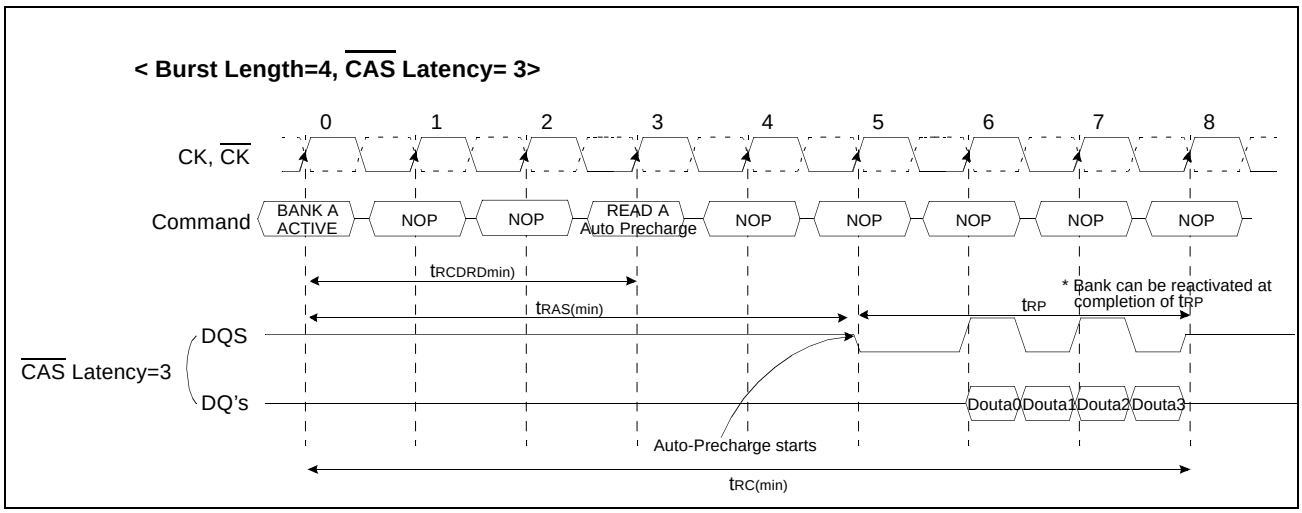


AUTO-PRECHARGE OPERATION

The Auto precharge command can be issued by having column address A8 High when a Read or a Write command is asserted into the DDR SDRAM. If A8 is low when Read or Write command is issued, then normal Read or Write burst operation is asserted and the bank remains active after the completion of the burst sequence. When the Auto precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during read or write cycle after tRAS(min) is satisfied.

Read with Auto Precharge

If a Read with Auto-precharge command is initiated, the DDR SDRAM automatically starts the precharge operation on BL/2 clock later from a Read with Auto-Precharge command when tRAS(min) is satisfied. If not, the start point of precharge operation will be delayed until tRAS(min) is satisfied. Once the precharge operation has started the bank cannot be reactivated and the new command can not be asserted until the Precharge time(tRP) has been satisfied.



When the Read with Auto precharge command is issued, new command can be asserted at T4,T5 and T6 respectively as follows.

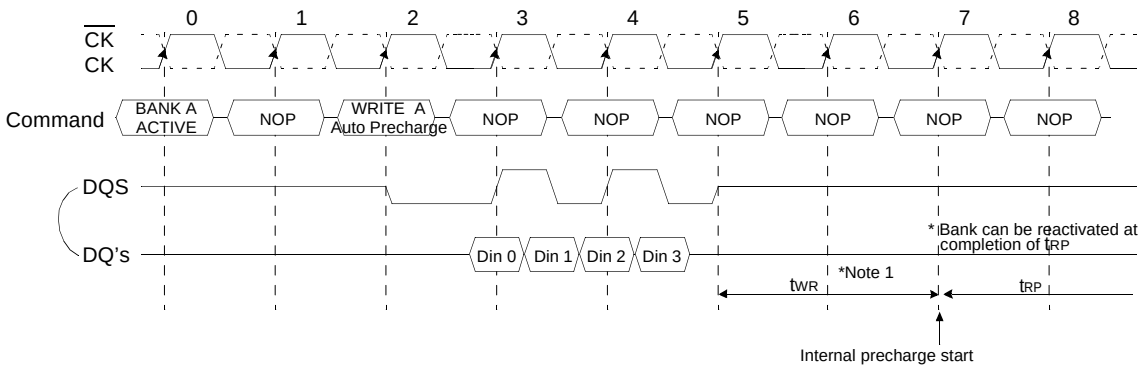
Asserted command	For same Bank			For Different Bank		
	4	5	6	4	5	6
READ	READ + No AP*1	READ+ No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

*1 : AP = Auto Precharge

Write with Auto Precharge

If A8 is high when Write command is issued , the write with Auto-Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping tWR(min).

< Burst Length=4 >



Asserted command	For same Bank						For Different Bank				
	3	4	5	6	7	8	3	4	5	6	7
WRITE	WRITE+ No AP*1	WRITE+ No AP	WRITE+ No AP	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE+ AP	WRITE+ AP	WRITE+ AP	WRITE+ AP	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	Illegal	Illegal	Illegal	READ+ NO AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal
READ+AP	Illegal	Illegal	Illegal	Illegal	READ + AP	Illegal	Illegal	Illegal	Illegal	Illegal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

Note : 1. For the case of tWR = 2 clock

PRECHARGE COMMAND

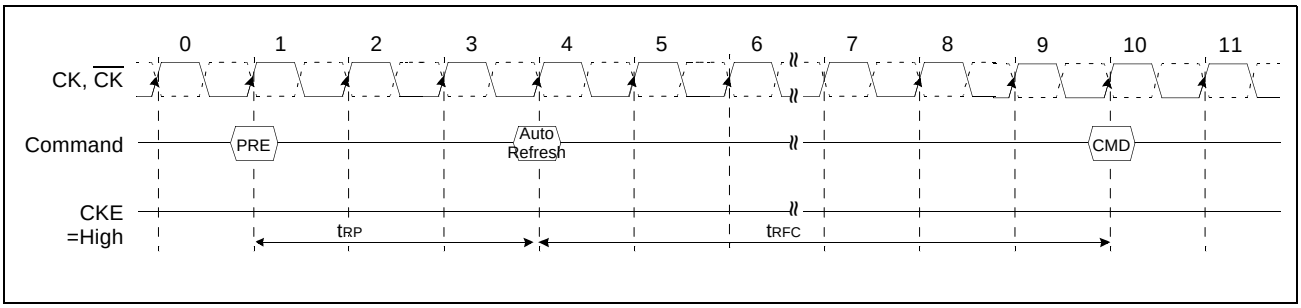
The precharge command is used to precharge or close a bank that has been activated. The precharge command is issued when CS, RAS and WE are low and CAS is high at the rising edge of the clock, CK. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank select addresses(BA_0, BA_1) are used to define which bank is precharged when the command is initiated. For write cycle, t_{WR}(min.) must be satisfied from the start of the last burst write cycle until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

< Bank Selection for Precharge by Bank address bits >

A_8/AP	BA1	BA_0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

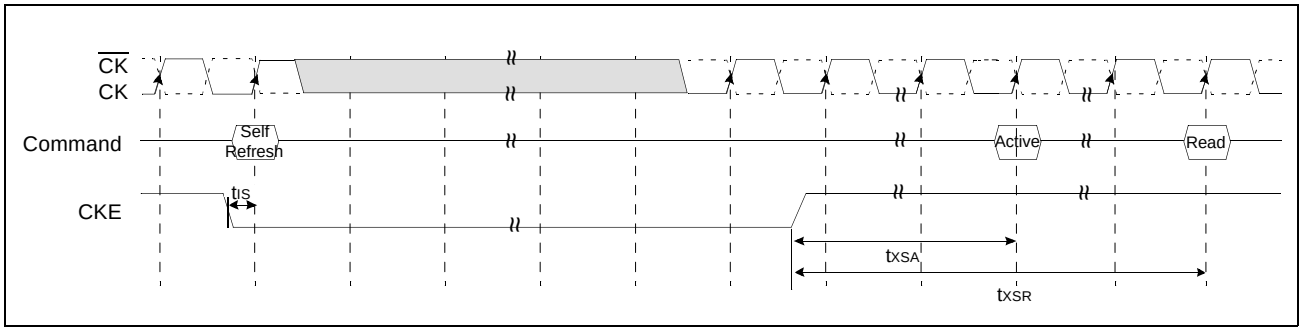
AUTO REFRESH

An Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ held low with CKE and $\overline{WE}$ high at the rising edge of the clock, CK. All banks must be precharged and idle for a t_{RP}(min) before the Auto Refresh command is applied. No control of the external address pins is required once this cycle has started because of the internal address counter. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the t_{RFC}(min).



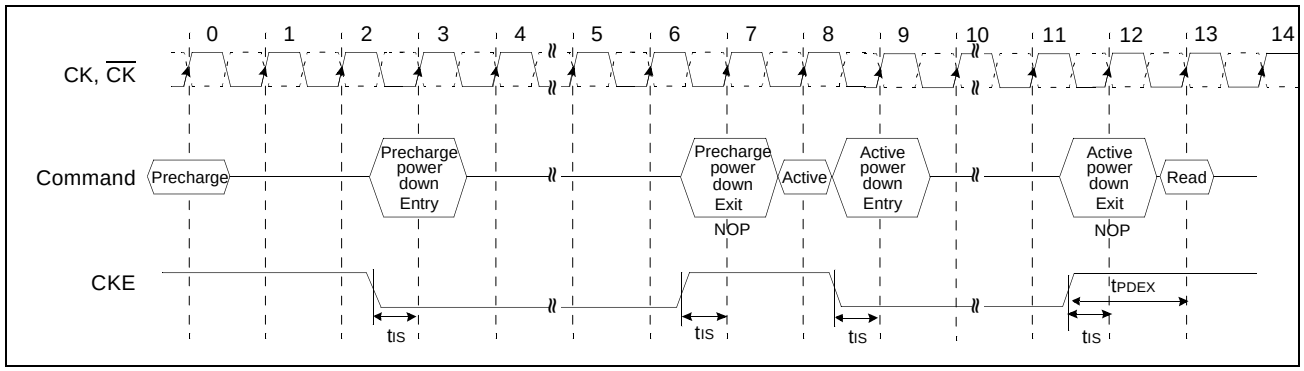
SELF REFRESH

A self refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock(CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than tXSR for locking of DLL.



POWER DOWN MODE

The power down is entered when CKE Low,and exited when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. The all banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1tCK+tIS prior to Row active command. During power down mode, refresh operations cannot be performed, therefore the device cannot remain in power down mode longer than the refresh period(tREF) of the device.



SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	$BA_{0,1}$	A_8/AP	Address*4	Note
Register	Extended Mode Register		H	X	L	L	L	L	X	OP CODE			1, 2
	Mode Register Set		H	X	L	L	L	L	X	OP CODE			
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address	5
	Auto Precharge Enable										H		5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address	5
	Auto Precharge Enable										H		5, 7
Burst Stop			H	X	L	H	H	L	X	X			8
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		6
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DM			H	X					V	X			9
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code.
A_0 ~ A_{10} & BA_0 ~ BA_1 : Program keys for 2Mx32 DDR (@EMRS/MRS)
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys for 4Mx32 DDR (@EMRS/MRS)

2. EMRS/MRS can be issued only at all banks precharge state.
A new command can be issued after 2 clock cycle of EMRS/MRS

3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.

4.

2Mx32 DDR	4Mx32 DDR
A_{10}~A_9, A_7~A_0	A_{11}~A_9, A_7~A_0

5. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
6. If A_8/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
7. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
8. Burst stop command is valid at every burst length.
9. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

FUNCTION TRUTH TABLE

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A_8	PRE/PREA	NOP*4
	L	L	L	H	X	REFA	AUTO-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA, CA, A_8	READ/READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TERM	Terminate Burst
	L	H	L	H	BA, CA, A_8	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP(Continue Burst END)
	L	H	H	H	X	NOP	NOP(Continue Burst END)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA, CA, A_8	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	Terminate Burst With DM=High, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst END)
	L	H	H	H	X	NOP	NOP(Continue Burst END)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO RECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
PRE-CHARGING	H	X	X	X	X	DESEL	NOP(Idle after t_{RP})
	L	H	H	H	X	NOP	NOP(Idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	NOP*4(Idle after t_{RP})
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP(ROW Active after t_{RCD})
	L	H	H	H	X	NOP	NOP(ROW Active after t_{RCD})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA, CA, A_8	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	New Write, Determine AP.
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	H	X	X	X	X	DESEL	NOP(Idle after t_{RP})
	L	H	H	H	X	NOP	NOP(Idle after t_{RP})
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS :

H=High Level, L=Low level, V=Valid, X=Dont Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Same Bank¢s previous Auto precharge will not be performed. But if Bank is different, previous Auto precharge will be performed.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action
SELF-REFRESHING	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh*1
	L	H	L	H	H	H	X	Exit Self-Refresh*1
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
Both Bank Precharge POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down*2
	L	H	L	H	H	H	X	Exit Power Down*2
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power Down)
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	H	X	X	X	X	Enter Power Down*3
	H	L	L	H	H	H	X	Enter Power Down*3
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row (& Bank) Active
	H	L	L	L	L	H	X	Enter Self-Refresh*3
	H	L	L	L	L	L	OP Code	Mode Register Access
	L	X	X	X	X	X	X	Refer to Current State=Power Down
Any State other than listed above	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle*4
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle*4
	L	L	X	X	X	X	X	Maintain Clock Suspend

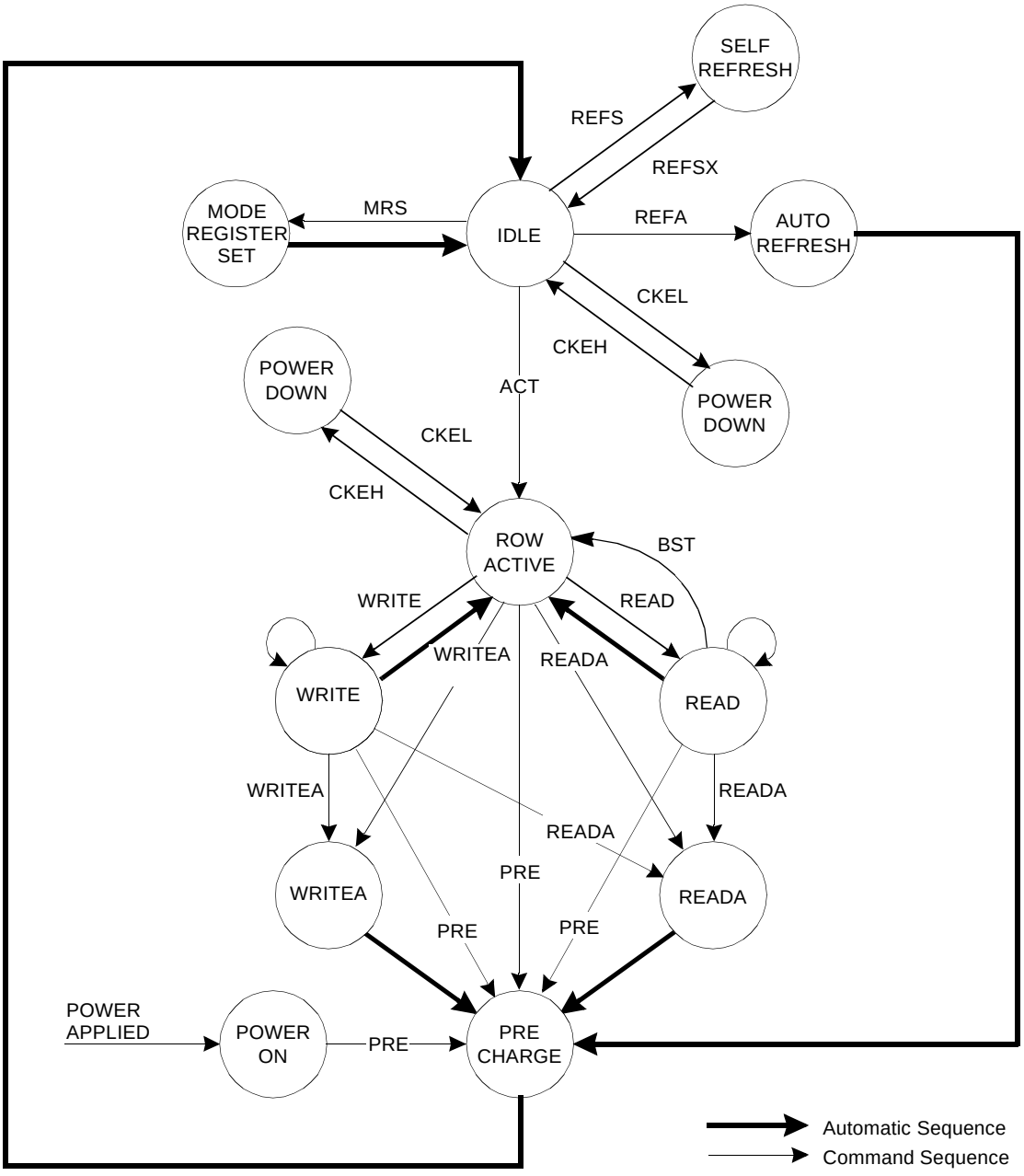
ABBREVIATIONS :

H=High Level, L=Low level, X=Don't Care

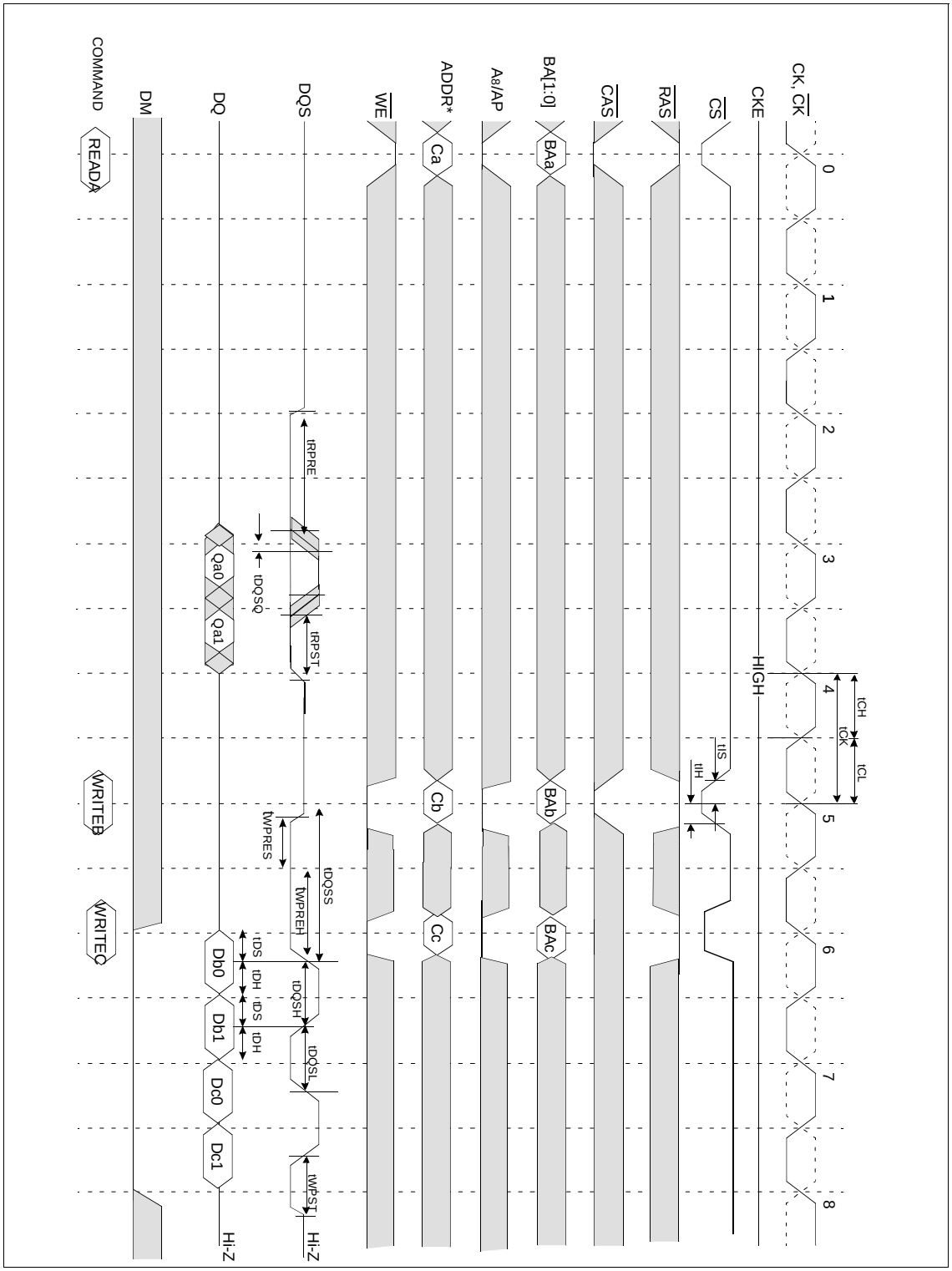
Note :

1. After CKE's low to high transition to exist self refresh mode. And a time of tRC(min) has to be elapse after CKE's low to high transition to issue a new command.
2. CKE low to high transition is asynchronous as if restarts internal clock.
   A minimum setup time "tSS + one clock" must be satisfied before any command other than exit.
3. Power-down and self refresh can be entered only from the all banks idle state.
4. Must be a legal command.

SIMPLIFIED STATE DIAGRAM



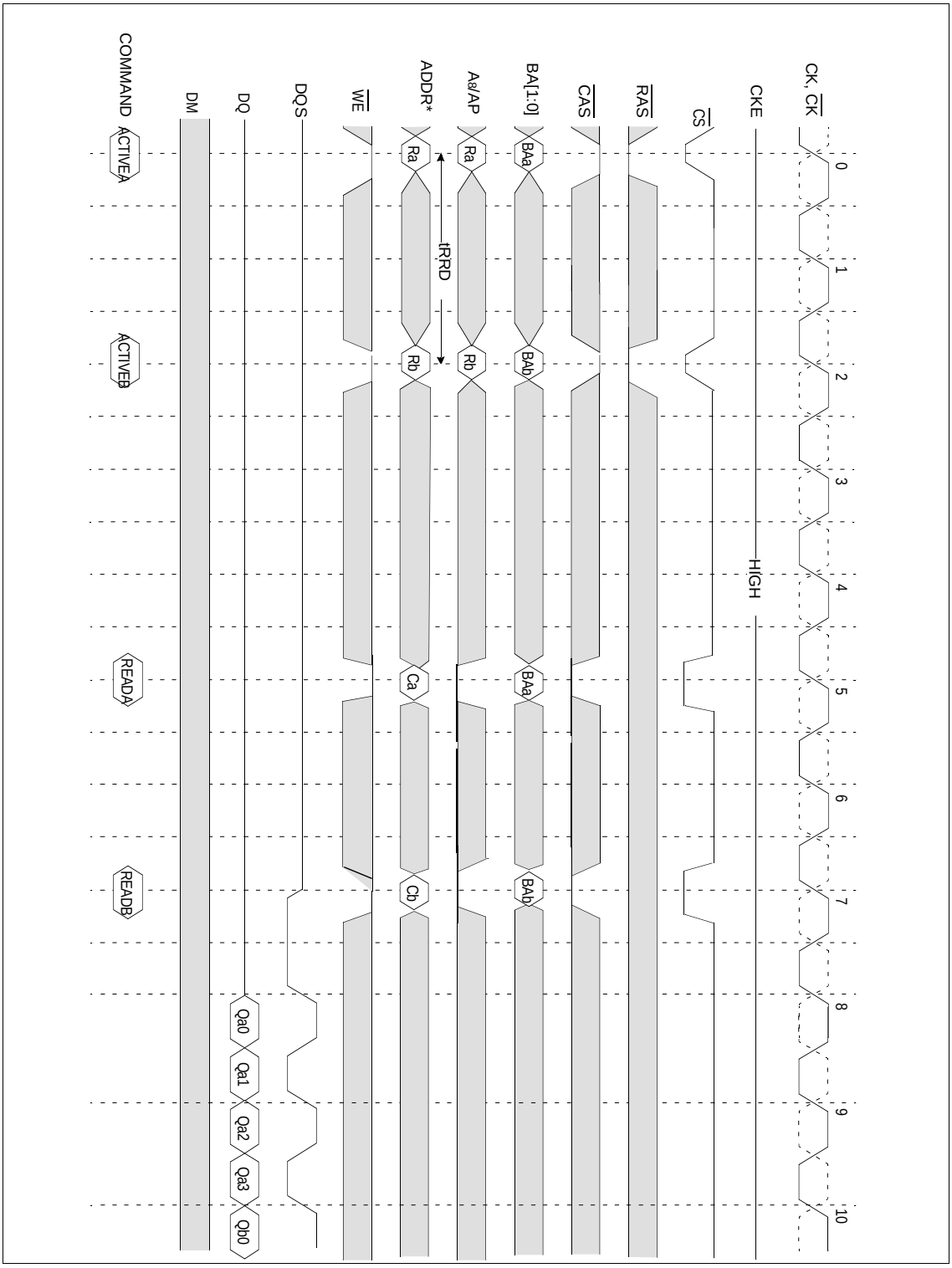
Basic Timing (Setup, Hold and Access Time @BL=2, CL=3)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

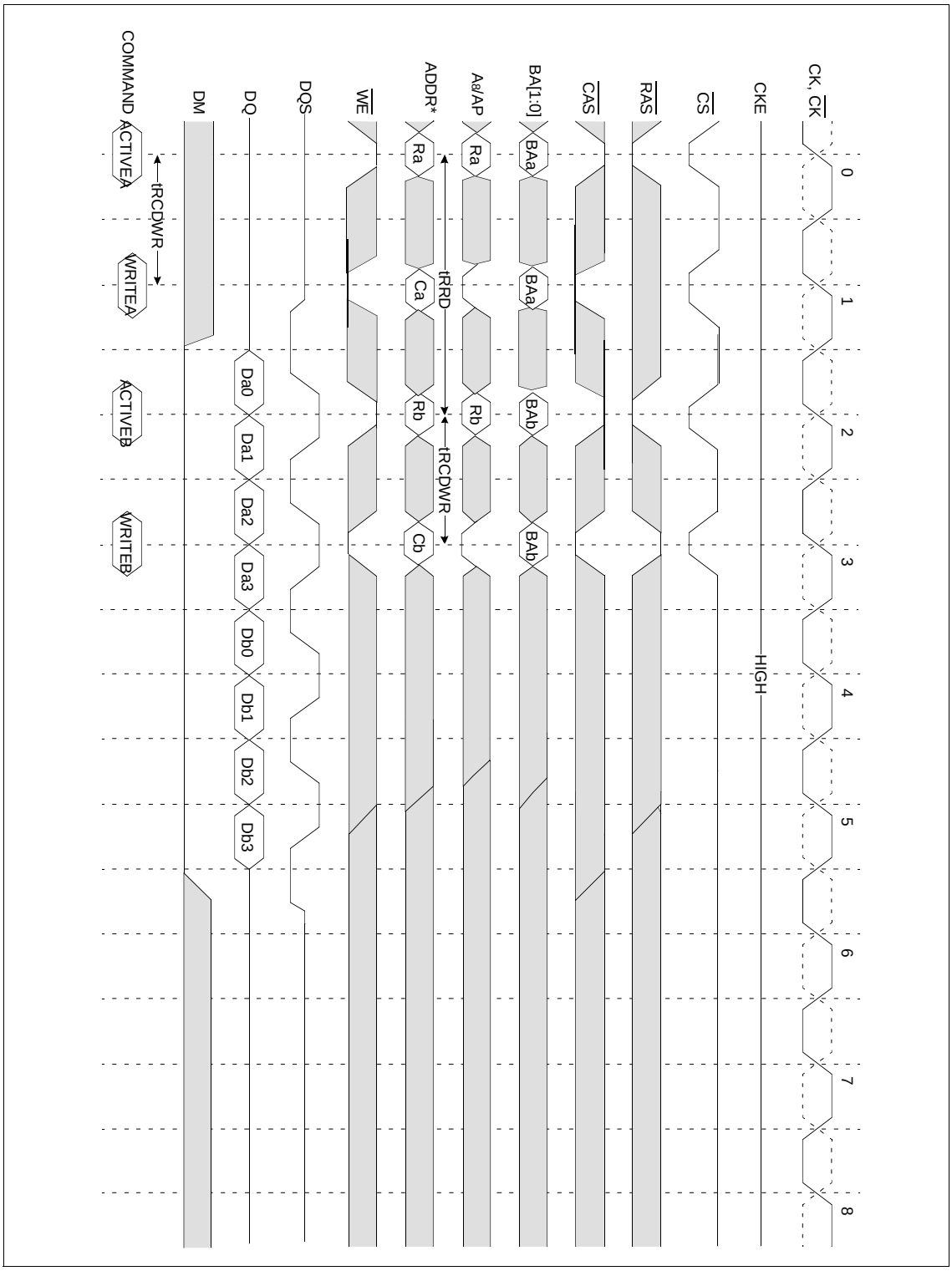
Multi Bank Interleaving READ (@BL=4, CL=3)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

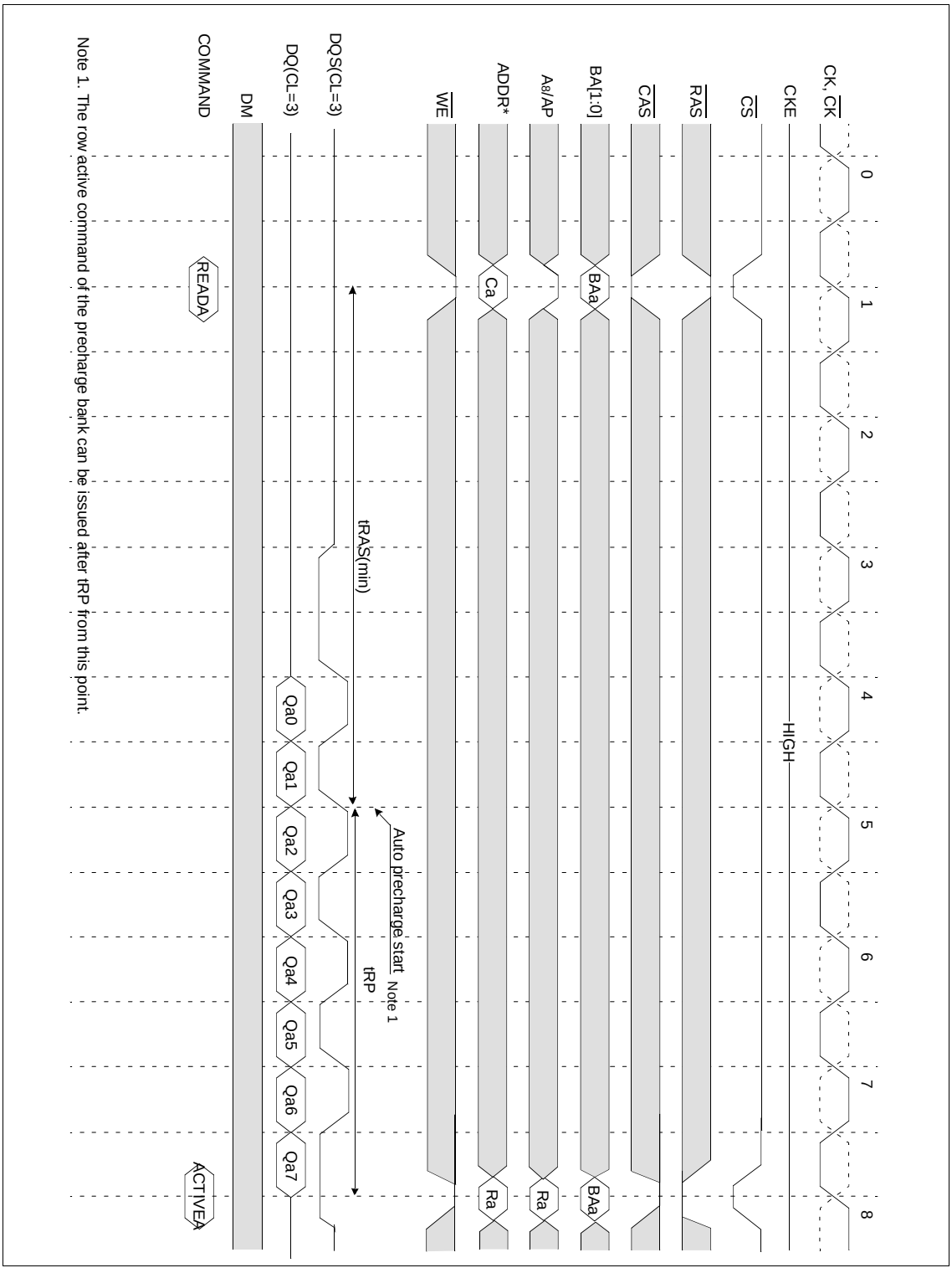
Multi Bank Interleaving WRITE (@BL=4, CL=3)



Note*

	2Mx32 DDR	4Mx32 DDR
	A10~A9, A7~A0	A11~A9, A7~A0

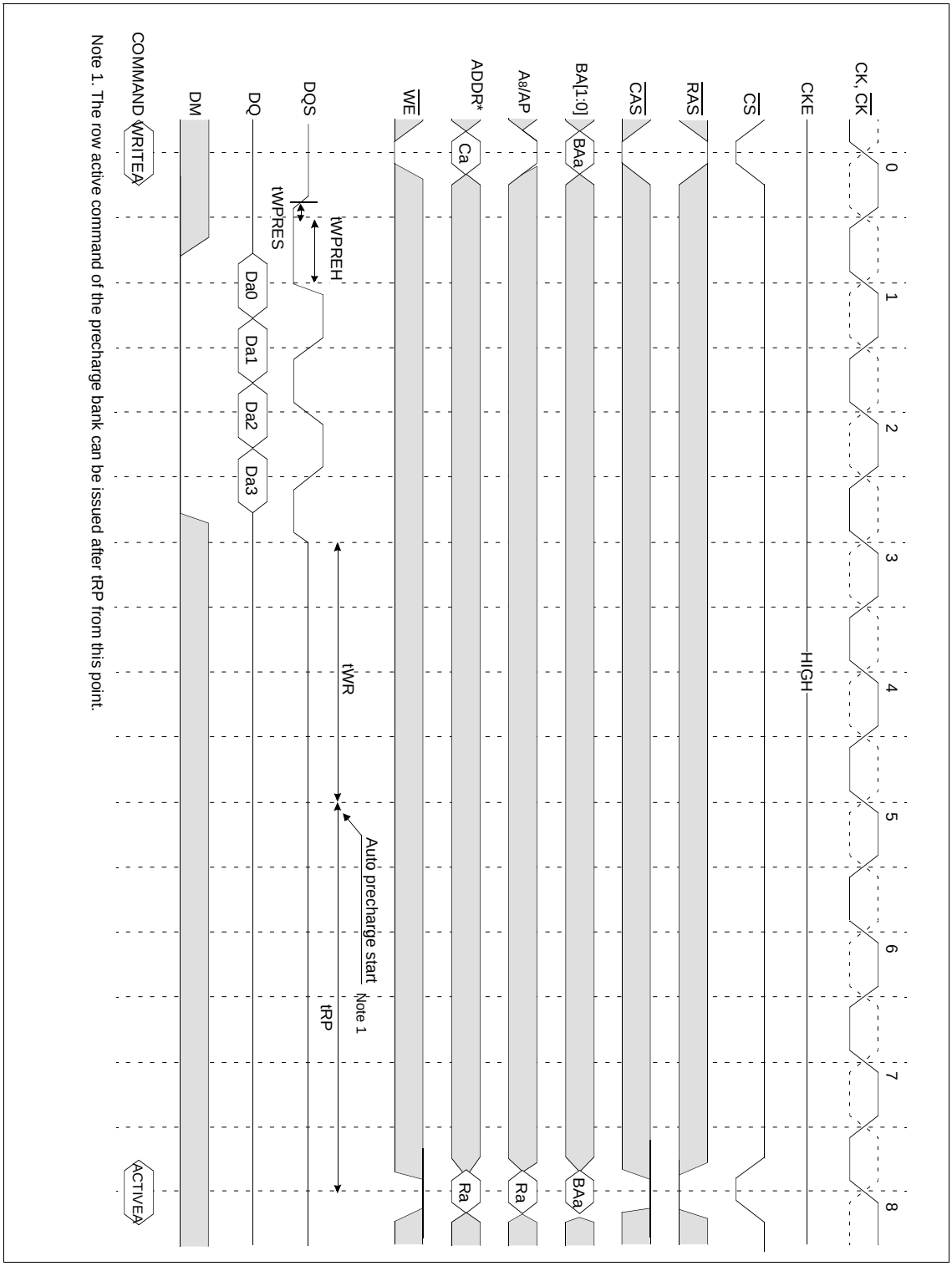
Auto Precharge after READ Burst (@BL=8)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

Auto Precharge after WRITE Burst (@BL=4)

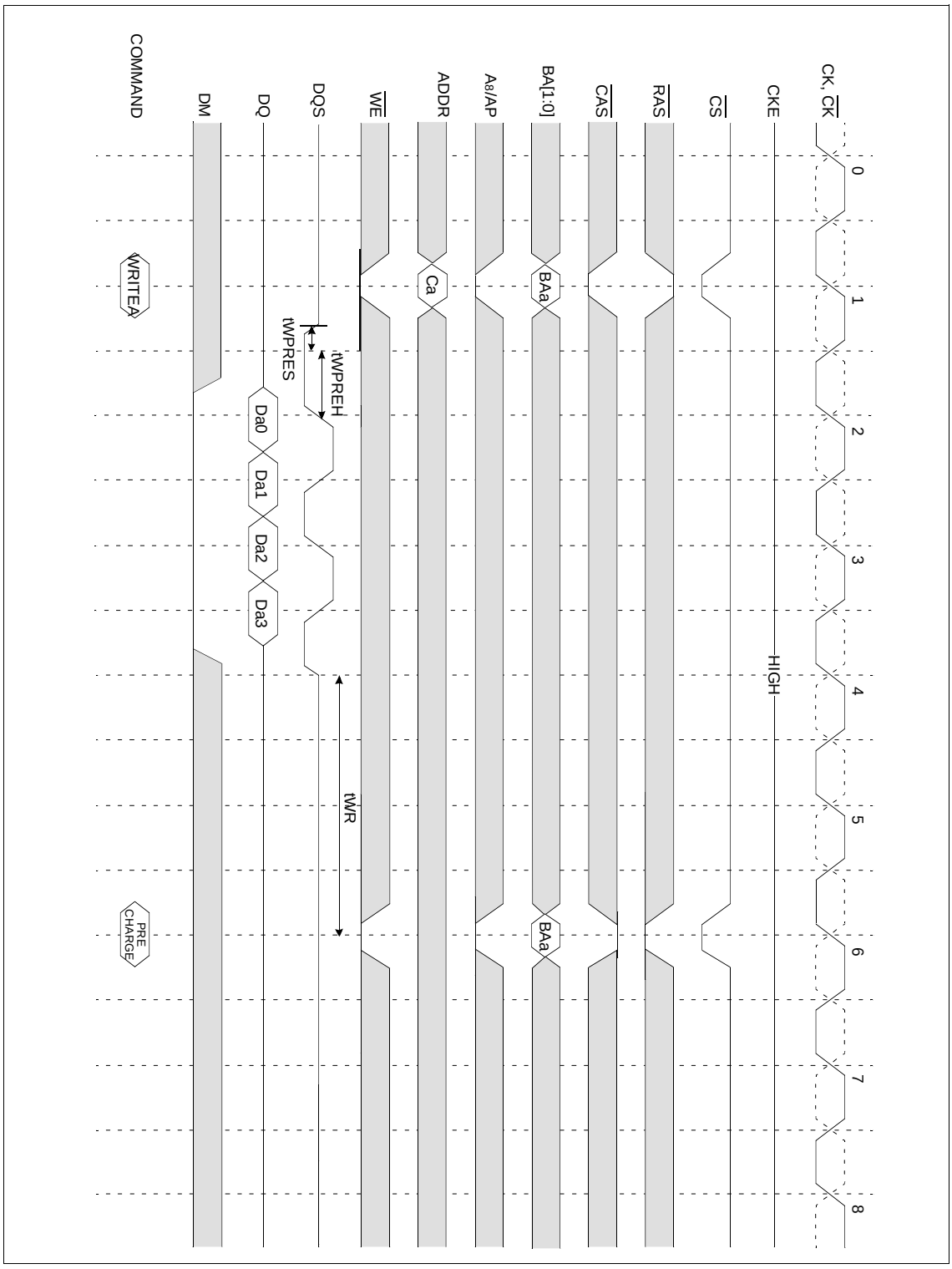


Note 1. The row active command of the precharge bank can be issued after tRP from this point.

Note*

2MX32 DDR	4MX32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

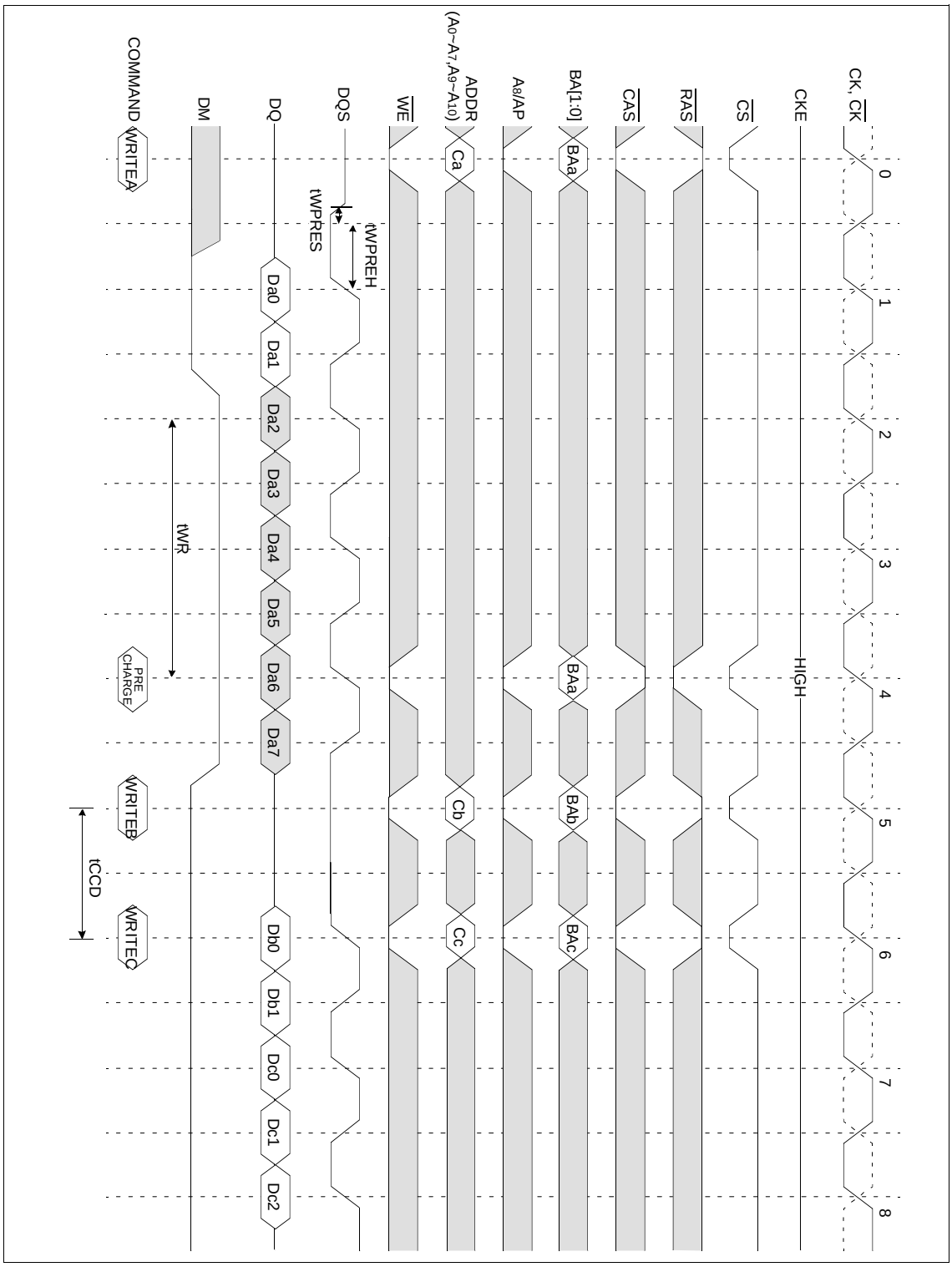
Normal WRITE Burst (@BL=4)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

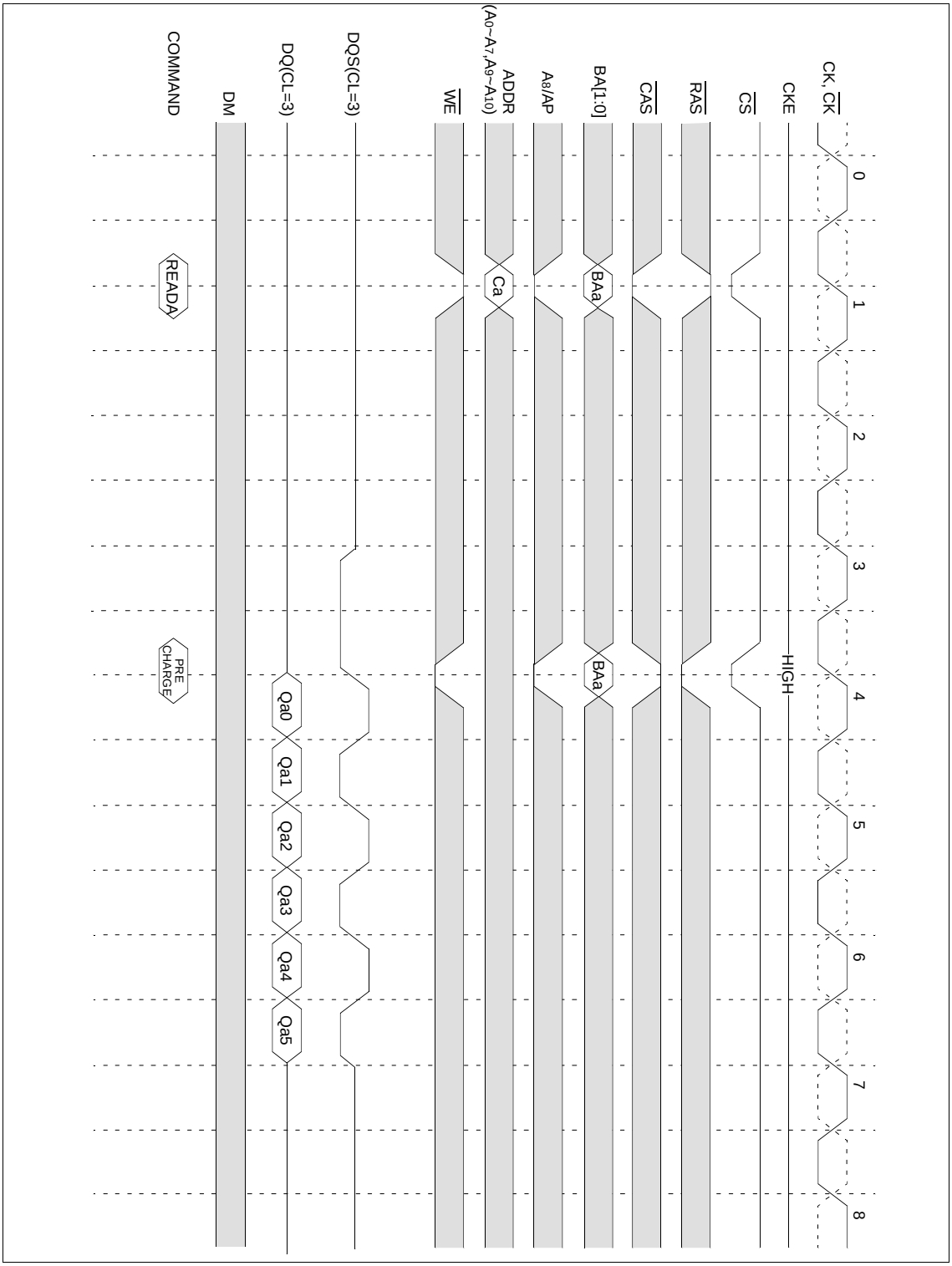
Write Interrupted by Precharge & DM (@BL=8)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

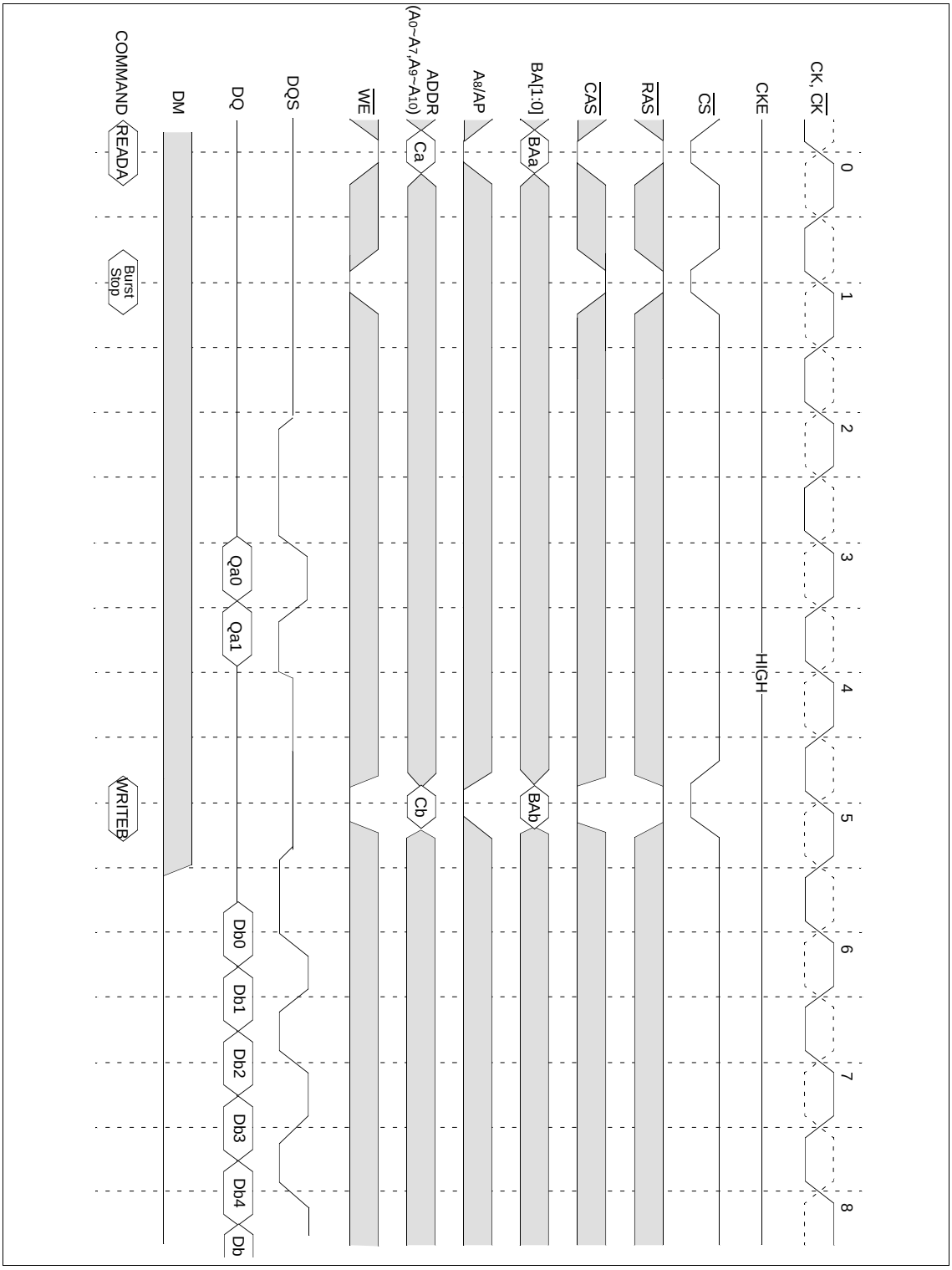
Read Interrupted by Precharge (@BL=8)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

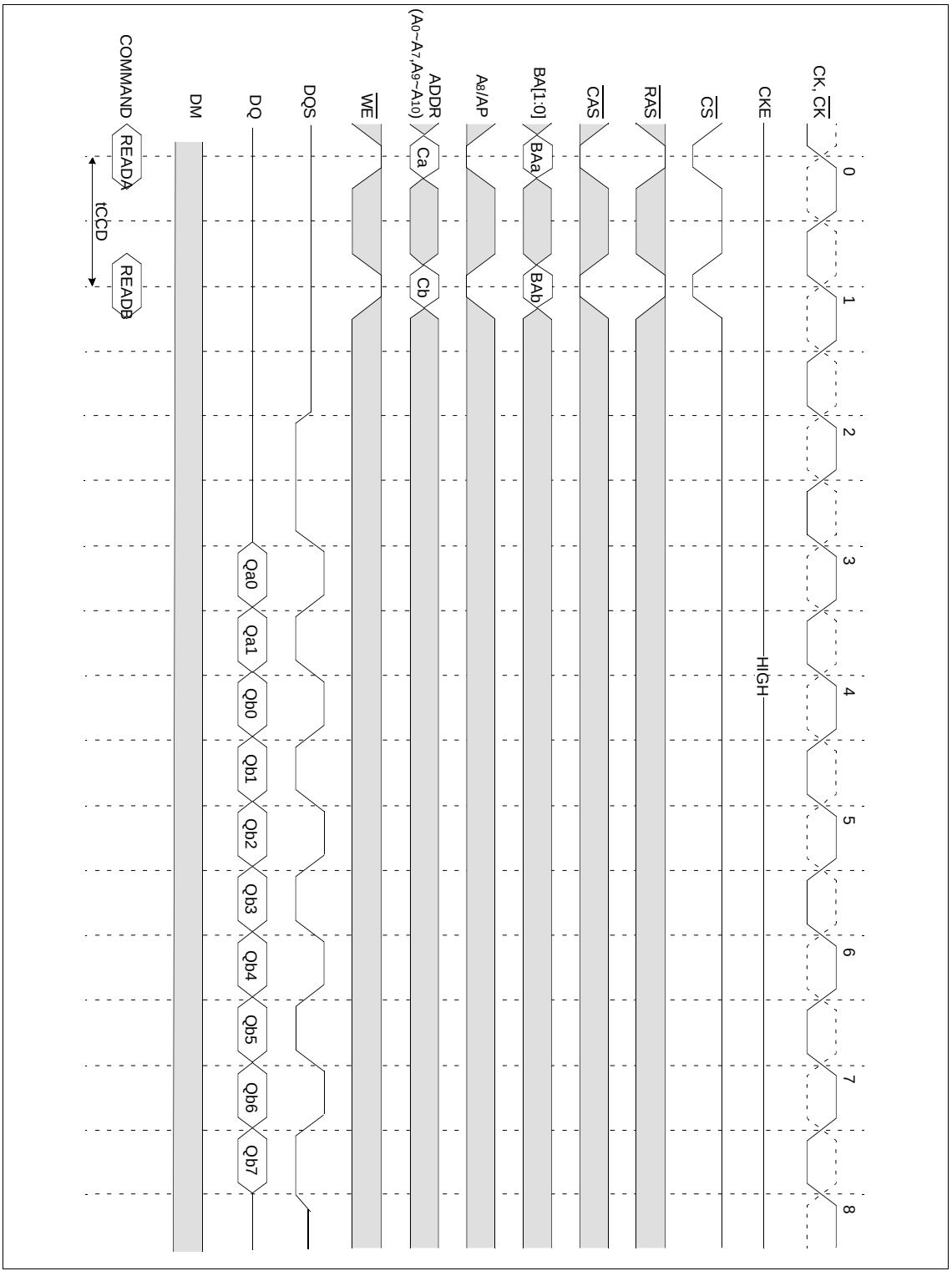
Read Interrupted by Burst stop & Write (@BL=8, CL=3)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

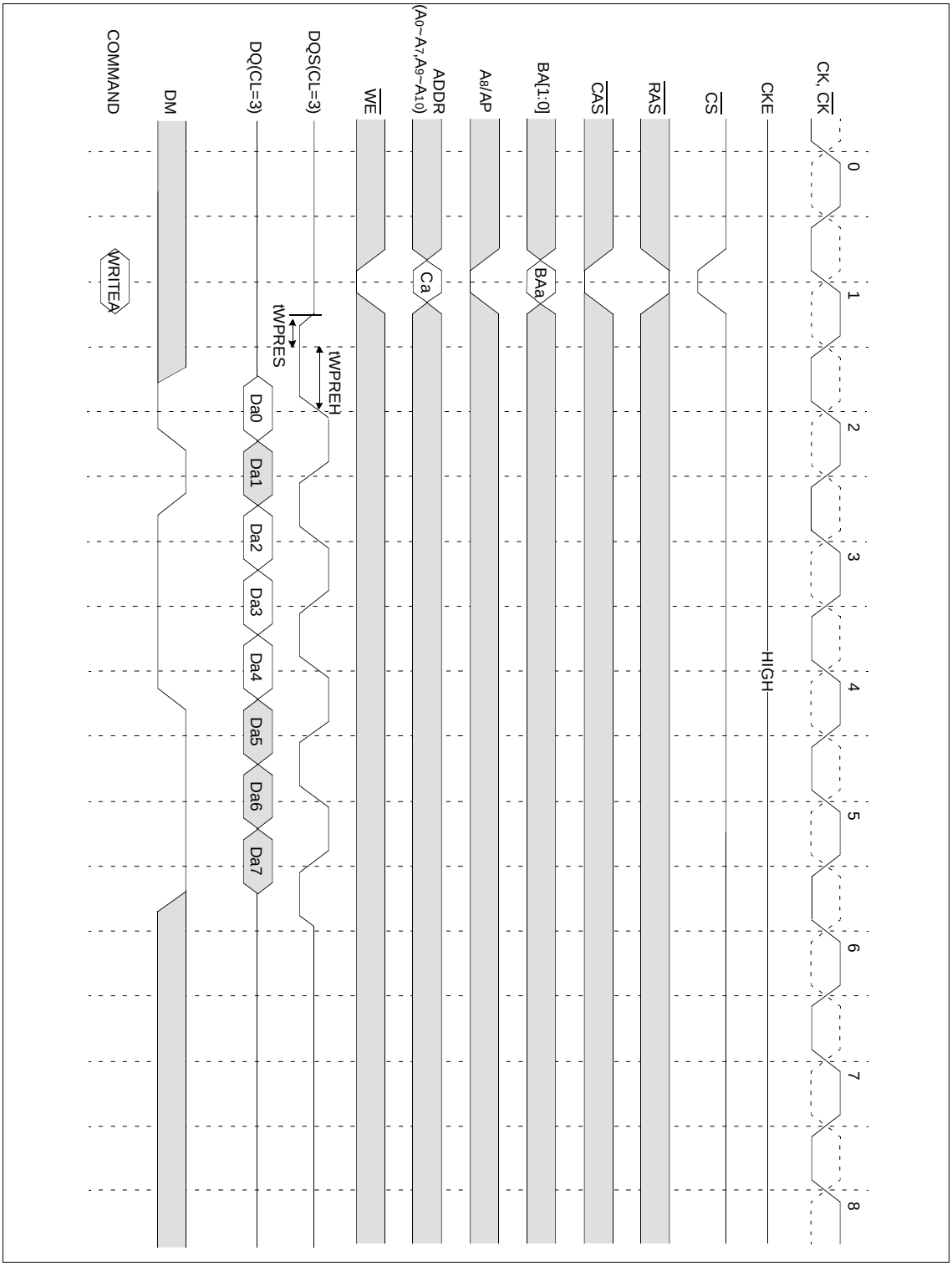
Read Interrupted by a Read (@BL=8, CL=3)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

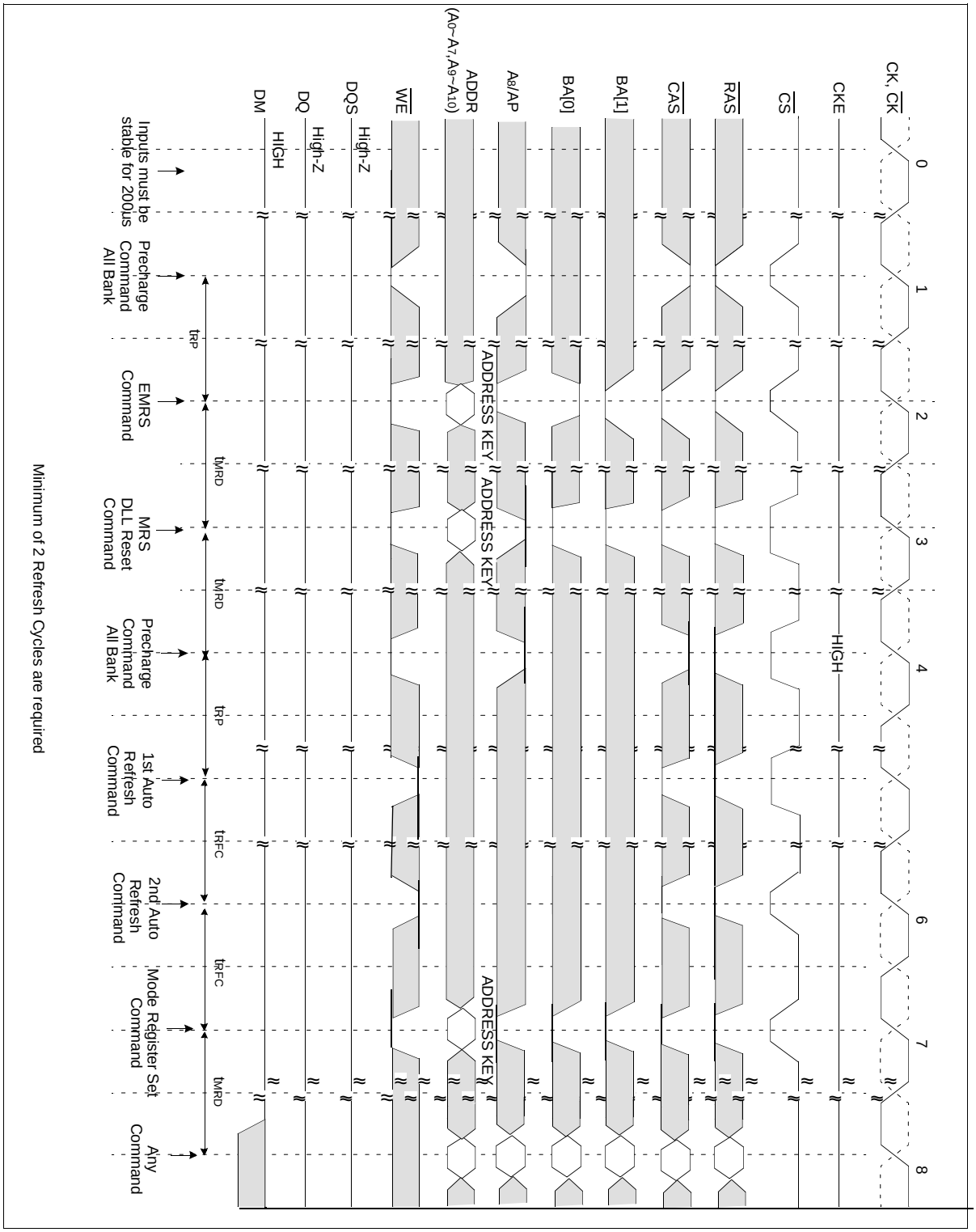
DM Function (@BL=8) only for write



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

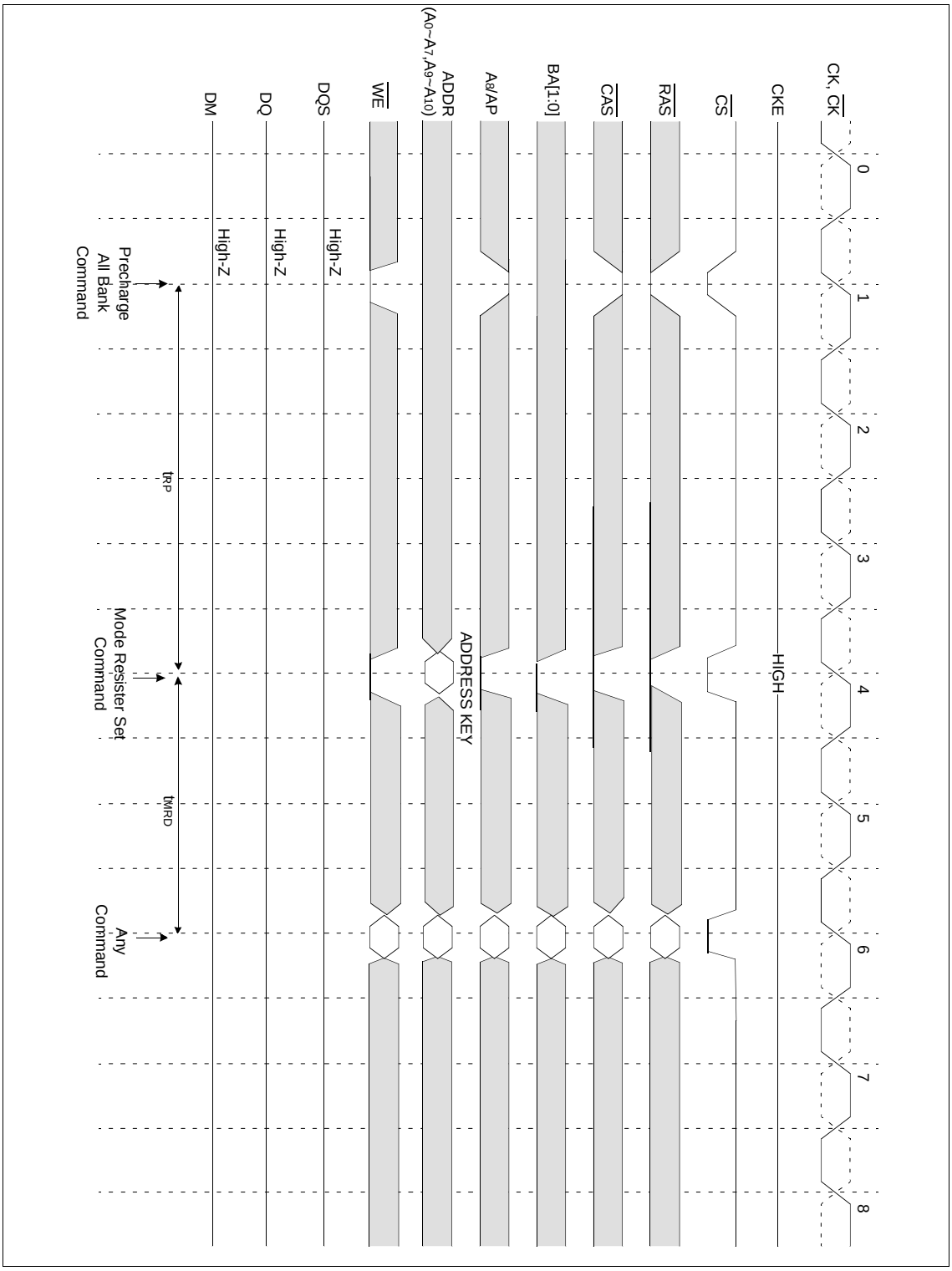
Power up Sequence & Auto Refresh(CBR)



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0

Mode Register Set



Note*

2Mx32 DDR	4Mx32 DDR
A10~A9, A7~A0	A11~A9, A7~A0