K4E661612E,K4E641612E

CMOS DRAM

4M x 16bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 4,194,304 x 16 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 4Mx16 EDO Mode DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- **Part Identification**
  - K4E661612E-TI/P(3.3V, 8K Ref.)
  - K4E641612E-TI/P(3.3V, 4K Ref.)

- **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	324	468
-50	288	432
-60	252	396

- **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
K4E661612E*	8K	64ms	128ms
K4E641612E	4K		

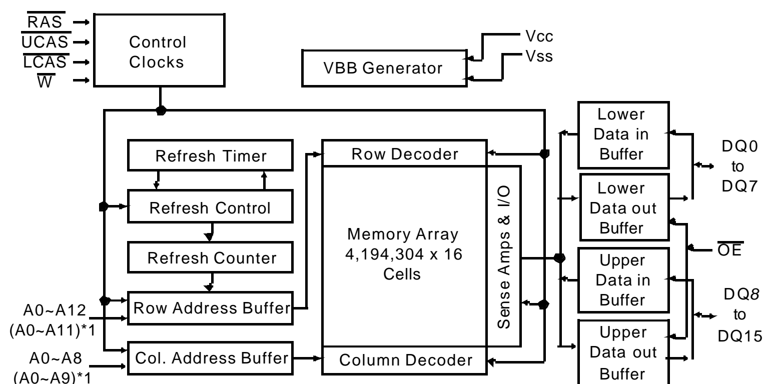
* Access mode & RAS only refresh mode
: 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)
CAS-before-RAS & Hidden refresh mode
: 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

- **Performance Range**

Speed	tRAC	tCAC	tRC	tHPC
-45	45ns	12ns	74ns	17ns
-50	50ns	13ns	84ns	20ns
-60	60ns	15ns	104ns	25ns

- Extended Data Out Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- Fast parallel test mode capability
- Self-refresh capability (L-ver only)
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic TSOP(II) packages
- +3.3V±0.3V power supply
- Industrial Temperature operating (-40~85°C)

FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

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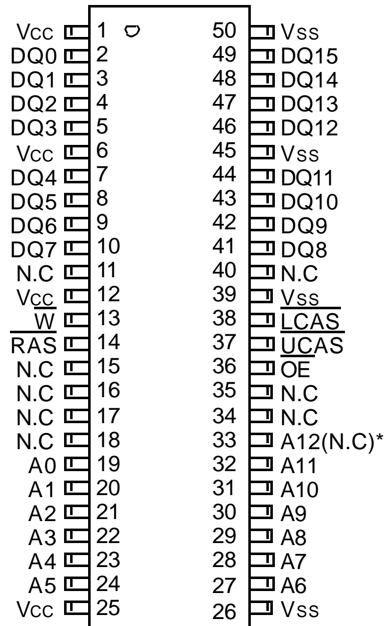
PIN CONFIGURATION (Top Views)



(400mil TSOP(II))

*(N.C) : N.C for 4K Refresh Product

Pin Name	Pin function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 15	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+3.3V)
N.C	No Connection

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on Vcc supply relative to V ss	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS} Address	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA= -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns which is measured at V_{CC}
*2 : -1.3 at pulse width≤15ns which is measured at V ss

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V_{OUT}≤V_{CC})	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

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DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4E661612E	K4E641612E	
I_{CC1}	Don't care	-45 -50 -60	90 80 70	130 120 110	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-45 -50 -60	90 80 70	130 120 110	mA mA mA
I_{CC4}	Don't care	-45 -50 -60	100 90 80	100 90 80	mA mA mA
I_{CC5}	Normal L	Don't care	0.5 200	0.5 200	mA uA
I_{CC6}	Don't care	-45 -50 -60	130 120 110	130 120 110	mA mA mA
I_{CC7}	L	Don't care	350	350	uA
I_{CCS}	L	Don't care	350	350	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{UCAS}$, $\overline{LCAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{UCAS}$=$\overline{LCAS}$=V_{IH}, $\overline{RAS}$, Address cycling @t_{RC}=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{UCAS}$ or $\overline{LCAS}$, Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{UCAS}$ or $\overline{LCAS}$ cycling @t_{RC}=min)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{UCAS}$, $\overline{LCAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
$\overline{W}$, $\overline{OE}$=V_{IH}, Address=Don't care, DQ=Open, T_{RC}=31.25us

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11)=V_{CC}-0.2V or 0.2V, DQ0 ~ DQ15=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

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CAPACITANCE (T_A=25°C, V_{CC}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	C_{IN1}	-	5	pF
Input capacitance [RAS, UCAS, LCAS, W, OE]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ15]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (-40°C≤T_A≤85°C, See note 2)

Test condition : V_{CC}=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	74		84		104		ns	
Read-modify-write cycle time	t_{RWC}	101		113		138		ns	
Access time from RAS	t_{RAC}		45		50		60	ns	3,4,10
Access time from CAS	t_{CAC}		12		13		15	ns	3,4,5
Access time from column address	t_{AA}		23		25		30	ns	3,10
CAS to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay from CAS	t_{CEZ}	3	13	3	13	3	13	ns	6,20
OE to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	2
RAS precharge time	t_{RP}	25		30		40		ns	
RAS pulse width	t_{RAS}	45	10K	50	10K	60	10K	ns	
RAS hold time	t_{RSH}	8		8		10		ns	
CAS hold time	t_{CSH}	35		38		40		ns	
CAS pulse width	t_{CAS}	7	5K	8	10K	10	10K	ns	
RAS to CAS delay time	t_{RCD}	11	33	11	37	14	45	ns	4
RAS to column address delay time	t_{RAD}	9	22	9	25	12	30	ns	10
CAS to RAS precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	7		7		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	13
Column address hold time	t_{CAH}	7		7		10		ns	13
Column address to RAS lead time	t_{RAL}	23		25		30		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to CAS	t_{RCH}	0		0		0		ns	8
Read command hold time referenced to RAS	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	7		7		10		ns	
Write command pulse width	t_{WP}	6		7		10		ns	
Write command to RAS lead time	t_{RWL}	8		8		10		ns	
Write command to CAS lead time	t_{CWL}	7		7		10		ns	16
Data set-up time	t_{DS}	0		0		0		ns	9,19

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AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Data hold time	t_{DH}	7		7		10		ns	9,19
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (L-ver)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
CAS to W delay time	t_{CWD}	24		27		32		ns	7,15
RAS to W delay time	t_{RWD}	57		64		77		ns	7
Column address to W delay time	t_{AWD}	35		39		47		ns	7
CAS set-up time (CAS -before-RAS refresh)	t_{CSR}	5		5		5		ns	17
CAS hold time (CAS -before-RAS refresh)	t_{CHR}	10		10		10		ns	18
RAS to CAS precharge time	t_{RPC}	5		5		5		ns	
Access time from CAS precharge	t_{CPA}		24		28		35	ns	3
Hyper Page cycle time	t_{HPC}	17		20		25		ns	21
Hyper Page read-modify-write cycle time	t_{HPRWC}	47		47		56		ns	21
CAS precharge time (Hyper page cycle)	t_{CP}	6.5		7		10		ns	14
RAS pulse width (Hyper page cycle)	t_{RASP}	45	200K	50	200K	60	200K	ns	
RAS hold time from CAS precharge	t_{RHCP}	24		30		35		ns	
OE access time	t_{OEA}		12		13		15	ns	3
OE to data delay	t_{OED}	8		10		13		ns	
CAS precharge to W delay time	t_{CPWD}	36		41		52		ns	
Output buffer turn off delay time from OE	t_{OEZ}	3	11	3	13	3	13	ns	6
OE command hold time	t_{OEH}	5		5		5		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	11
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	11
W to RAS precharge time (C-B-R refresh)	t_{WRP}	10		10		10		ns	
W to RAS hold time (C-B-R refresh)	t_{WRH}	10		10		10		ns	
Output data hold time	t_{DOH}	4		5		5		ns	
Output buffer turn off delay from RAS	t_{REZ}	3	13	3	13	3	13	ns	6,20
Output buffer turn off delay from W	t_{WEZ}	3	13	3	13	3	13	ns	6
W to data delay	t_{WED}	8		15		15		ns	
OE to CAS hold time	t_{OCH}	5		5		5		ns	
CAS hold time to OE	t_{CHO}	5		5		5		ns	
OE precharge time	t_{OEP}	5		5		5		ns	
W pulse width (Hyper Page Cycle)	t_{WPE}	5		5		5		ns	
RAS pulse width (C-B-R self refresh)	t_{RASS}	100		100		100		us	22,23,24
RAS precharge time (C-B-R self refresh)	t_{RPS}	74		90		110		ns	22,23,24
CAS hold time (C-B-R self refresh)	t_{CHS}	-50		-50		-50		ns	22,23,24

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TEST MODE CYCLE

(Note 11)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	79		89		109		ns	
Read-modify-write cycle time	t_{RWC}	110		121		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		55		65	ns	3,4,10,12
Access time from $\overline{CAS}$	t_{CAC}		17		18		20	ns	3,4,5,12
Access time from column address	t_{AA}		28		30		35	ns	3,10,12
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	55	10K	65	10K	ns	
$\overline{CAS}$ pulse width	t_{CAS}	12	10K	13	10K	15	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		18		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	39		43		50		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	28		30		35		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	29		35		39		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	62		72		84		ns	7
Column Address to $\overline{W}$ delay time	t_{AWD}	40		47		54		ns	7
Hyper Page cycle time	t_{HPC}	22		25		30		ns	21
Hyper Page read-modify-write cycle time	t_{HPRWC}	52		53		61		ns	21
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	55	200K	65	200K	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		29		33		40	ns	3
$\overline{OE}$ access time	t_{OEA}		17		18		20	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		18		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	13		18		20		ns	

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NOTES

1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. This parameters are referenced to the CAS leading edge in early write cycles and to the W falling edge in OE controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. These specifiecations are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. t_{ASC}, t_{CAH} are referenced to the earlier CAS falling edge.
14. t_{CP} is specified from the last CAS rising edge in the previous cycle to the first CAS falling edge in the next cycle.
15. t_{CWD} is referenced to the later CAS falling edge at word read-modify-write cycle.

K4E64(6)1612E Truth Table

RAS	LCAS	UCAS	W	OE	DQ0 - DQ7	DQ8-DQ15	STATE
H	X	X	X	X	Hi-Z	Hi-Z	Standby
L	H	H	X	X	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	-

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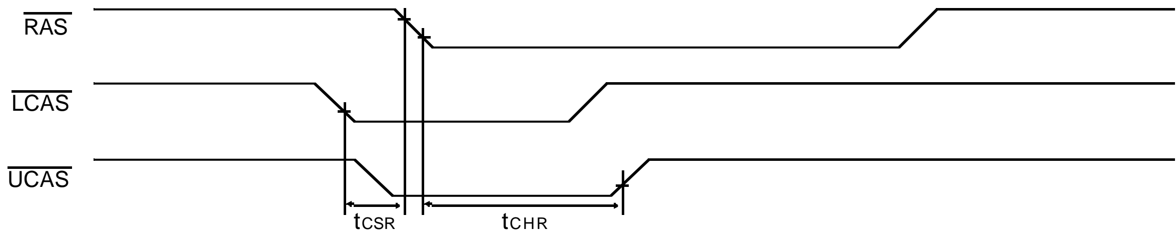
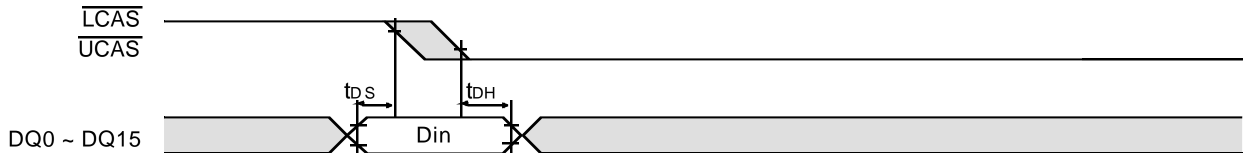
16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling before $\overline{RAS}$ transition low.
18. t_{CHR} is referenced to the later $\overline{CAS}$ rising high after $\overline{RAS}$ transition low.



19. t_{DS} is specified for the earlier $\overline{CAS}$ falling edge and t_{DH} is specified by the later $\overline{CAS}$ falling edge in early write cycle.



20. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going.
21. $t_{ASC} \geq 6$ns, Assume t_T=2.0ns, if $t_{ASC} \leq 6$ns, then t_{HPC}(min) and t_{CAS}(min) must be increased by the value of "6ns-t_{ASC}".
22. If $t_{RASS} \geq 100$us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.
23. For $\overline{RAS}$-only-Refresh and Burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles(4K/8K) of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
24. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval, CBR refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

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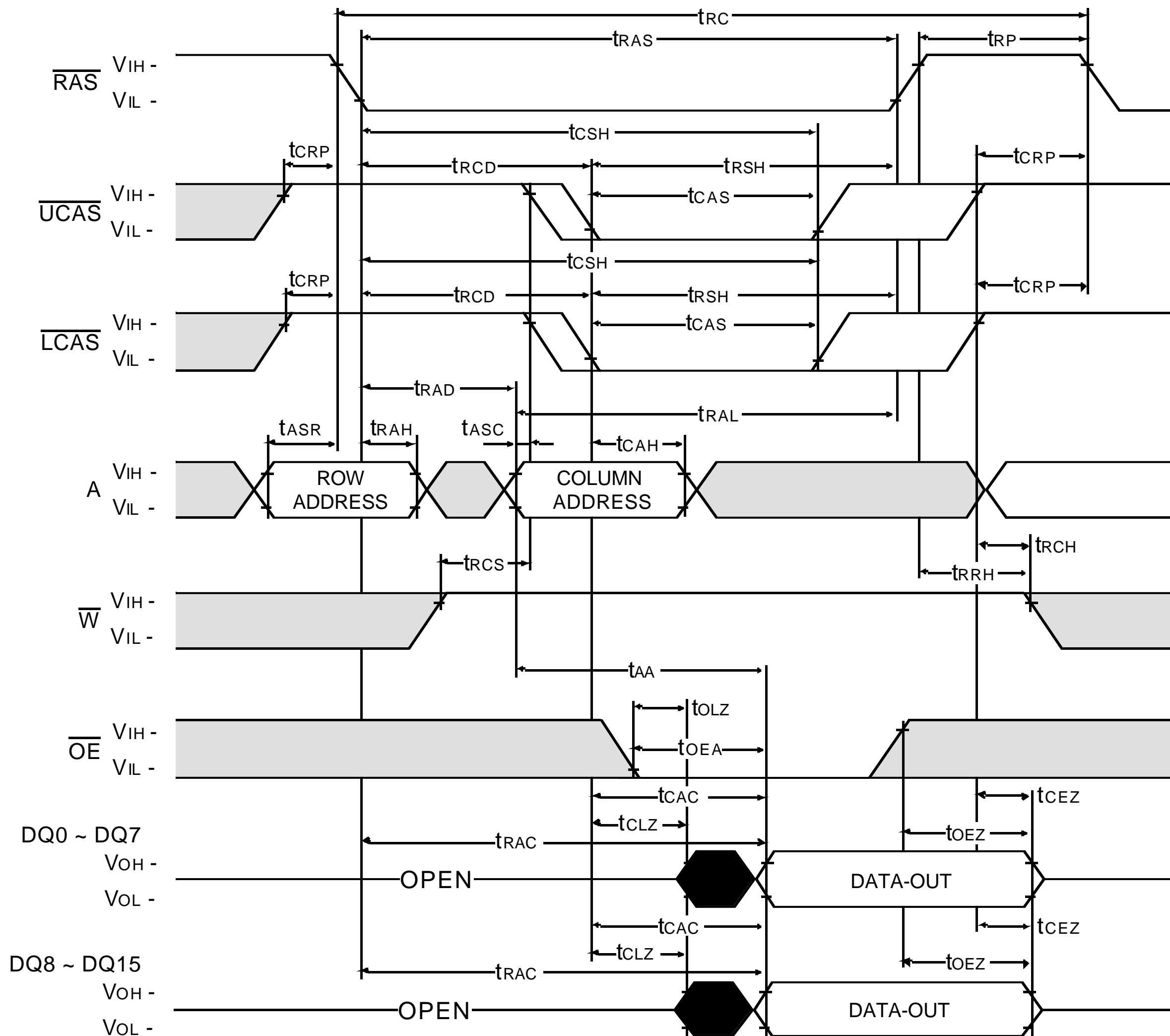
WORD READ CYCLE



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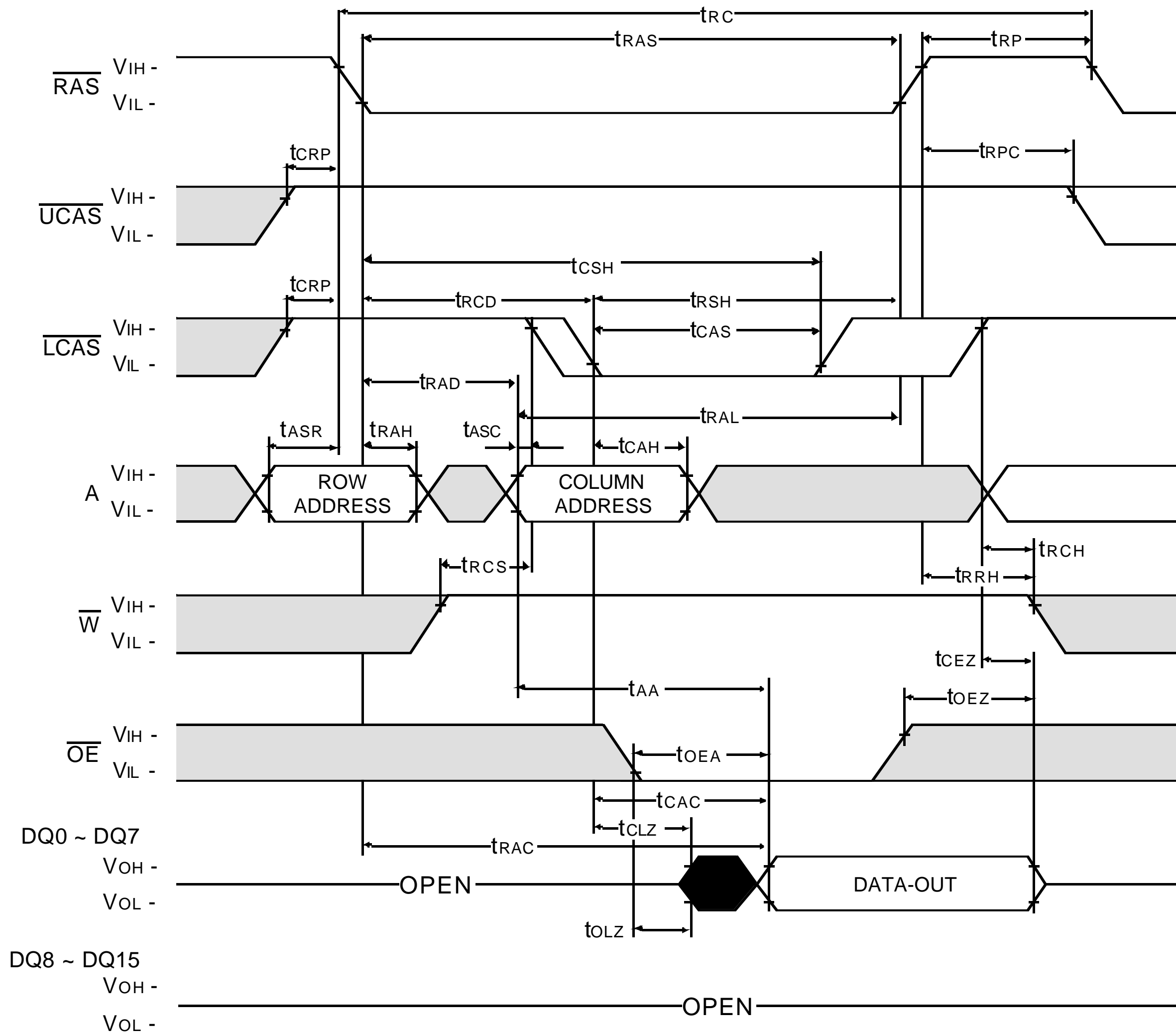
LOWER BYTE READ CYCLE

NOTE : D IN = OPEN



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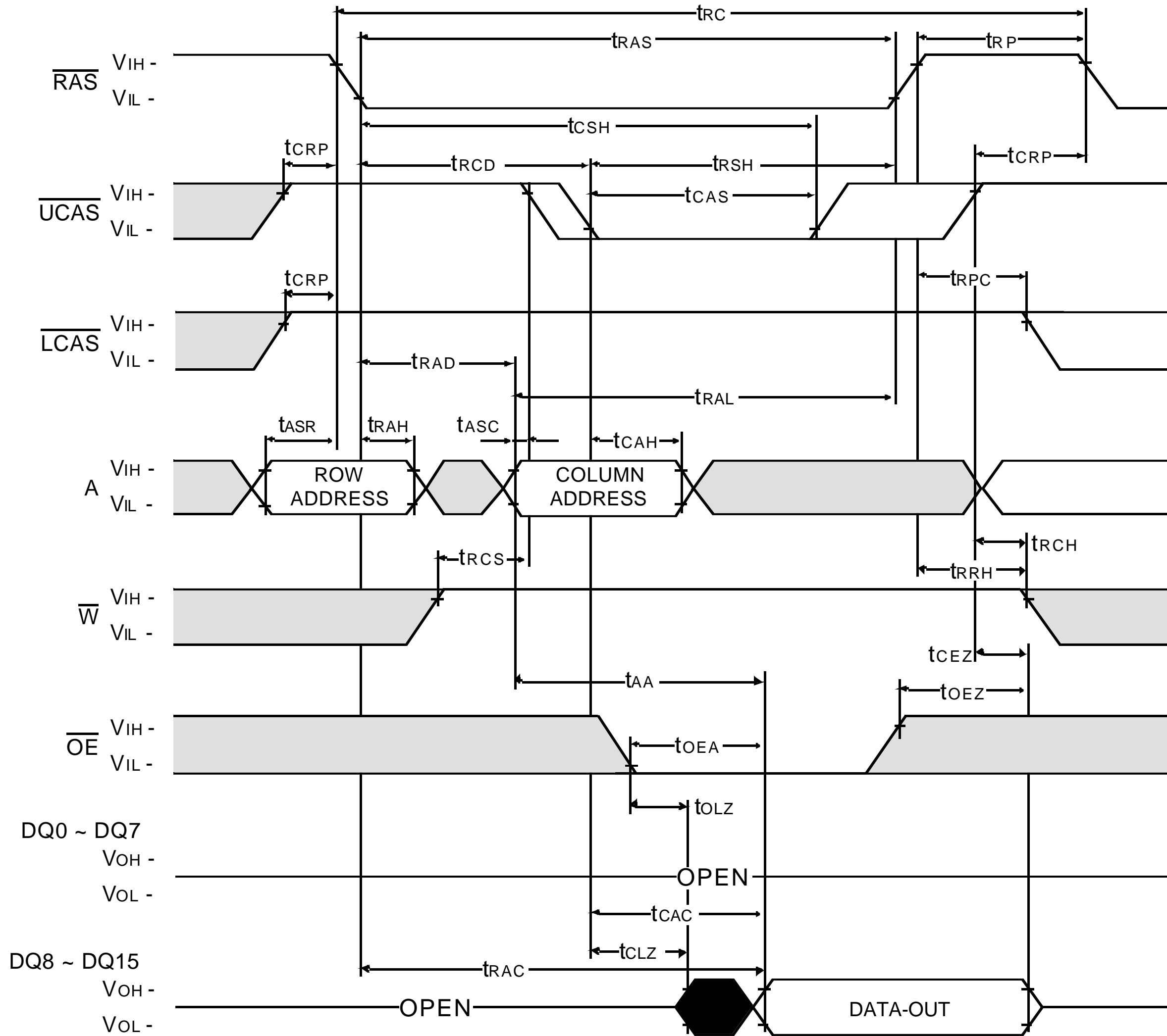
UPPER BYTE READ CYCLE

NOTE : D IN = OPEN



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WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

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LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

Don't care

Undefined

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UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

tRC
tRAS
tRP
RAS VIH - VIL -
tCSH
tCRP
tRCD
tRSH
tCAS
tCRP
UCAS VIH - VIL -
tCRP
LCAS VIH - VIL -
tRAD
tRAL
tASR tRAH tASC tCAH
A VIH - VIL -
ROW ADDRESS
COLUMN ADDRESS
tWCS
tWCH
tWP
W VIH - VIL -
OE VIH - VIL -
DQ0 ~ DQ7 VIH - VIL -
tDS
tDH
DQ8 ~ DQ15 VIH - VIL -
DATA-IN

Don’t care

Undefined

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WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT = OPEN

tRC
tRAS
tRP
RAS VIH - VIL -
tCSH
tCRP
tRCD
tRSH
tCAS
UCAS VIH - VIL -
tCSH
tCRP
tRCD
tRSH
tCAS
LCAS VIH - VIL -
tRAD
tRAL
tASR tRAH tASC tCAH
A VIH - VIL -
ROW ADDRESS
COLUMN ADDRESS
tCWL
tRWL
tWP
W VIH - VIL -
OE VIH - VIL -
tOED
tOEH
tDS tDH
DQ0 ~ DQ7 VIH - VIL -
DATA-IN
tDS tDH
DQ8 ~ DQ15 VIH - VIL -
DATA-IN

Don′t care

Undefined

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LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

Don't care

Undefined

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UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

NOTE : DOUT = OPEN

Don't care

Undefined

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WORD READD - MODIFY - WRITE CYCLE

tRWC
tRAS
tRP

RAS VIH -
VIL -

tCRP
tRCD
tRSH
tCAS

UCAS VIH -
VIL -

tCRP
tRCD
tRSH
tCAS

LCAS VIH -
VIL -

tRAD
tCSH

tASR tRAH tASC tCAH

A VIH -
VIL -

ROW ADDR.
COLUMN ADDRESS

tAWD
tRWL
tCWD
tCWL
tWP

W VIH -
VIL -

tRWD
tOEA

OE VIH -
VIL -

tOLZ
tCLZ
tCAC
tAA
tRAC
tOED
tOEZ
tDS
tDH

DQ0 ~ DQ7
VI/OH -
VI/OL -

VALID DATA-OUT
VALID DATA-IN

tOLZ
tCLZ
tCAC
tAA
tRAC
tOED
tOEZ
tDS
tDH

DQ8 ~ DQ15
VI/OH -
VI/OL -

VALID DATA-OUT
VALID DATA-IN

Don′t care
Undefined

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LOWER-BYTE READ - MODIFY - WRITE CYCLE

Don′t care

Undefined

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UPPER-BYTE READ - MODIFY - WRITE CYCLE

tRWC
tRAS
tRP
RAS VIH - VIL -
tCRP
tRCD
tRSH
tCAS
UCAS VIH - VIL -
tCRP
tRPC
LCAS VIH - VIL -
tRAD
tCSH
tASR tRAH tASC tCAH
A VIH - VIL -
ROW ADDR
COLUMN ADDRESS
tAWD
tRWL
tCWD
tCWL
tWP
W VIH - VIL -
tRWD
tOEA
OE VIH - VIL -
DQ0 ~ DQ7
VOH -
VOL -
OPEN
tOLZ
tCLZ
tCAC
tAA
tRAC
tOED
tOEZ
tDS
tDH
DQ8 ~ DQ15
VI/OH -
VI/OL -
VALID DATA-OUT
VALID DATA-IN

Don′t care
Undefined

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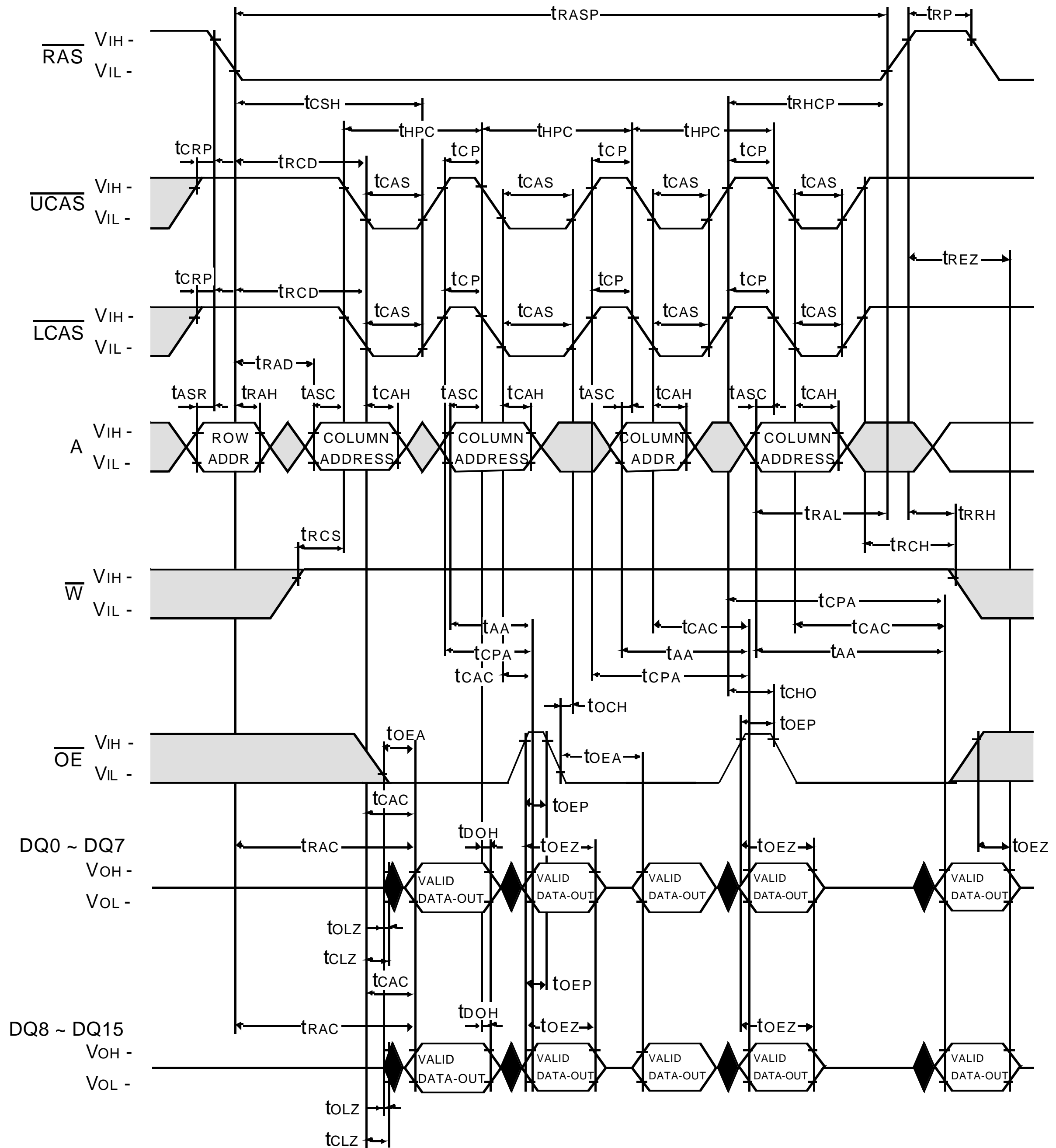
HYPER PAGE MODE WORD READ CYCLE



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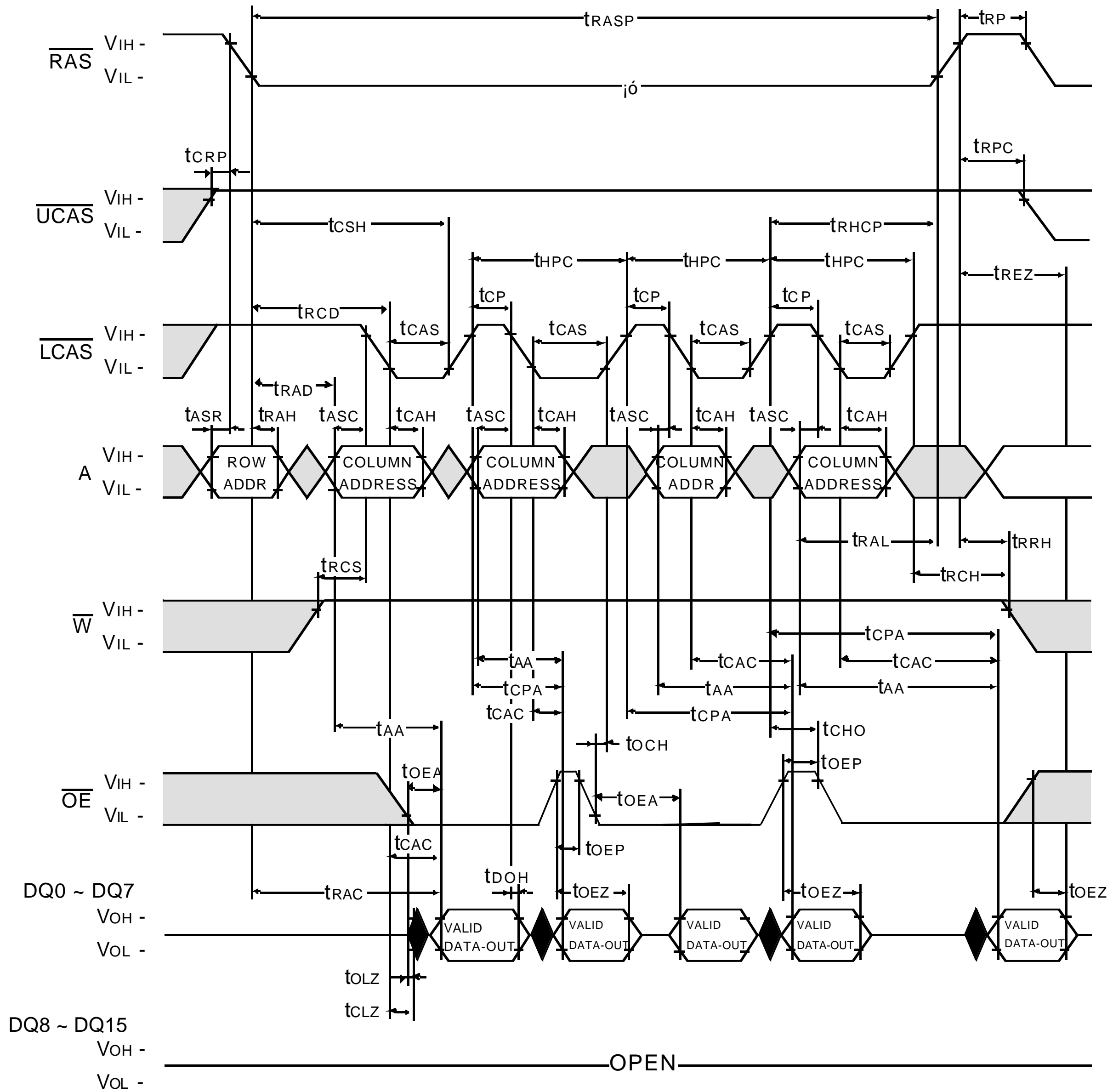
HYPER PAGE MODE LOWER BYTE READ CYCLE



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HYPER PAGE MODE UPPER BYTE READ CYCLE

Don't care

Undefined

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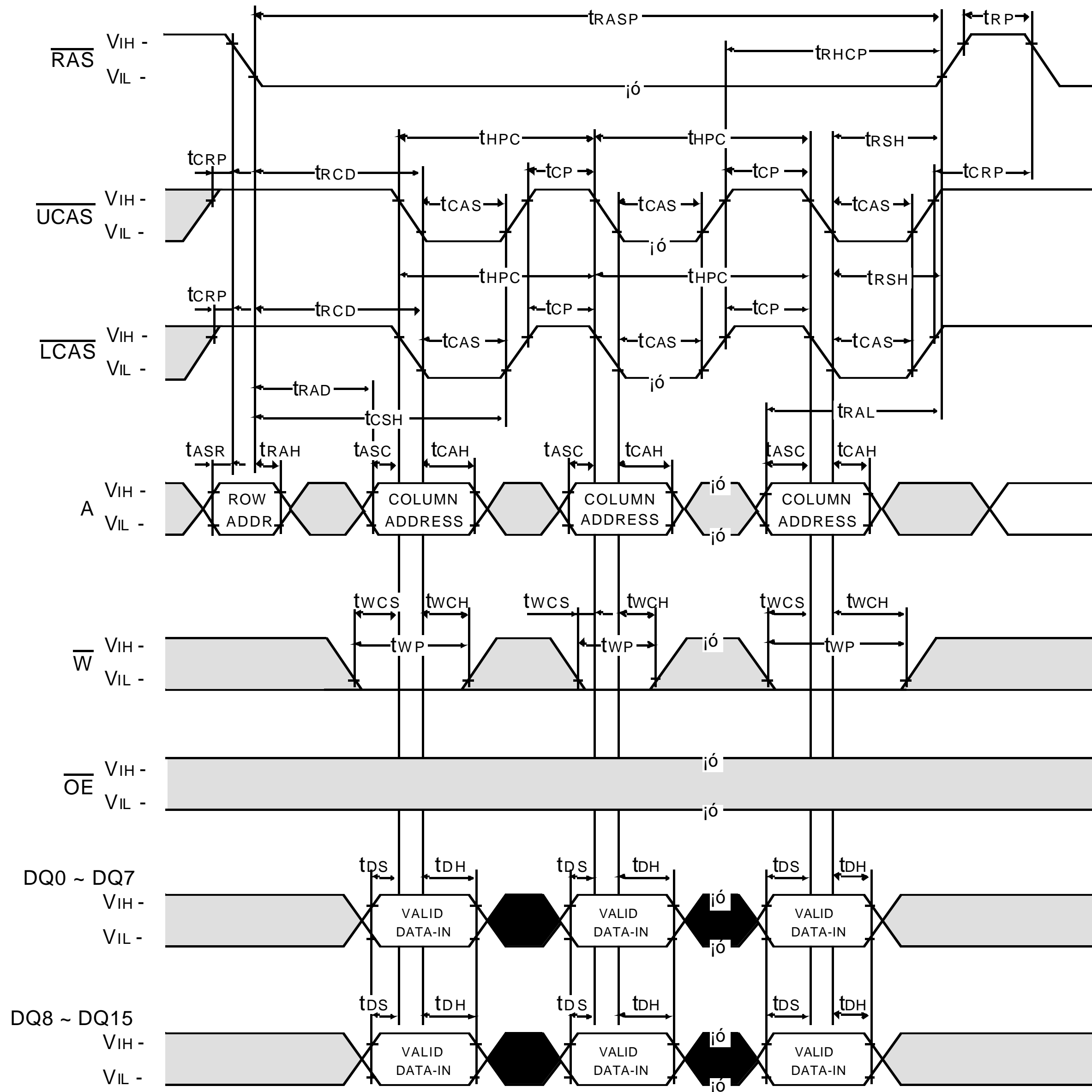
HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



Don't care

Undefined

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HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

Don't care

Undefined

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HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

RAS VIH - VIL - tRASP tRP tRHCP
UCAS VIH - VIL - tCRP tRCD tHPC tHPC tRSH tCAS tCP tCAS tCP tCAS tRPC
LCAS VIH - VIL - tCRP
tRAD tCSH tRAL
A VIH - VIL - tASR tRAH tASC tCAH tASC tCAH tASC tCAH ROW ADDR COLUMN ADDRESS COLUMN ADDRESS COLUMN ADDRESS
W VIH - VIL - tWCS tWCH tWP tWCS tWCH tWP tWCS tWCH tWP
OE VIH - VIL -
DQ0 ~ DQ7 VIH - VIL -
DQ8 ~ DQ15 VIH - VIL - tDS tDH tDS tDH tDS tDH VALID DATA-IN VALID DATA-IN VALID DATA-IN

Don′t care
Undefined

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HYPER PAGE MODE WORD READ - MODIFY - WRITE CYCLE

Don't care

Undefined

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HYPER PAGE MODE LOWER BYTE READ - MODIFY - WRITE CYCLE

tRASP
tRP
tCSH
tHPRWC
RAS VIH - VIL -
tCRP
tRPC
UCAS VIH - VIL -
tCRP
tRCD
tCP
tRSH
tCRP
LCAS VIH - VIL -
tCAS
tCAS
tRAD
tRAH
tCAH
tRAL
tASR
tASC
tASC
tCAH
A VIH - VIL -
ROW ADDR
COL. ADDR
COL. ADDR
tRCS
tCWL
tRCS
tRWL
tCWL
tWP
tWP
W VIH - VIL -
tCWD
tAWD
tRWD
tCWD
tAWD
tCPWD
OE VIH - VIL -
tOEA
tOEA
tOED
tOED
tCAC
tCAC
tAA
tAA
tDH
tDH
tOEZ
tDS
tOEZ
tDS
DQ0 ~ DQ7
tRAC
VI/OH -
VI/OL -
tCLZ
tCLZ
tOLZ
tOLZ
VALID DATA-OUT
VALID DATA-IN
VALID DATA-OUT
VALID DATA-IN
DQ8 ~ DQ15
VI/OH -
VI/OL -
OPEN

Don't care

Undefined

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HYPER PAGE MODE UPPER BYTE READ - MODIFY - WRITE CYCLE

RAS VIH - VIL -
UCAS VIH - VIL -
LCAS VIH - VIL -
A VIH - VIL -
W VIH - VIL -
OE VIH - VIL -
DQ0 ~ DQ7 VI/OH - VI/OL -
DQ8 ~ DQ15 VI/OH - VI/OL -

tRASP tRP tCSH tHPRWC tCRP tRCD tCP tRSH tCAS tRPC tRAD tRAH tCAH tASR tASC tRAL ROW ADDR COL. ADDR tRCS tCWL tRWL tWP tCWD tAWD tRWD tCPWD tOEA OPEN tOLZ tOED tCAC tDH tAA tOEZ tDS tRAC tCLZ VALID DATA-OUT VALID DATA-IN

Don't care

Undefined

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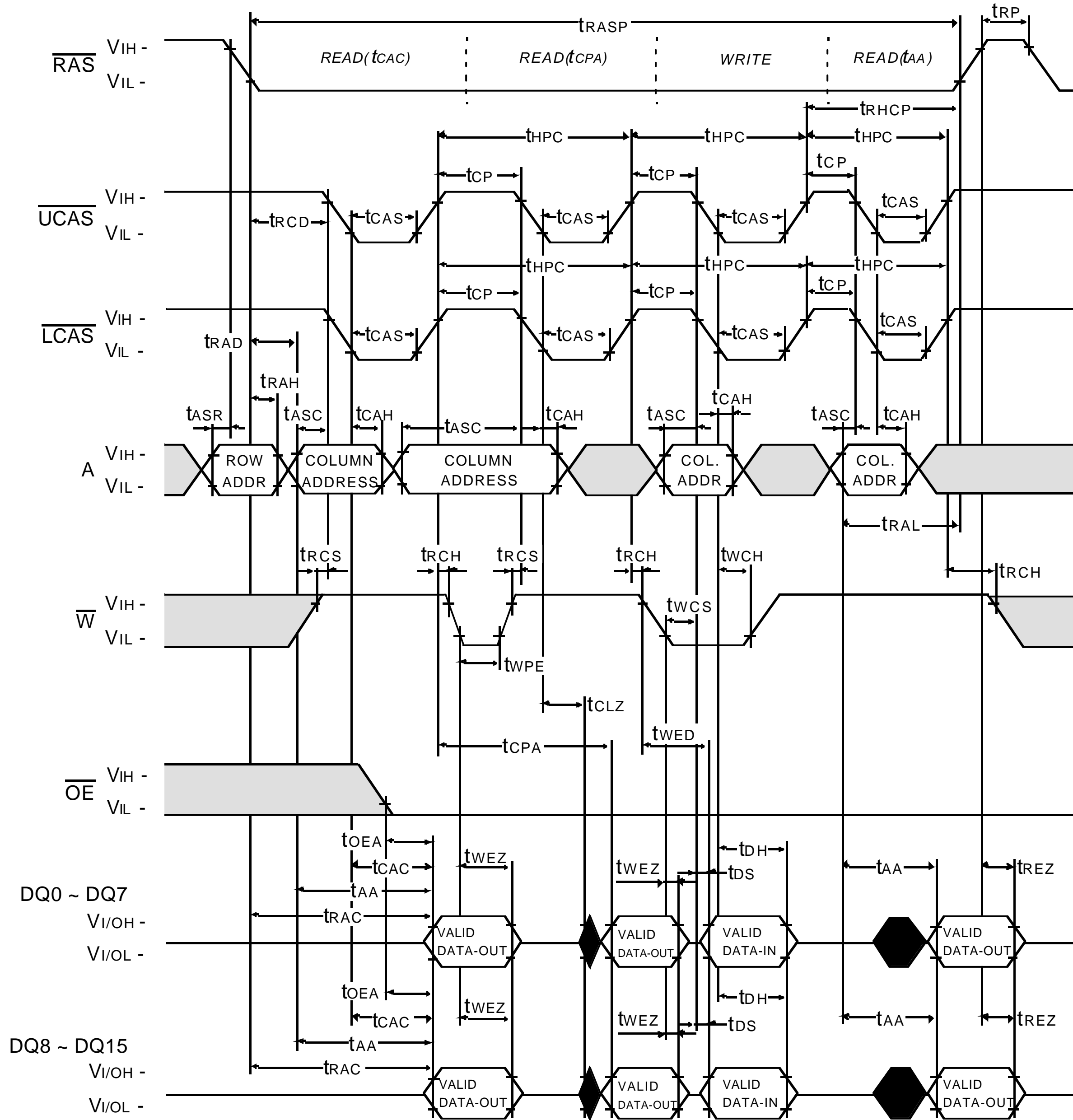
HYPER PAGE READ AND WRITE MIXED CYCLE



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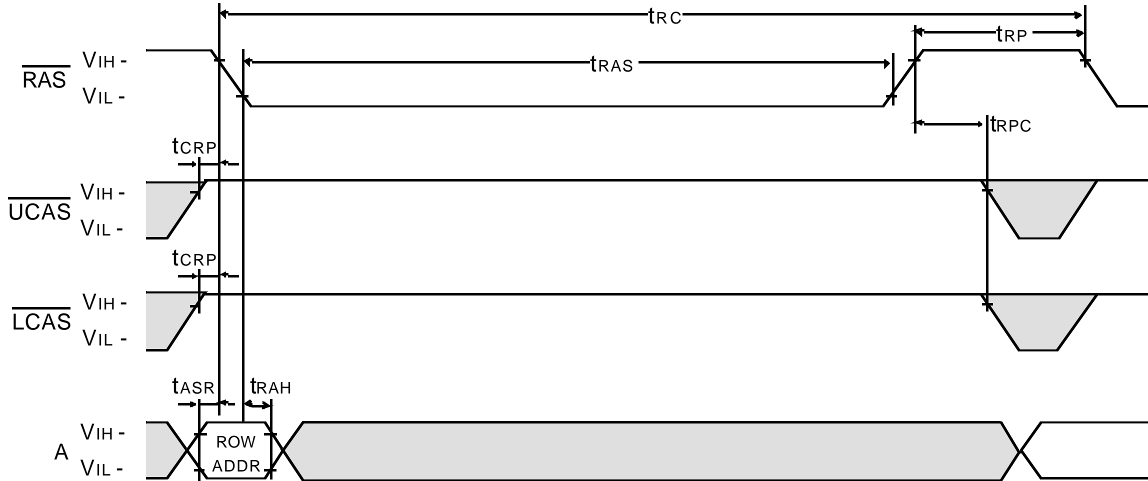
RAS - ONLY REFRESH CYCLE

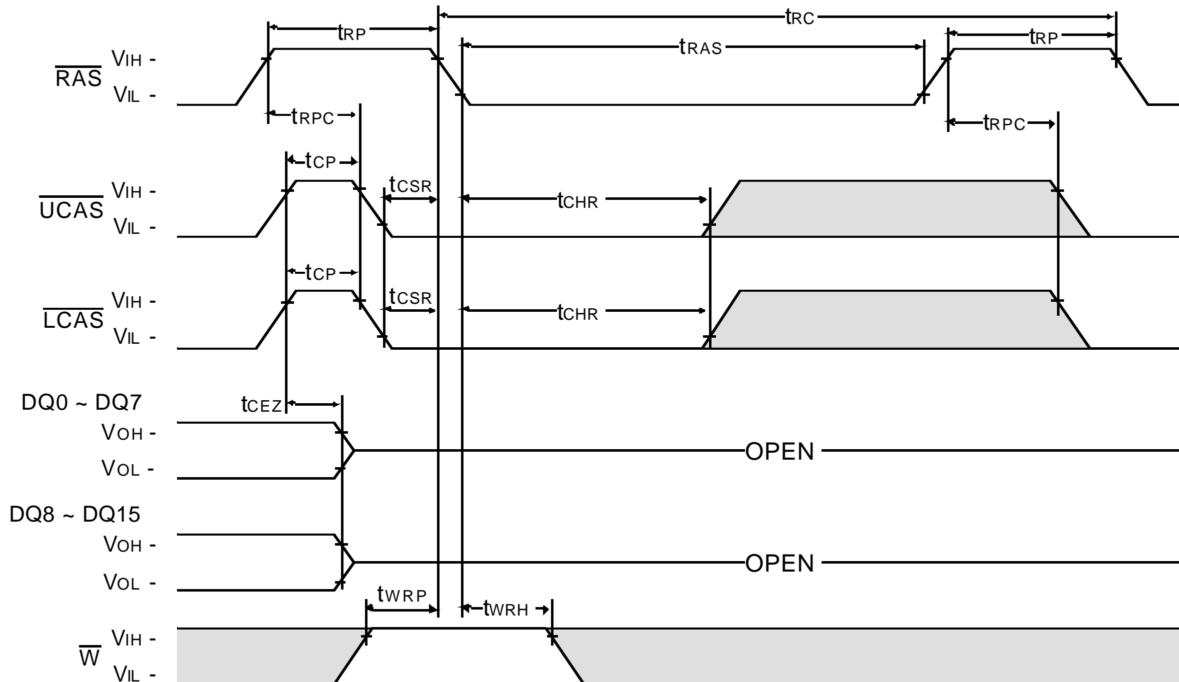
NOTE : W, OE , DIN = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

NOTE : OE, A = Don't care



Don't care

Undefined

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HIDDEN REFRESH CYCLE (READ)

RAS VIH - VIL -
UCAS VIH - VIL -
LCAS VIH - VIL -
A VIH - VIL -
W VIH - VIL -
OE VIH - VIL -
DQ0 ~ DQ7 VOH - VOL -
DQ8 ~ DQ15 VOH - VOL -

tRC tRP tRAS tCRP tRCD tRSH tCHR tRAD tASR tRAH tASC tCAH tWRH tRCS tRAL tAA tOEA tCEZ tREZ tCAC tCLZ tWEZ tOLZ tRAC tOEZ

ROW ADDRESS
COLUMN ADDRESS
OPEN
DATA-OUT

Don't care
Undefined

* In Hidden refresh cycle of 64Mb A-die & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

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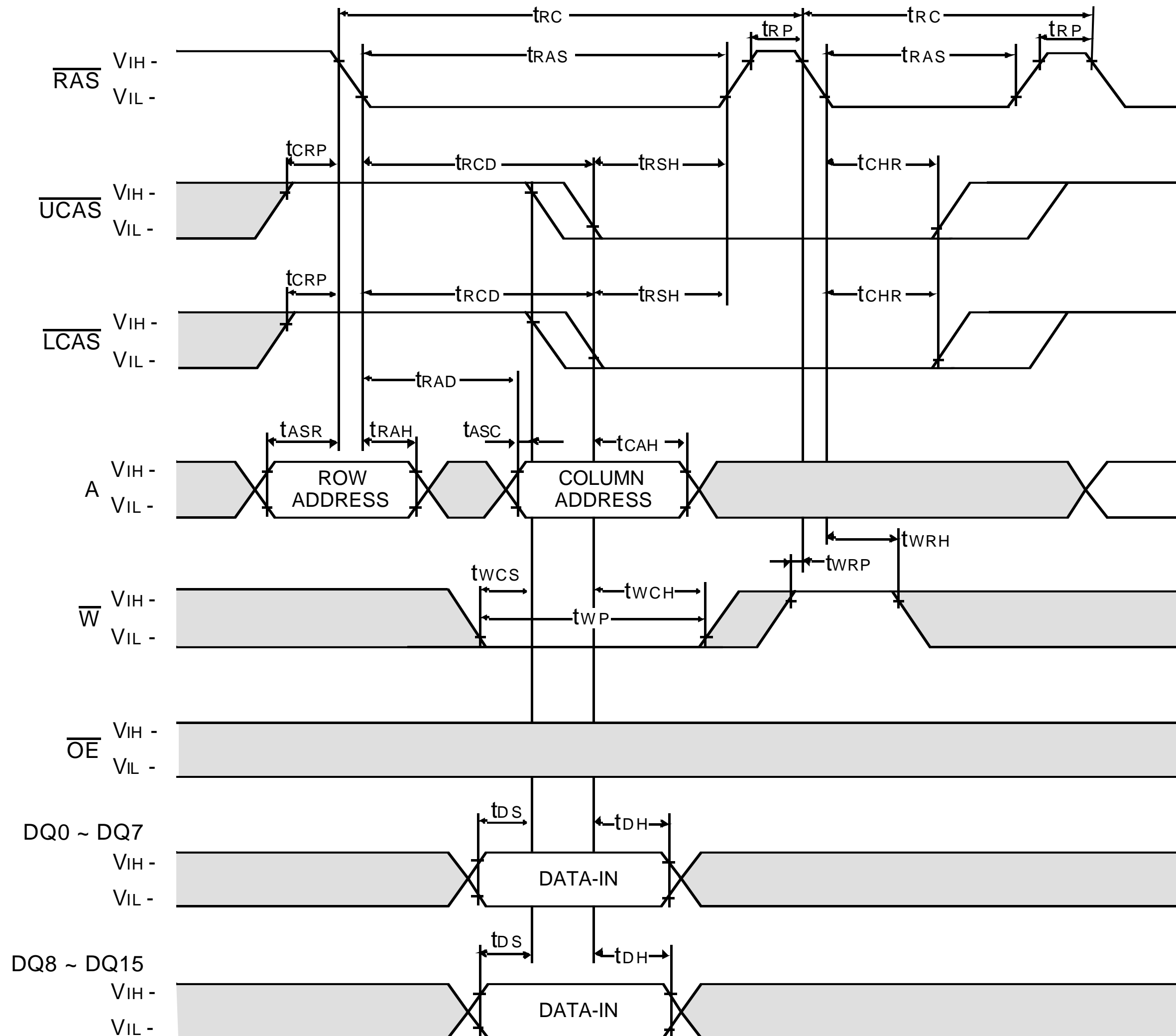
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



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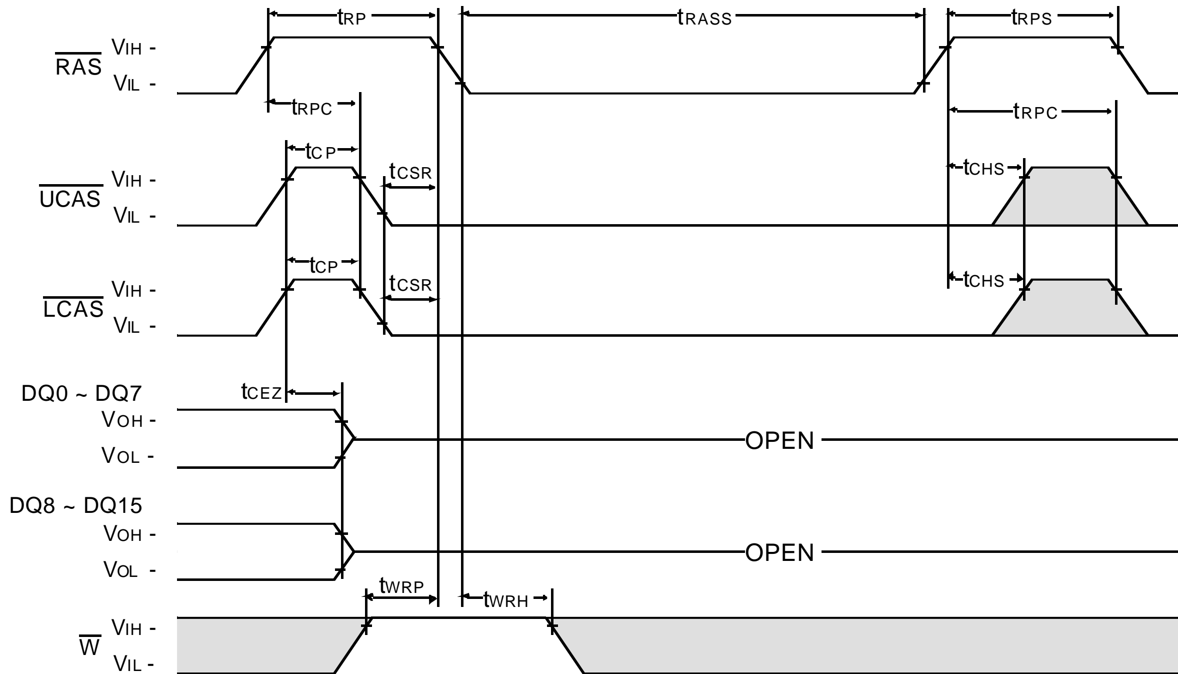
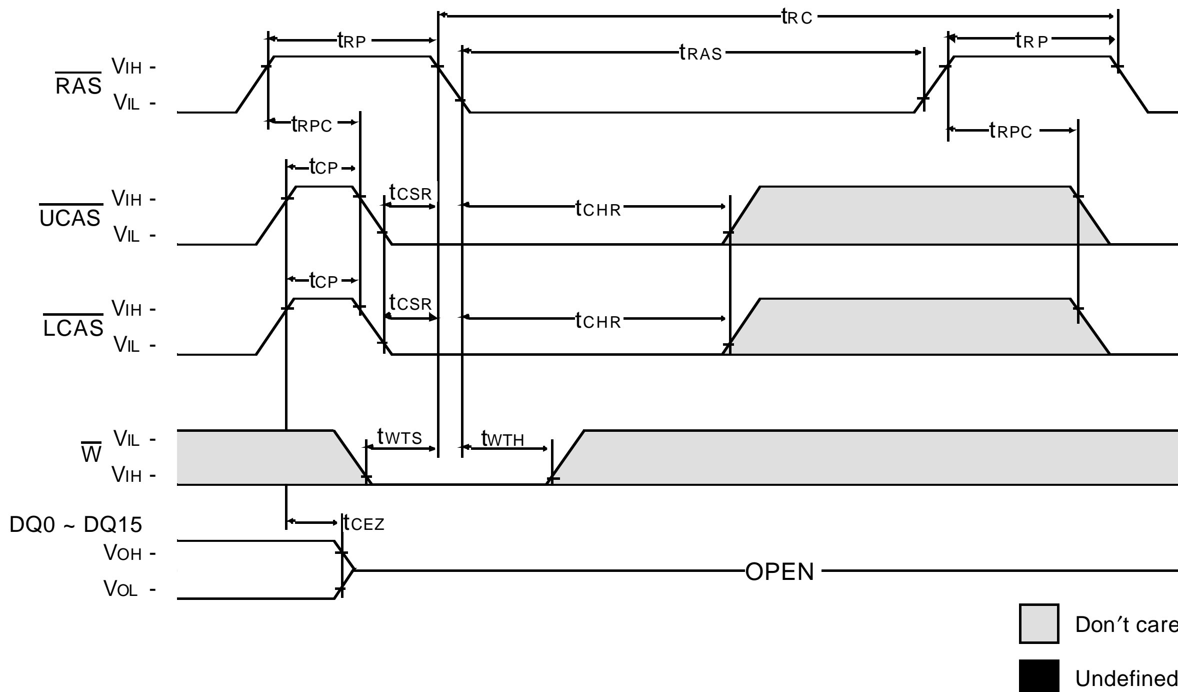
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : OE , A = Don′t care



TEST MODE IN CYCLE

NOTE : OE , A = Don′t care



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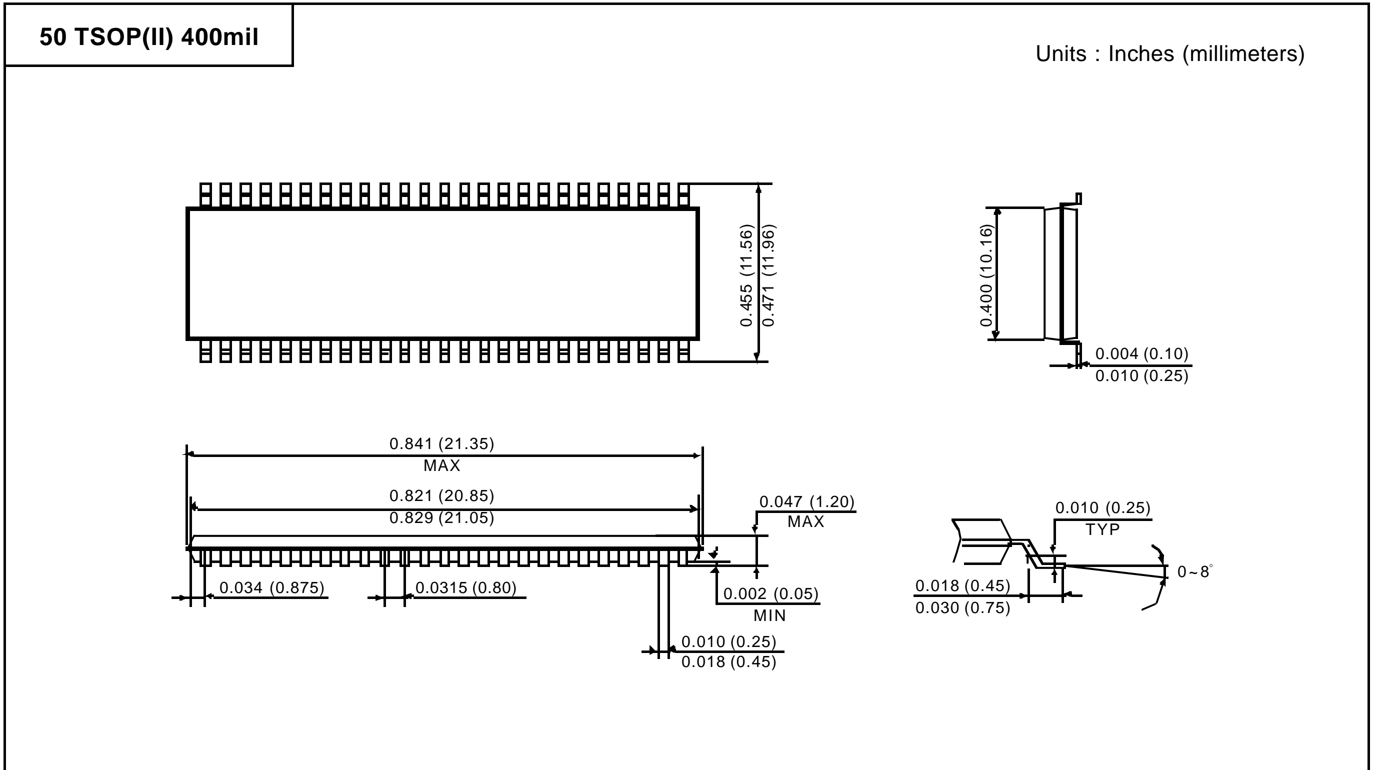
PACKAGE DIMENSION

50 TSOP(II) 400mil

Units : Inches (millimeters)



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