1Gbit GDDR3 SDRAM

136FBGA with Halogen-Free & Lead-Free

(RoHS compliant)

Revision 1.0
May 2009

Revision History

Revision	Month	Year	History
0.1	December	2008	***Target Spec***
0.5	April	2009	***Preliminary Spec*** - Removed 'Low Power Mode' from EMRS2 on page19 (A2 bit should be set '0')
1.0	May	2009	***The First Copy*** - Add thermal characteristics values on page 54 - Add IDD spec values on page 55,56

4M x 32Bit x 8 Banks Graphic Double Data Rate 3 Synchronous DRAM with Uni-directional Data Strobe

FEATURES

- 1.7V(min) ~ 1.9V(max) power supply for device operation
- 1.7V(min) ~ 1.9V(max) power supply for I/O interface
- On-Die Termination (ODT)
- Output Driver Strength adjustment by EMRS1
- Calibrated output drive
- 1.8V Pseudo Open drain compatible inputs/outputs
- Merged mode or non merged mode set by EMRS2.
- 1CS mode or 2CS mode set by EMRS1
- Fully independent 8banks are selected by $\overline{CS0}$ and $\overline{CS1}$
- Differential clock inputs (CK and $\overline{CK}$)
- Commands entered on each positive CK edge
- CAS latency : 7, 8, 9, 10, 11, 12, 13, 14, 15 (clock)
- Programmable Burst length : 4 and 8
- Programmable Write latency : 1, 2, 3, 4, 5, 6 and 7 (clock)
- Single ended READ strobe (RDQS) per byte
- Single ended WRITE strobe (WDQS) per byte
- RDQS edge-aligned with data for READs
- WDQS center-aligned with data for WRITEs
- Data Mask(DM) for masking WRITE data
- Auto & Self refresh modes
- Auto Precharge option
- 32ms, auto refresh (8K cycle)
- Halogen-free & Lead-free 136 Ball FBGA
- Maximum clock frequency up to 1.3GHz
- Maximum data rate up to 2.6Gbps/pin
- DLL for outputs
- Boundary scan function with SEN pin.
- Mirror function with MF pin

ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	VDD&VDDQ	Package
K4J10324KE-HC7A	1300MHz	2.6Gbps/pin	1.8V±0.1V	136 Ball FBGA
K4J10324KE-HC08	1200MHz	2.4Gbps/pin		
K4J10324KE-HC1A	1000MHz	2.0Gbps/pin		
K4J10324KE-HC12	800MHz	1.6Gbps/pin		
K4J10324KE-HC14	700MHz	1.4Gbps/pin		

GENERAL DESCRIPTION FOR 4M x 32Bit x 8 Bank GDDR3 SDRAM

The K4J10324KE is 1G bits of hyper synchronous data rate Dynamic RAM organized as 16 x 2,097,152 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 10.4GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

32MX32 GDDR3 SGRAM ADDRESSING

CONFIGURATION	32MX32 GDDR3 Addressing Scheme	
	1CS mode($\overline{CS0}$)	2CS mode($\overline{CS0}$ / $\overline{CS1}$)
Row address	A0~A12	A0~A11
Column address	A0~A7,A9	A0~A7,A9
Bank address	BA0~BA2	BA0~BA2
Autoprecharge	A8	A8
Refresh	8K/32ms	8K/32ms
Refresh period	3.9us	3.9us

PIN CONFIGURATION

Normal Package (Top View)

1CS mode in Non-Merged Mode

	1	2	3	4	5	6	7	8	9	10	11	12
A	VDDQ	VDD	VSS	ZQ					MF	VSS	VDD	VDDQ
B	VSSQ	DQ0	DQ1	VSSQ					VSSQ	DQ9	DQ8	VSSQ
C	VDDQ	DQ2	DQ3	VDDQ					VDDQ	DQ11	DQ10	VDDQ
D	VSSQ	WDQS0	RDQS0	VSSQ					VSSQ	RDQS1	WDQS1	VSSQ
E	VDDQ	DQ4	DM0	VDDQ					VDDQ	DM1	DQ12	VDDQ
F	VDD	DQ6	DQ5	$\overline{CAS}$					$\overline{CS0}$	DQ13	DQ14	VDD
G	VSS	VSSQ	DQ7	BA0					BA1	DQ15	VSSQ	VSS
H	VREF	A1	$\overline{RAS}$	CKE					$\overline{WE}$	BA2	A5	VREF
J	VSSA	A12	RFU	VDDQ					VDDQ	$\overline{CK}$	CK	VSSA
K	VDDA	A10	A2	A0					A4	A6	A8/AP	VDDA
L	VSS	VSSQ	DQ25	A11					A7	DQ17	VSSQ	VSS
M	VDD	DQ24	DQ27	A3					A9	DQ19	DQ16	VDD
N	VDDQ	DQ26	DM3	VDDQ					VDDQ	DM2	DQ18	VDDQ
P	VSSQ	WDQS3	RDQS3	VSSQ					VSSQ	RDQS2	WDQS2	VSSQ
R	VDDQ	DQ28	DQ29	VDDQ					VDDQ	DQ21	DQ20	VDDQ
T	VSSQ	DQ30	DQ31	VSSQ					VSSQ	DQ23	DQ22	VSSQ
V	VDDQ	VDD	VSS	SEN					RESET	VSS	VDD	VDDQ

Note :
1. This ballout is for 1CS mode in Non-merged mode. This mode is a normal functionality mode for 1Gb GDDR3
2. 1CS mode use $\overline{CS0}$ and A12 (don't care J3 pin) by EMRS1.
3. RFU is reserved for future use

PIN CONFIGURATION

Normal Package (Top View)

2CS mode in Non-Merged Mode

	1	2	3	4	5	6	7	8	9	10	11	12
A	VDDQ	VDD	VSS	ZQ					MF	VSS	VDD	VDDQ
B	VSSQ	DQ0	DQ1	VSSQ					VSSQ	DQ9	DQ8	VSSQ
C	VDDQ	DQ2	DQ3	VDDQ					VDDQ	DQ11	DQ10	VDDQ
D	VSSQ	WDQS0	RDQS0	VSSQ					VSSQ	RDQS1	WDQS1	VSSQ
E	VDDQ	DQ4	DM0	VDDQ					VDDQ	DM1	DQ12	VDDQ
F	VDD	DQ6	DQ5	$\overline{CAS}$					$\overline{CS0}$	DQ13	DQ14	VDD
G	VSS	VSSQ	DQ7	BA0					BA1	DQ15	VSSQ	VSS
H	VREF	A1	$\overline{RAS}$	CKE					$\overline{WE}$	BA2	A5	VREF
J	VSSA	RFU	$\overline{CS1}$	VDDQ					VDDQ	$\overline{CK}$	CK	VSSA
K	VDDA	A10	A2	A0					A4	A6	A8/AP	VDDA
L	VSS	VSSQ	DQ25	A11					A7	DQ17	VSSQ	VSS
M	VDD	DQ24	DQ27	A3					A9	DQ19	DQ16	VDD
N	VDDQ	DQ26	DM3	VDDQ					VDDQ	DM2	DQ18	VDDQ
P	VSSQ	WDQS3	RDQS3	VSSQ					VSSQ	RDQS2	WDQS2	VSSQ
R	VDDQ	DQ28	DQ29	VDDQ					VDDQ	DQ21	DQ20	VDDQ
T	VSSQ	DQ30	DQ31	VSSQ					VSSQ	DQ23	DQ22	VSSQ
V	VDDQ	VDD	VSS	SEN					RESET	VSS	VDD	VDDQ

Note :
1. This ballout is for 2CS mode in Non-merged mode. This mode is a special mode for 1Gb GDDR3
2. 2CS mode use both $\overline{CS0}$ and $\overline{CS1}$ (don't care J2 pin) by EMRS1.
3. RFU is reserved for future use.

PIN CONFIGURATION

Normal Package (Top View)

Merged Mode

	1	2	3	4	5	6	7	8	9	10	11	12
A	VDDQ	VDD	VSS	ZQ					MF	VSS	VDD	VDDQ
B	VSSQ	DQ0	DQ1	VSSQ					VSSQ	DQ9	DQ8	VSSQ
C	VDDQ	DQ2	DQ3	VDDQ					VDDQ	DQ11	DQ10	VDDQ
D	VSSQ	WDQS0	RDQS0	VSSQ					VSSQ	RDQS1	WDQS1	VSSQ
E	VDDQ	DQ4	DM0	VDDQ					VDDQ	DM1	DQ12	VDDQ
F	VDD	DQ6	DQ5	$\overline{CAS}$					$\overline{CS0}$	DQ13	DQ14	VDD
G	VSS	VSSQ	DQ7	BA0					BA1	DQ15	VSSQ	VSS
H	VREF	A1	$\overline{RAS}$	CKE					$\overline{WE}$	BA2	A5	VREF
J	VSSA	RFU	A12/$\overline{CS1}$	VDDQ					VDDQ	$\overline{CK}$	CK	VSSA
K	VDDA	A10	A2	A0					A4	A6	A8/AP	VDDA
L	VSS	VSSQ	DQ25	A11					A7	DQ17	VSSQ	VSS
M	VDD	DQ24	DQ27	A3					A9	DQ19	DQ16	VDD
N	VDDQ	DQ26	DM3	VDDQ					VDDQ	DM2	DQ18	VDDQ
P	VSSQ	WDQS3	RDQS3	VSSQ					VSSQ	RDQS2	WDQS2	VSSQ
R	VDDQ	DQ28	DQ29	VDDQ					VDDQ	DQ21	DQ20	VDDQ
T	VSSQ	DQ30	DQ31	VSSQ					VSSQ	DQ23	DQ22	VSSQ
V	VDDQ	VDD	VSS	SEN					RESET	VSS	VDD	VDDQ

Note :
1. This ballout is for Merged mode. A12 and $\overline{CS1}$ pins are merged in this mode.
2. Non-merged or Merged mode can be selected by EMRS2.
3. RFU is reserved for future use

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. CMD, ADD inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing). CK and $\overline{CK}$ should be maintained stable except self-refresh mode.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS0}$, $\overline{CS1}$	Input	**Chip Select:** All commands are masked when $\overline{CS0}$ and $\overline{CS1}$ are registered HIGH. $\overline{CS0}$ and $\overline{CS1}$ provides for internal bank selection which is independent 8 Banks in the DRAM with multiple banks. $\overline{CS0}$ and $\overline{CS1}$ are considered part of the command code. $\overline{CS0}$ and $\overline{CS1}$ must not activate simultaneously.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM0 ~DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of clock. Although DM pins are input only, the DM loading matches the DQ and WDQS loading.
BA0 ~ BA2	Input	**Bank Address Inputs:** BA0, BA1 and BA2 define to which bank an Active, Read, Write or Precharge command is being applied.
A0 ~ A11	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A8 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1,BA2. The address inputs also provide the op-code during Mode Register Set commands. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA7, CA9 . Column address CA8 is used for auto precharge.
DQ0 ~ DQ31	Input/ Output	**Data Input/ Output:** Bi-directional data bus.
RDQS0 ~ RDQS3	Output	**READ Data Strobe:** Output with read data. RDQS is edge-aligned with read data.
WDQS0 ~ WDQS3	Input	**WRITE Data Strobe:** Input with write data. WDQS is center-aligned to the inout data.
NC/RFU		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply
V_{SS}	Supply	Ground
V_{DDA}	Supply	DLL Power Supply
V_{SSA}	Supply	DLL Ground
V_{REF}	Supply	**Reference voltage:** 0.7*VDDQ , **2 Pins :** (H12) for Data input , (H1) for CMD and ADDRESS
MF	Input	Mirror Function for clamshell mounting of DRAMs. VDDQ CMOS input.
ZQ	Reference	Resistor connection pin for On-die termination.
RES	Input	Reset pin: RESET pin is a VDDQ CMOS input
SEN	Input	**Scan enable :** Must tie to the ground in case not in use. VDDQ CMOS input.

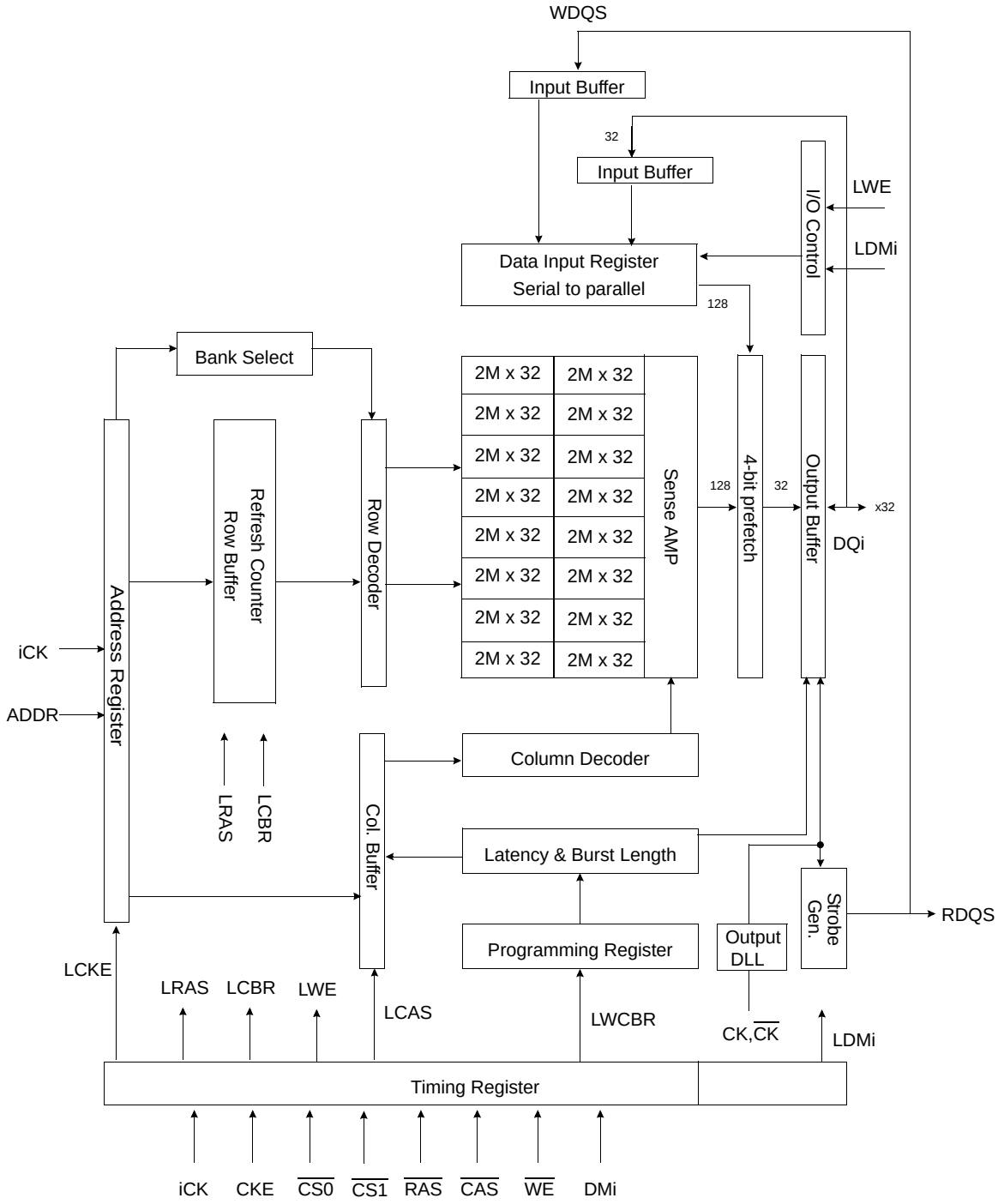
Mirror Function

The GDDR3 SDRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines which help to route devices back to back. The MF ball will affect RAS, CAS, WE, CS0 and CKE on balls H3, F4, H9, F9 and H4 respectively and A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, BA0, BA1 and BA2 on balls K4, H2, K3, M4, K9, H11, K10, L9, K11, M9, K2, L4, G4, G9 and H10 respectively and only detects a DC input. The MF ball should be tied directly to VSS or VDD depending on the desired control line orientation. When the MF ball is tied low the ball orientation is as follows, RAS - H3, CAS - F4, WE - H9, CS0 - F9, CKE - H4, A0 - K4, A1 - H2, A2 - K3, A3 - M4, A4 - K9, A5 - H11, A6 - K10, A7 - L9, A8 - K11, A9 - M9, A10 - K2, A11 - L4, BA0 - G4, BA1 - G9 and BA2 - H10. The high condition on the MF ball will change the location of the control balls as follows;RAS - H10, CAS - F9, WE - H4, CS0 - F4, CKE - H9, A0 - K9, A1 - H11, A2 - K10, A3 - M9, A4 - K4, A5 - H2, A6 - K3, A7 - L4, A8 - K2, A9 - M4, A10 - K11, A11 - L9, BA0 - G9, BA1 - G4 and BA2 - H3.

Mirror Function Signal Mapping

PIN	MF LOGIC STATE	
	HIGH	LOW
$\overline{RAS}$	H10	H3
$\overline{CAS}$	F9	F4
$\overline{WE}$	H4	H9
$\overline{CS0}$	F4	F9
CKE	H9	H4
A0	K9	K4
A1	H11	H2
A2	K10	K3
A3	M9	M4
A4	K4	K9
A5	H2	H11
A6	K3	K10
A7	L4	L9
A8	K2	K11
A9	M4	M9
A10	K11	K2
A11	L9	L4
BA0	G9	G4
BA1	G4	G9
BA2	H3	H10

BLOCK DIAGRAM (4Mbit x 32I/O x 8 Bank)

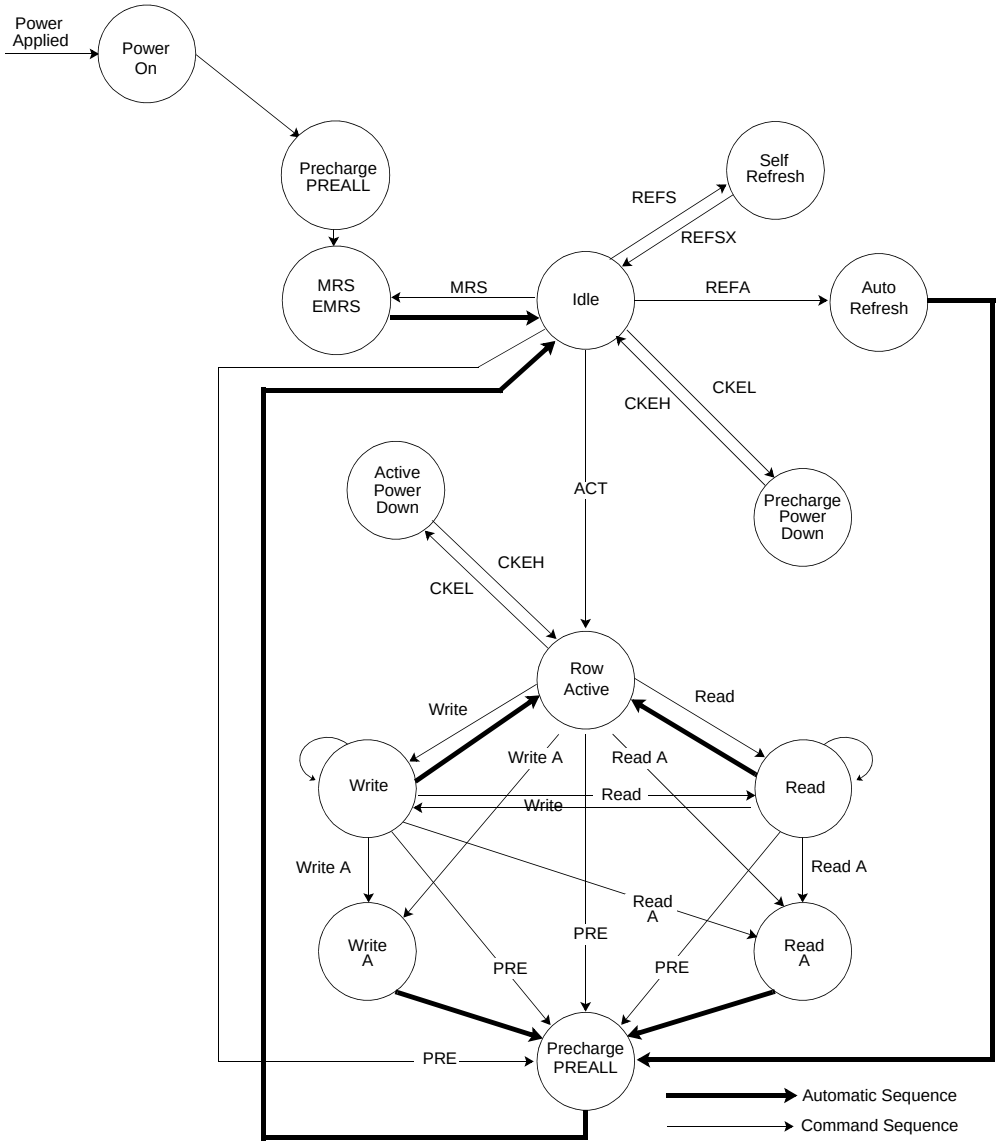


Note :
1. Both $\overline{CS1}$ and A12 are not enabled simultaneously each mode.
   - 2CS mode use both $\overline{CS0}$ and $\overline{CS1}$, but don't care A12.
   - 1CS mode use $\overline{CS0}$ and row address A12 instead of $\overline{CS1}$.

* iCK : internal clock

FUNCTIONAL DESCRIPTION

Simplified State Diagram



PREALL = Precharge All Banks
MRS = Mode Register Set
EMRS = Extended Mode Register Set
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
REFA = Auto Refresh

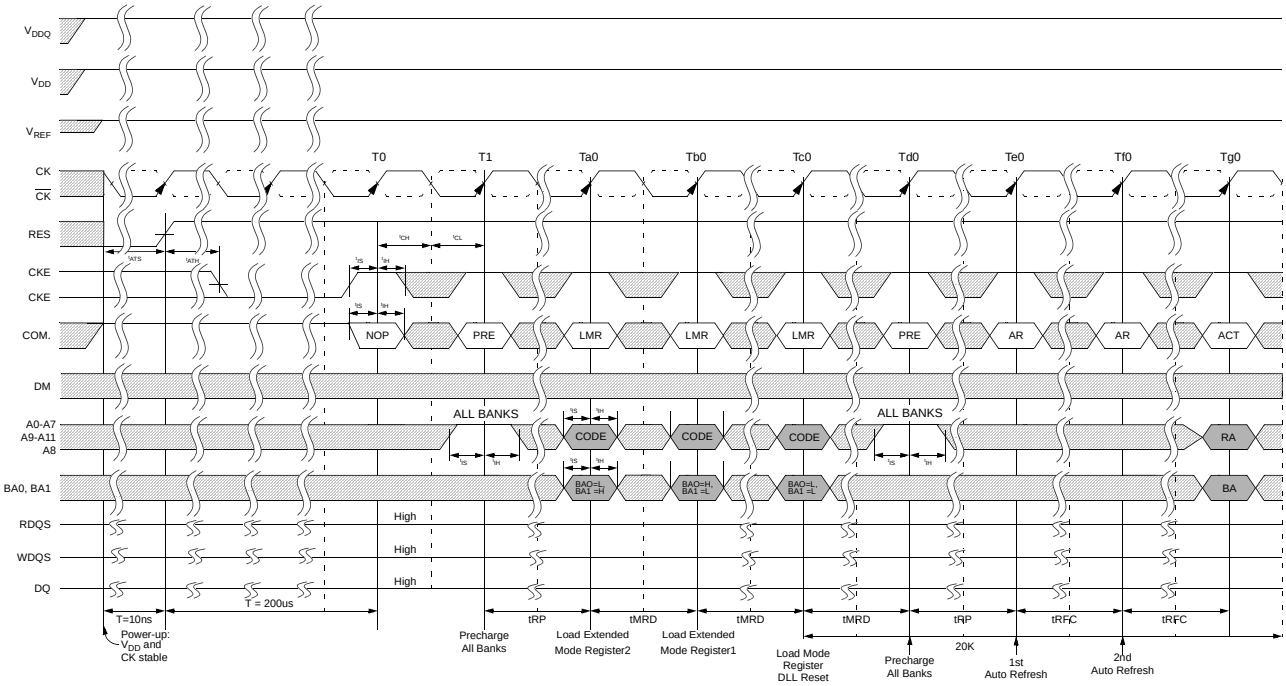
CKEL = Enter Power Down
CKEH = Exit Power Down
ACT = Active
Write A = Write with Autoprecharge
Read A = Read with Autoprecharge
PRE = Precharge

INITIALIZATION for 1CS Mode($\overline{CS0}$)

GDDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

1. Apply power and keep CKE/RESET at low state (All other inputs may be undefined)
   - Apply VDD and VDDQ simultaneously
   - Apply VDDQ before Vref. (Inputs are not recognized as valid until after V_{REF} is applied)
   - The VDD voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min and the power voltage ramps are without any slope reversal
2. Required minimum 100us for the stable power before RESET pin transition to HIGH
   - Upon power-up, the address/command active termination value will be set automatically based on the state of RESET and CKE.
   - On the rising edge of RESET the CKE pin is latched to determine the address and command bus termination value.
     If CKE is sampled at a zero, the address termination is set to 1/2 of ZQ.
     If CKE is sampled at a one, the address termination is set to ZQ.
   - RESET must be maintained at a logic LOW level and CS at a logic high value during power-up to ensure that the DQ outputs will be in a High-Z state, all active terminators off, and all DLLs off.
3. Minimum 200us delay required prior to applying any executable command after stable power and clock.
4. Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, then RESET and CKE should be brought to HIGH.
5. Issue a PRECHARGE ALL command following after NOP command.
6. Issue a EMRS2 command (BA1BA0="10") to select operating mode.
7. Issue a EMRS1 command (BA1BA0="01") to enable the DLL.
8. Issue MRS command (BA0BA1 = "00") to reset the DLL and to program the operating parameters.
   20K clock cycles are required between the DLL to lock.
9. Issue a PRECHARGE ALL command
10. Issue at least two AUTO refresh commands to update the driver impedance and calibrate the output drivers.

Following these requirements, the GDDR3 SDRAM is ready for normal operation.



INITIALIZATION for 2CS Mode($\overline{CS0}$ / $\overline{CS1}$)

GDDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

1. Apply power and keep CKE/RESET at low state (All other inputs may be undefined)
   - Apply VDD and VDDQ simultaneously
   - Apply VDDQ before Vref. (Inputs are not recognized as valid until after V_{REF} is applied)
   - The VDD voltage ramp time must be no greater than 200 ms from when VDD ramps from 300 mV to VDD min and the power voltage ramps are without any slope reversal
2. Required minimum 100us for the stable power before RESET pin transition to HIGH
   - Upon power-up, the address/command active termination value will be set automatically based on the state of RESET and CKE.
   - On the rising edge of RESET the CKE pin is latched to determine the address and command bus termination value.
     If CKE is sampled at a zero, the address termination is set to 1/2 of ZQ.
     If CKE is sampled at a one, the address termination is set to ZQ.
   - RESET must be maintained at a logic LOW level and CS at a logic high value during power-up to ensure that the DQ outputs will be in a High-Z state, all active terminators off, and all DLLs off.
3. Minimum 200us delay required prior to applying any executable command after stable power and clock.
4. Once the 200us delay has been satisfied, a DESELECT or NOP command should be applied, then RESET and CKE should be brought to HIGH,
5. Issue a PRECHARGE ALL command following after NOP command.
6. Issue a EMRS2 command (BA1BA0="10") to select operating mode
7. Issue a EMRS1 command (BA1BA0="01") to enable the DLL and BA2 = 1 to enable the 2CS mode.
8. Issue MRS command (BA0BA1 = "00") to reset the DLL and to program the operating parameters.
   20K clock cycles are required between the DLL to lock.

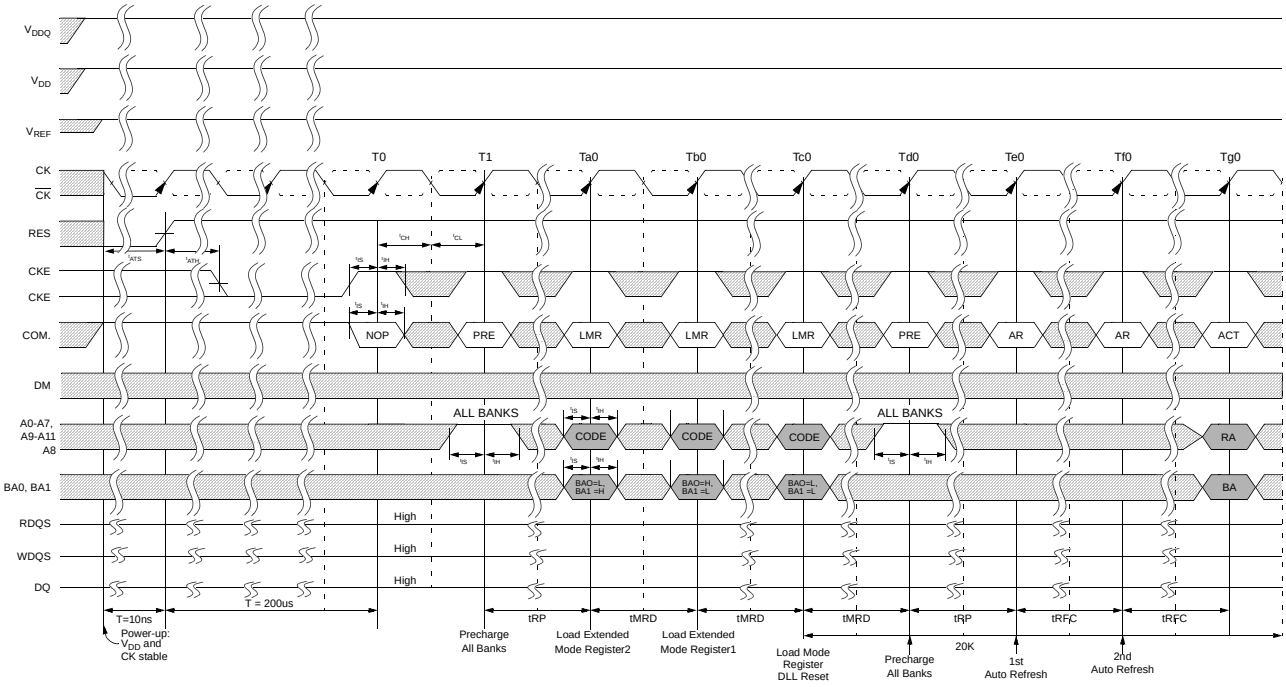
9-1. Issue $\overline{CS0}$ a PRECHARGE ALL command

9-2. Issue $\overline{CS1}$ a PRECHARGE ALL command

For initialization only, we do issue the CS0 and CS1 simultaneously.

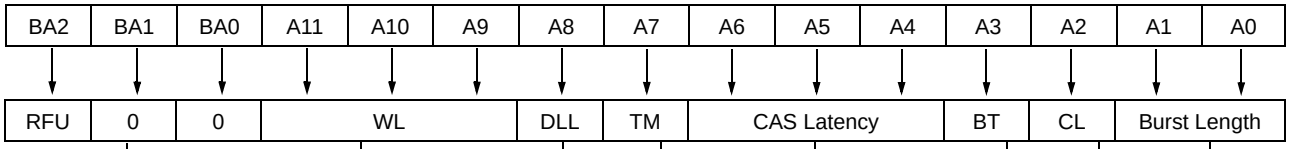
10. Issue at least two AUTO refresh commands to update the driver impedance and calibrate the output drivers.

Following these requirements, the GDDR3 SDRAM is ready for normal operation.



MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of GDDR3 SDRAM. It programs CAS latency, addressing mode, test mode and various vendor specific options to make GDDR3 SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for the proper operation. The mode register is written by asserting low on $\overline{CS0}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The GDDR3 SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A11 and BA0, BA1, BA2 in the same cycle as $\overline{CS0}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum clock cycles specified as tMRD are required to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The Burst length uses A0 ~ A1. CAS latency (read latency from column address) uses A2, A6 ~ A4. A7 is used for test mode. A8 is used for DLL reset. A9 ~ A11 are used for Write latency. Refer to the table for specific codes for various addressing modes and CAS latencies.



BA_1	BA_0	A_n ~ A_0
0	0	MRS
0	1	EMRS

Test Mode

A_7	mode
0	Normal
1	Test

Burst Type

A_3	Burst Type
0	Sequential
1	Reserved

DLL

A_8	DLL Reset
0	No
1	Yes

Note : DLL reset is self-clearing

Write Latency

A_{11}	A_{10}	A_9	Write Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

RFU(Reserved for future use) should stay "0" during MRS cycle

CAS Latency

A_2	A_6	A_5	A_4	CAS Latency
0	0	0	0	8
0	0	0	1	9
0	0	1	0	10
0	0	1	1	11
0	1	0	0	Reserved
0	1	0	1	Reserved(5)
0	1	1	0	Reserved(6)
0	1	1	1	7
1	0	0	0	12
1	0	0	1	13
1	0	1	0	14
1	0	1	1	15
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Burst Length

A_1	A_0	Burst Length
0	0	Reserved
0	1	Reserved
1	0	4
1	1	8

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER AND ACTIVE TERMINATOR

The GDDR3 SDRAM is equipped with programmable impedance output buffers and Active Terminators. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor(RQ) is connected between the ZQ pin and Vss. The value of the resistor must be six times of the desired output impedance.
For example, a 240Ω resistor is required for an output impedance of 40 Ω. To ensure that output impedance is one sixth the value of RQ (within 10 %), the range of RQ is 120Ω to 360Ω (20Ω to 60Ω) output impedance.
MF,SEN, RES, CK and CK are not internally terminated. CK and /CK will be terminated on the system module using external 1% resisters. The output impedance is updated during all AUTO REFRESH commands and NOP commands when a READ is not in progress to compensate for variations in voltage supply and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during update. To guarantee optimum output driver impedance after power-up, the GDDR3(x32) needs at least 20us after the clock is applied and stable to calibrate the impedance upon power-up. The user may operate the part with less than 20us, but the optimal output impedance is not guaranteed. The value of ZQ is also used to calibrate the internal address/command termination resisters. The two termination values that are selectable during power up are 1/2 of ZQ and ZQ. The value of ZQ is used to calibrate the internal DQ termination resisters. The two termination values that are selectable are 1/4 of ZQ and 1/2 of ZQ.

BURST LENGTH

Read and write accesses to the GDDR3 SDRAM are burst oriented, with the burst length being programmable, as shown in MRS table. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equals to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2-A*i* when the burst length is set to four (Where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmable burst length applies to both READ and WRITE bursts.

BURST TYPE

Accesses within a given burst must be programmed to be sequential; this is referred to as the burst type and is selected via bit M3. This device does not support the interleaved burst mode found in DDR SDRAM devices. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in below table: Burst Definition

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst
				Type= Sequential
4	A2	A1	A0	
	0	X	X	0 - 1 - 2 - 3
8	A2	A1	A0	
	0	X	X	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	1	X	X	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3

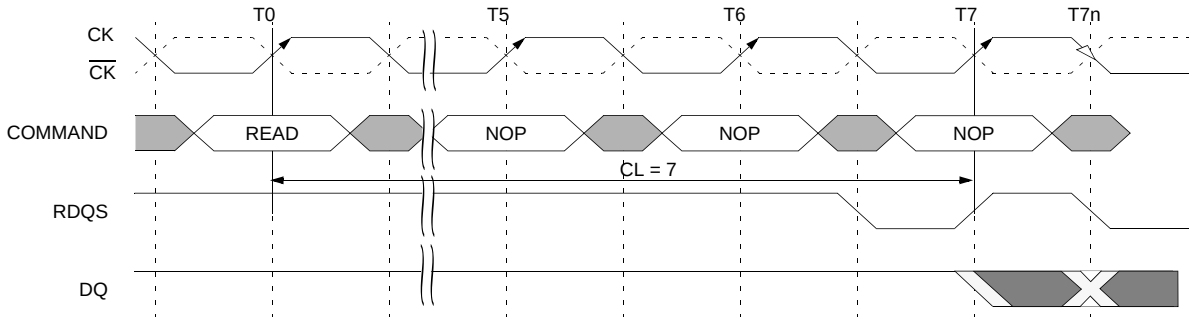
Note : 1. For a burst length of four, A2-A7 select the block of four burst.
2. For a burst length of eight, A3-A7 select the block of eight burst; A2 select the starting column within the block.
3. The value X of A0 and A1 column is "Don't care".

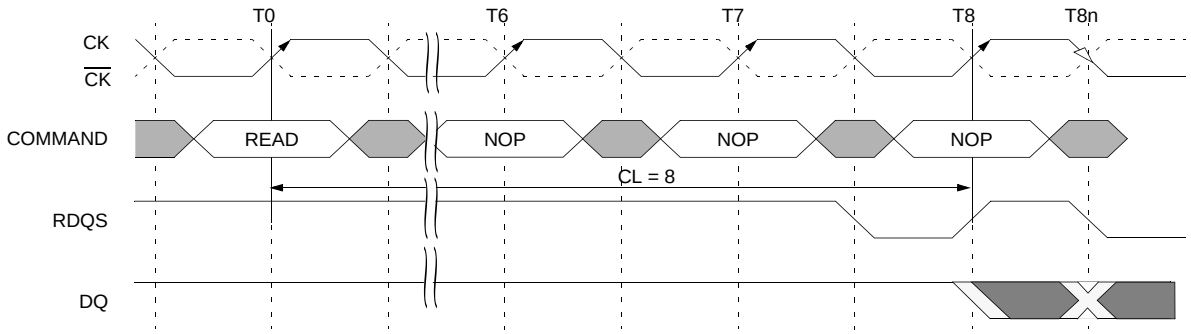
CAS LATENCY (READ LATENCY)

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 7~15 clocks. If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n*+*m*. Below table indicates the operating frequencies at which each CAS latency setting can be used. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latency

SPEED	Allowable CAS Latency				
	CL=15	CL=14	CL=12	CL=11	CL=10
1300MHz	O	-	-	-	-
1200MHz	O	O	-	-	-
1000MHz	O	O	O	-	-
800MHz	O	O	O	O	-
700MHz	O	O	O	O	O



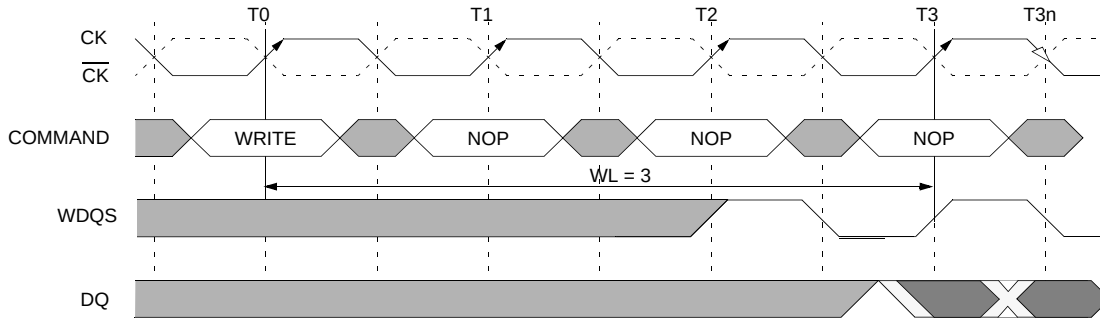


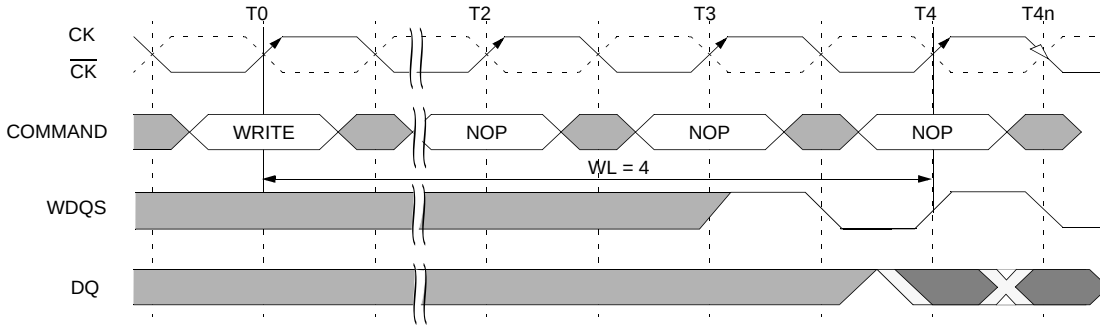
Burst Length = 4 in the cases shown
Shown with nominal t_{AC} and nominal t_{DSDQ}

DON'T CARE TRANSITIONING DATA

WRITE LATENCY

The Write latency (WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data. The latency can be set from 1 to 7 clocks depending in the operating frequency and desired current draw. If a WRITE command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n+m*. Reserved states should not be used as unknown operation or incompatibility with future versions may result.





Burst Length = 4 in the cases shown

DON'T CARE TRANSITIONING DATA

TEST MODE

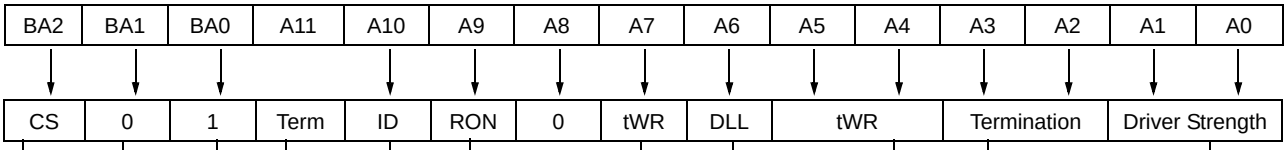
The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7 set to zero, and bits A0-A6 and A8-A11 set to the desired values. Test mode is entered by issuing a MODE REGISTER SET command with bit A7 set to one, and bits A0-A6 and A8-A11 set to the desired values. Test mode functions are specific to each DRAM manufacturer and its exact functions are hidden from the user.

DLL RESET

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to zero, and bits A0-A6 and A8-A11 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits A0-A7 and A9-A11 set to the desired values. When a DLL Reset is complete the GDDR3 SDRAM reset bit 8 of the mode register to a zero. After DLL Reset MRS, Power down can not be issued within 10 clocks.

EXTENDED MODE REGISTER SET1(EMRS1)

The extended mode register stores the data output driver strength and on-die termination options. The extended mode register is written by asserting low on CS0, RAS, CAS, WE and high on BA0(The GDDR3 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A11 and BA0,BA1,BA2 in the same cycle as CS0, RAS, CAS and WE going low are written in the extended mode register. The minimum clock cycles specified as tMRD are required to complete the write operation in the extended mode register. Four kinds of the output driver strength are supported by EMRS (A1, A0) code. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. "High" on BA0 is used for EMRS1. Refer to the table for specific codes.



BA_1	BA_0	A_n ~ A_0
0	0	MRS
0	1	EMRS1

Vendor ID

A_{10}	Vendor ID
0	Off
1	On

DLL

A_6	DLL
0	Enable
1	Disable

Drive Strength

A_1	A_0	Driver Strength
0	0	Autocal
0	1	30Ω
1	0	40Ω
1	1	50Ω

ADDR/CMD Termination

A_{11}	Termination
0	Default
1	Half of default

Default value is determined by CKE status at the rising edge of RESET during power-up

Ron of Pull-up

A_9	RON
0	40Ω
1	60Ω

tWR

A_7	A_5	A_4	tWR
0	0	0	11
0	0	1	13
0	1	0	5
0	1	1	15
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10

Data Termination

A_3	A_2	Termination
0	0	ODT Disabled*1
0	1	Reserved
1	0	ZQ/4
1	1	ZQ/2

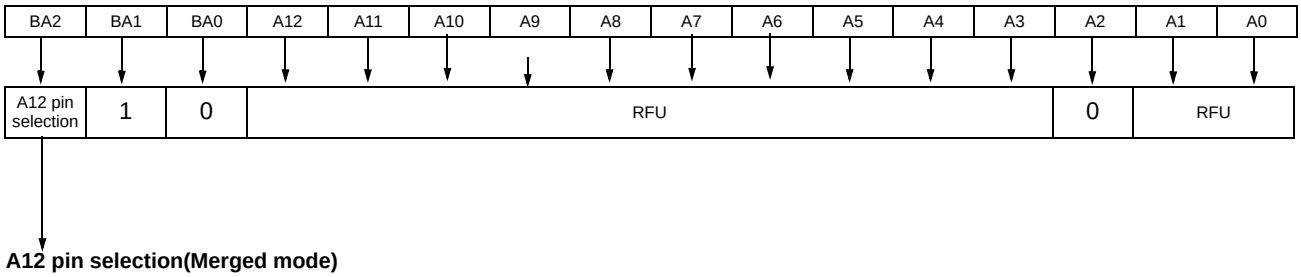
* ZQ : Resistor connection pin for On-die termination
* 1 : ALL ODT will be disabled

CS mode set

BA2	CS mode
0	1CS
1	2CS

* 2CS has two kinds of fully independent 8banks which are selected by CS0 and CS1
* 1CS has 8banks which is selected by CS0 and A12 of columm address.
* Default mode is 1CS before issuing BA2 EMRS.

EXTENDED MODE REGISTER SET2(EMRS2)



A12 pin selection(Merged mode)

BA2	A12 pin position
0	A12(J2 pin): Non-Merged
1	A12/ $\overline{CS1}$ (J3 pin): Merged

* Note : After selecting A12 pin position between J2 and J3 pin by EMRS2, 1Gb GDDR3 set CS1 mode by EMRS1

* Refer to the page4 to 6 for the pin configuration

* RFU(Reserved for future use) should stay "0" during EMRS cycle

MRS set usage for CS mode and Merged mode

CS Mode MRS set	Merged mode=0	Merged mode=1
0	1CS	1CS
1	2CS	2CS

DLL ENABLE/DISABLE

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after disabling the DLL for debugging or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 20K clock cycles must occur before a READ command can be issued.

DATA TERMINATION

The Data Termination, DT, is used to determine the value of the internal data termination resisters. The GDDR3 SDRAM supports 60Ω and 120Ω termination. The termination may also be disabled for testing and other purposes.

DATA DRIVER IMPEDANCE

The Data Driver impedance (DZ) is used to determine the value of the data drivers impedance. When autocalibration is used the data driver impedance is set to RQ/6 and it's tolerance is determined by the calibration accuracy of the device. When any other value is selected the target impedance is set nominally to the desired impedance. However, the accuracy is now determined by the device's specific process corner, applied voltage and operating temperature.

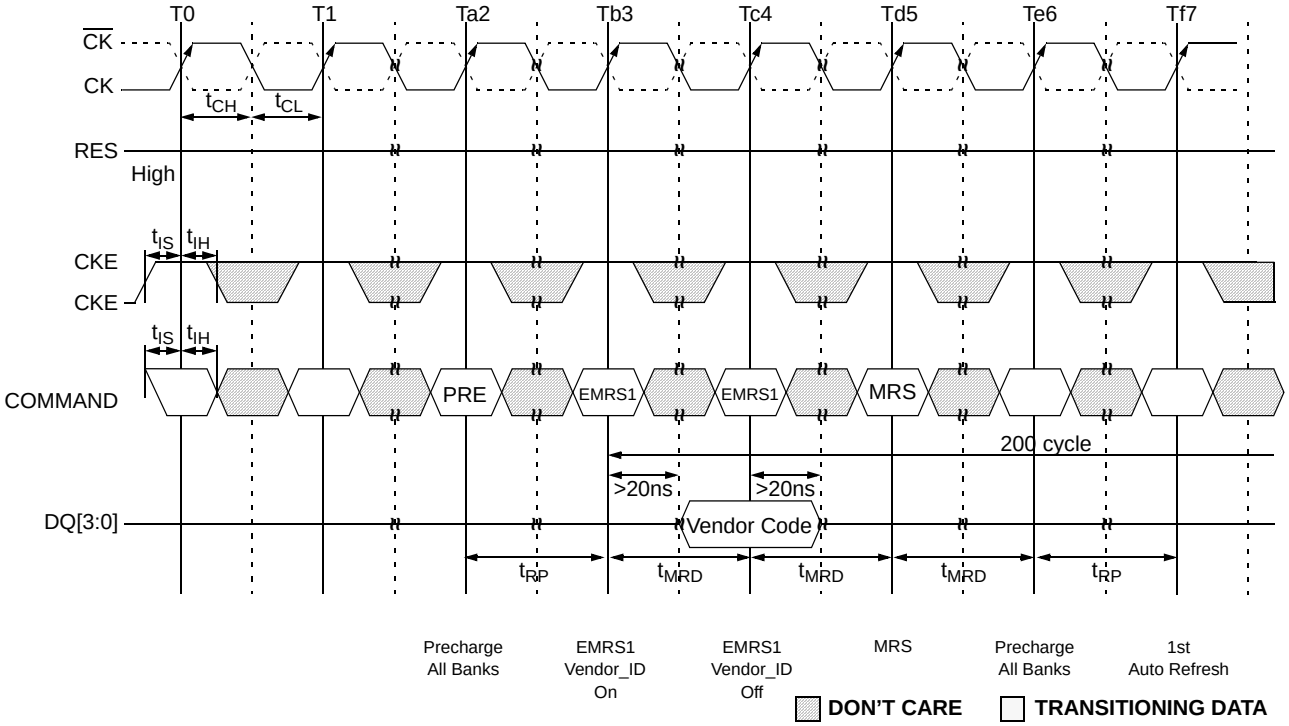
MANUFACTURERS VENDOR CODE AND REVISION IDENTIFICATION

The Manufacturers Vendor Code, V, is selected by issuing a EXTENDED MODE REGISTER SET command with bits A10 set to one, and bits A0-A9 and A11 set to the desired values. When the V function is enabled the GDDR3 SDRAM will provide its manufacturers vendor code on DQ[3:0] and revision identification on DQ[7:4]

Manufacturer	DQ[3:0]	DQ[7:4]
Samsung	1 [0001]	1 [0001]

DQs	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
Vendor ID	1	0	0	0	1	0	0	0

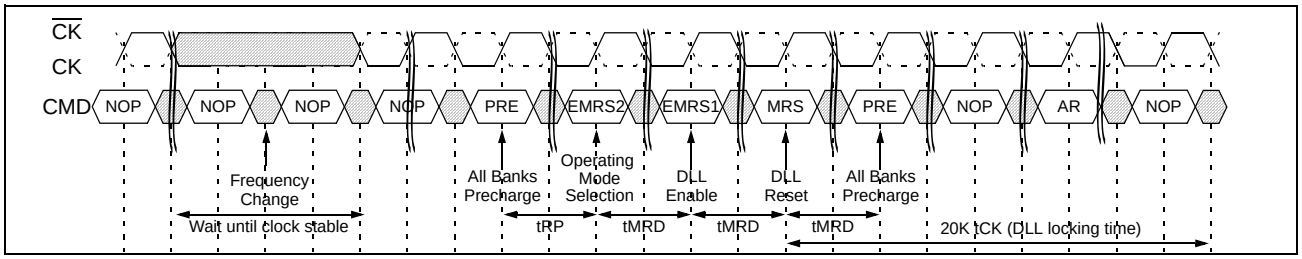
Vendor ID Read



Clock frequency change sequence during the device operation

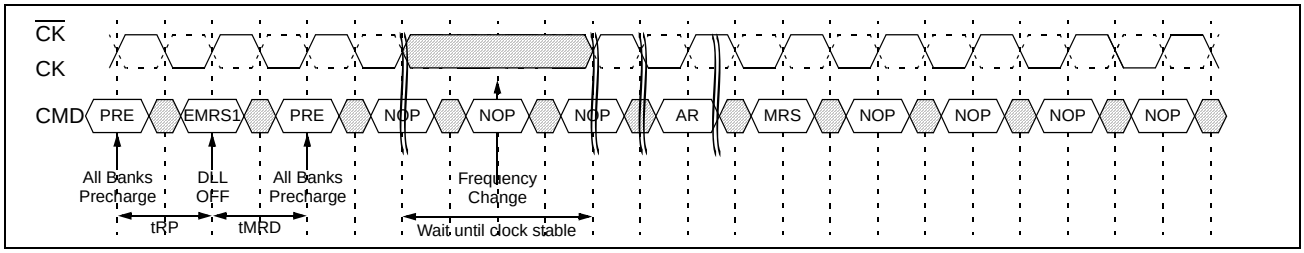
Both existing tCK and desired tCK are in DLL-On mode

- Change frequency from existing frequency to desired frequency
- Issue Precharge All Banks command
- Issue EMRS2 command to select the operating mode
- Issue EMRS1 command to enable DLL
- Issue MRS command to reset the DLL while other fields are valid and required 20K tCK to lock the DLL
- Issue Precharge All Banks command. Issue at least Auto-Refresh command



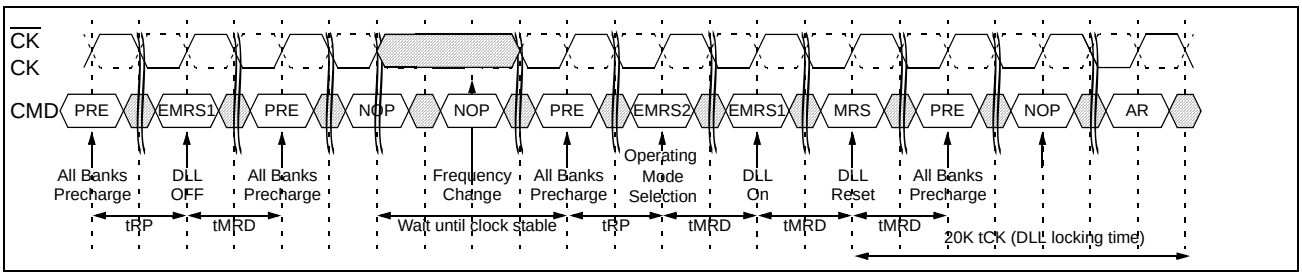
Existing tCK is in DLL-on mode while desired tCK is in DLL-off mode

- Issue Precharge All Banks command
- Issue EMRS1 command to disable the DLL
- Issue Precharge All Banks command
- Change the frequency from existing to desired.
- Issue Auto-Refresh command at least two. Issue MRS command



Clock frequency change in case existing tCK is in DLL-off mode while desired tCK is in DLL-on mode

- Issue Precharge All Banks command and issue EMRS1 command to disable the DLL.
- Issue Precharge All Banks command.
- Change the clock frequency from existing to desired
- Issue Precharge All Banks command.
- Issue EMRS2 command to select the operating mode
- Issue EMRS1 command to enable the DLL
- Issue MRS command to reset the DLL and required 20K tCK to lock the DLL.
- Issue Precharge All Banks command.
- Issue Auto-Refresh command at least two



BOUNDARY SCAN FUNCTION

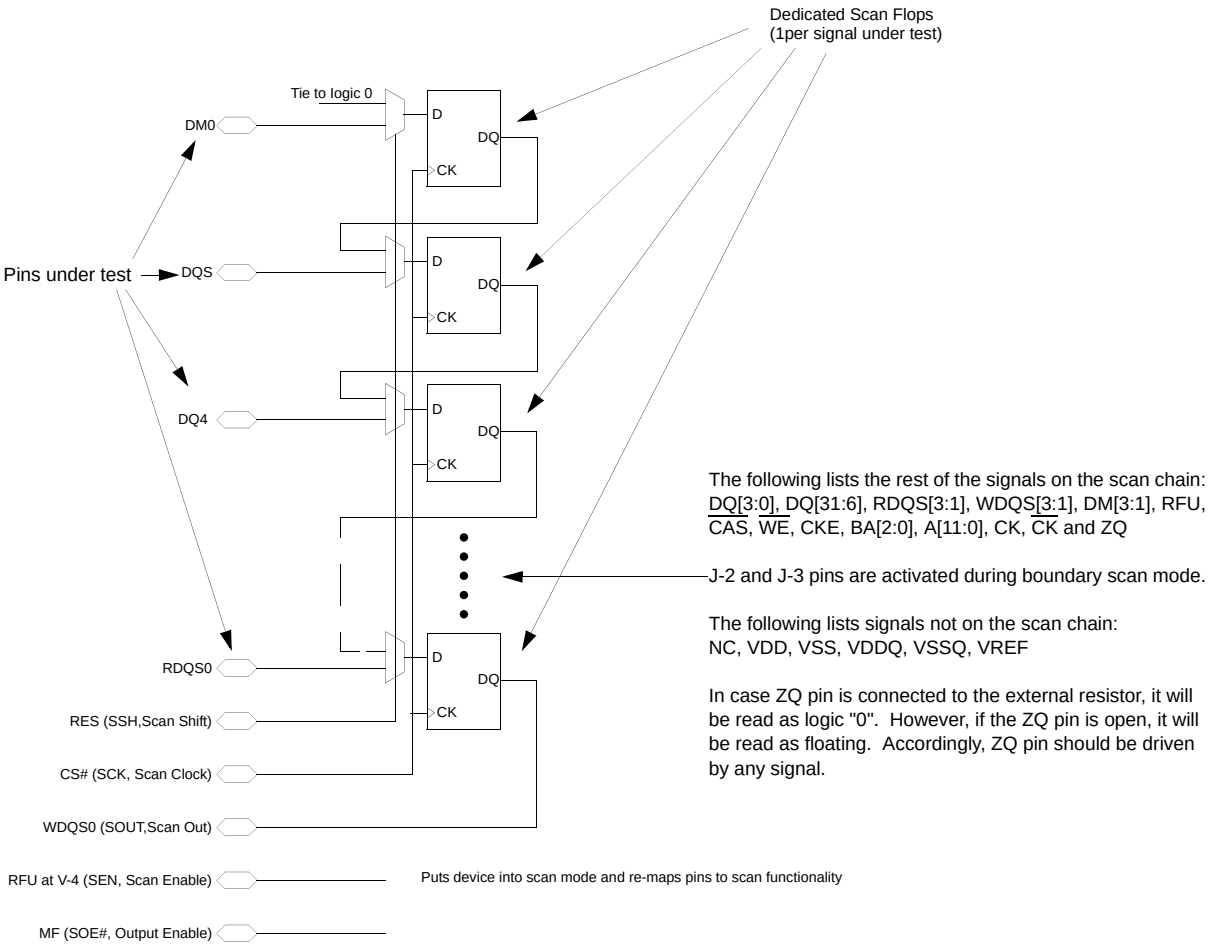
GENERAL INFORMATION

The 1Gb GDDR3 incorporates a modified boundary scan test mode as an optional feature. This mode doesn't operate in accordance with IEEE Standard 1149.1 - 1990. To save the current GDDR3 ball-out, this mode will scan parallel data input and output and the scanned data through WDQS0 pin controlled by an add-on pin, SEN which is located at V-4 of 136 ball package.
For the normal device operation other than boundary scan, there required device re-initialization by device power-off and then power-on.

DISABLING THE SCAN FEATURE

It is possible to operate the 1Gb GDDR3 without using the boundary scan feature. SEN(at V-4 of 136 ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RES, MF, WDQS0 and $\overline{CS}$ will be operating at normal GDDR3 functionalities when SEN is deasserted.

Figure 1. Internal Block Diagram (Reference Only)



BOUNDARY SCAN EXIT ORDER

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-3	13	E-10	25	K-11	37	R-10	49	L-3	61	G-4
2	C-2	14	F-10	26	K-10	38	T-11	50	M-2	62	F-4
3	C-3	15	E-11	27	K-9	39	T-10	51	M-4	63	F-2
4	B-2	16	G-10	28	M-9	40	T-3	52	K-4	64	G-3
5	B-3	17	F-11	29	M-11	41	T-2	53	K-3	65	E-2
6	A-4	18	G-9	30	L-10	42	R-3	54	K-2	66	F-3
7	B-10	19	H-9	31	N-11	43	R-2	55	L-4	67	E-3
8	B-11	20	H-10	32	M-10	44	P-3	56	J-3		
9	C-10	21	H-11	33	N-10	45	P-2	57	J-2		
10	C-11	22	J-11	34	P-11	46	N-3	58	H-2		
11	D-10	23	J-10	35	P-10	47	M-3	59	H-3		
12	D-11	24	L-9	36	R-11	48	N-2	60	H-4		

*Note :
1. When the device is in scan mode, the mirror function will be disabled and none of the pins are remapped.
2. Since the other input of the MUX for DM0 tied to GND, the device will output the continuous zeros after scanning a bit #67, if the chip stays in scan shift mode.

SCAN PIN DESCRIPTION

Package Ball	Symbol	Normal Function	Type	Description
V-9	SSH	RES	Input	Scan shift. Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
F-9	SCK	CS	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock.
D-2	SOUT	WDQS0	Output	Scan Output.
V-4	SEN	RFU	Input	Scan Enable. Logic HIGH would enable the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.
A-9	$\overline{SOE}$	MF	Input	Scan Output Enable. Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDD or GND through a resistor (typically 1K Ω) for normal operation. Tester needs to overdrive this pin guarantee the required input logic level in scan mode.

*Note :
1. When SEN is asserted, no commands are to be executed by the GDDR3. This applies to both user commands and manufacturing commands which may exist while RES is deasserted.
2. All scan functionalities are valid only after the appropriate power-up and initialization sequence. (RES and CKE, to set the ODT of the C/A)
3. In scan mode, the ODT for the address and control lines set to a nominal termination value of ZQ. The ODT for DQ's will be disabled. It is not necessary for the termination to be calibrated.
4. In a double-load clam-shell configuration, SEN will be asserted to both devices. Separate two $\overline{SOE}$'s should be provided to top and bottom devices to access the scanned output. When either of the devices is in scan mode, $\overline{SOE}$ for the other device which not in a scan will be disabled.

SCAN DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

PARAMETER/CONDITON	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF}+0.15	-	V	1,2
Input Low (Logic 0) Voltage	V_{IL}(DC)	-	V_{REF}-0.15	V	1,2

*Note : 1. The parameter applies only when SEN is asserted.
2. All voltages referenced to GND.

Figure 2. Scan Capture Timing

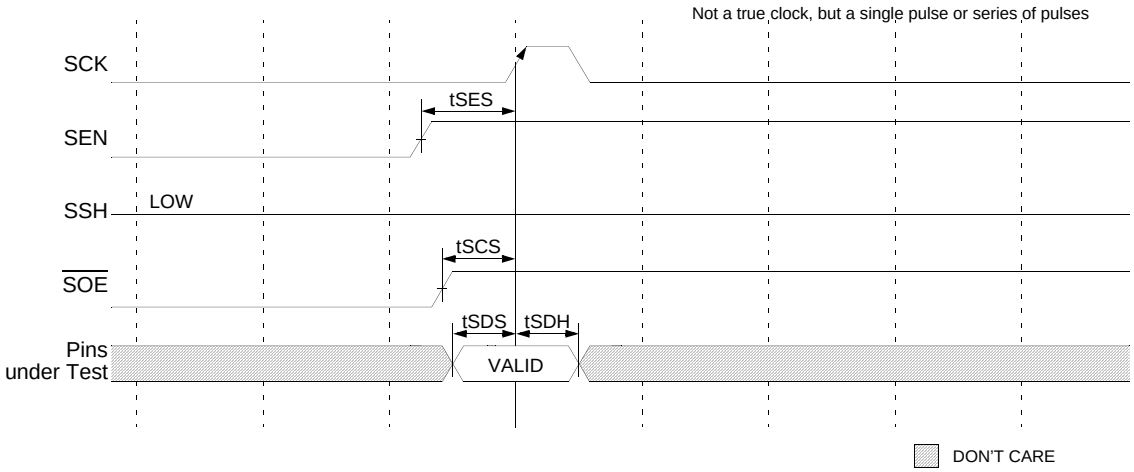
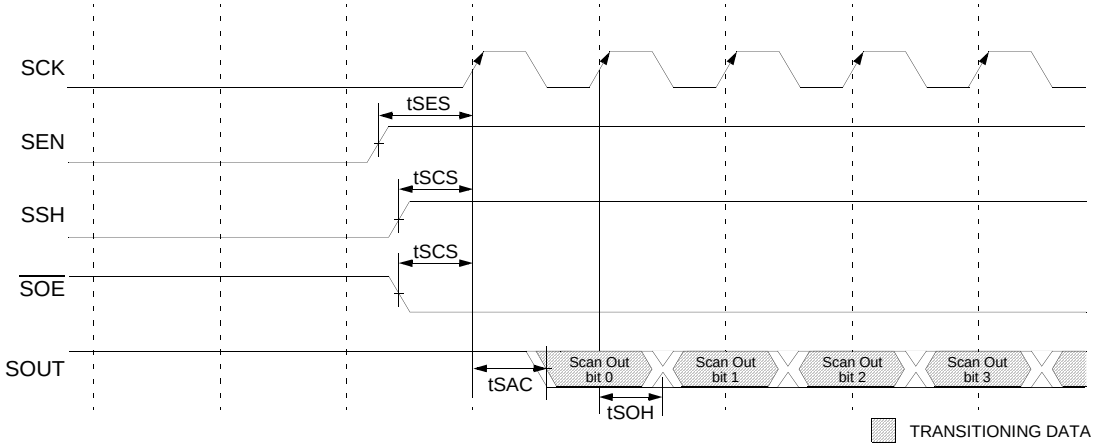


Figure 3.Scan Shift Timing

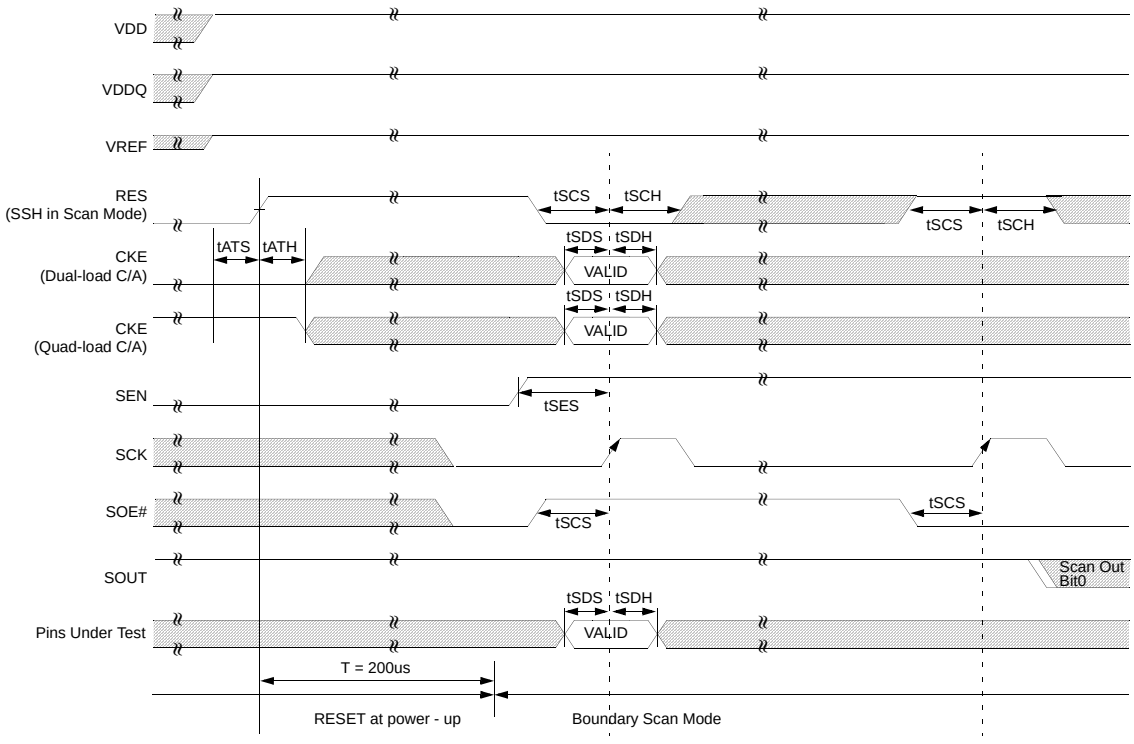


SCAN AC ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITON	SYMBOL	MIN	MAX	UNITS	NOTES
Clock					
Clock cycle time	tSCK	40	-	ns	1
Scan Command Time					
Scan enable setup time	tSES	20	-	ns	1,2
Scan enable hold time	tSEH	20	-	ns	1
Scan command setup time for SSH, SOE# and SOUT	tSCS	14	-	ns	1
Scan command hold time for SSH, SOE# and SOUT	tSCH	14	-	ns	1
Scan Capture Time					
Scan capture setup Time	tSDS	10	-	ns	1
Scan capture hold Time	tSDH	10	-	ns	1
Scan Shift Time					
Scan clock to valid scan output	tSAC	-	6	ns	1
Scan clock to scan output hold	tSOH	1.5	-	ns	1

*Note : 1. The parameter applies only when SEN is asserted.
2. Scan Enable should be issued earlier than other Scan Commands by 3ns.

Figure 4. Scan Initialization Sequence



Note : To set the pre-defined ODT for C/A, a boundary scan mode should be issued after an appropriate ODT initialization sequence with RES and CKE signals

COMMANDS

Below Truth Table-COMMANDs provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the operation section : these tables provide current state/next state information.

TRUTH TABLE - COMMANDs

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	8, 11
NO OPERATION (NOP)	L	H	H	H	X	8
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2
DATA TERMINATOR DISABLE	X	H	L	H	X	

TRUTH TABLE - DM Operation

Name (Function)	DM	DQS	NOTES
Write Enable	L	Valid	
Write Inhibit	H	X	10

Note :
1. CKE is HIGH for all commands except SELF REFRESH.
2. BA0~BA1 select either the mode register or the extended mode register (BA0=0, BA1=0 select the mode register; BA0=1, BA1=0 select extended mode register; other combinations of BA0~BA1 are reserved). A0~A11 provide the op-code to be written to the selected mode register.
3. BA0~BA2 provide bank address and A0~A11 provide row address.
4. BA0~BA2 provide bank address; A0~A7 and A9 provide column address; A8 HIGH enables the auto precharge feature (non persistent) , and A8 LOW disables the auto precharge feature.
5. A8 LOW : BA0~BA2 determine which bank is precharged.
   A8 HIGH : All banks are precharged and BA0~BA2 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; All inputs and I/Os are "Don't Care" except for CKE.
8. DESELECT and NOP are functionally interchangeable.
9. Cannot be in powerdown or self-refresh state.
10. Used to mask write data ; provided coincident with the corresponding data.
11. Except DATA Termination disable.

DESELECT

The DESELECT function (/CS high) prevents new commands from being executed by the GDDR3(x32). The GDDR3(x32) SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct selected GDDR3(x32) to perform a NOP (/CS LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0-A11. See mode register descriptions in the Register Definition section. The Load Mode Register command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0,BA1, BA2 inputs select the bank, and the address provided on inputs A0-A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1, BA2 inputs select the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1, BA2 inputs select the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on inputs A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW. the corresponding data will be written to memory; If the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one banks are to be precharged, inputs BA0,BA1,BA2 select the bank. Otherwise BA0, BA1,BA2 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command will be treated as a NOP if there is no open row is already in the process of precharging.

AUTO PRECHARGE

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A8 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enable or disabled for each individual READ or WRITE command. Auto precharge ensures that the precharge is initiated at the earliest valid state within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating $t_{RAS(min)}$, as described for each burst type in the operation section of this datasheet. The user must not issue another command to the same bank until the precharge time(t_{RP}) is completed.

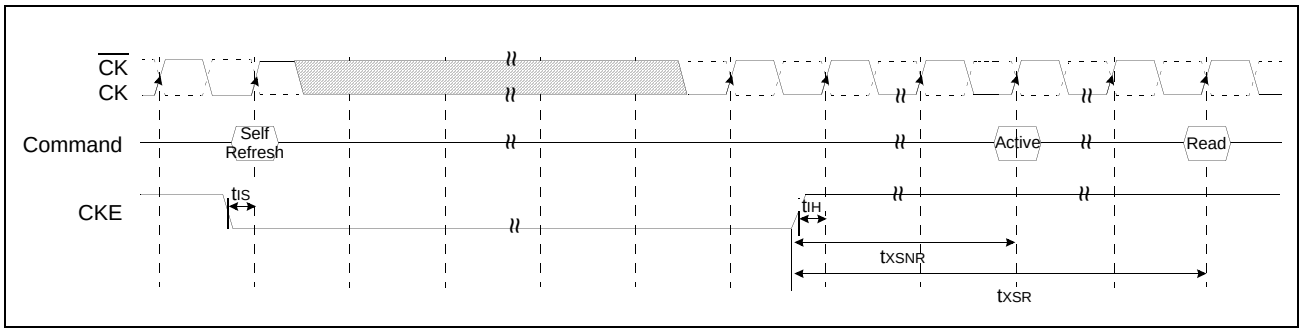
AUTO REFRESH

Auto Refresh is used during normal operation of the GDDR3 SDRAM and is analogous to /CAS-BEFORE-/RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an Auto Refresh command. The 1Gb(x32) GDDR3 requires Auto Refresh cycles at an average interval of 3.9us (maximum).

A maximum Auto Refresh commands can be posted to any given GDDR3(x32) SDRAM, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9 x 3.9us(35.1us). This maximum absolute interval is to allow GDDR3(x32) SDRAM output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR3(x32) SDRAM ,even if the rest of the system is powered down. SELF REFRESH command can be issued only in case all banks are in precharge state. When in the self refresh mode, the GDDR3(x32) SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. The active termination is also disabled upon entering Self Refresh and enabled upon exiting Self Refresh. (20K clock cycles must then occur before a READ command can be issued). Input signals except CKE & Reset are "Don't Care" during SELF REFRESH. The procedure for exiting self refresh requires a sequence of commands. First, CK and /CK must be stable prior to CKE going back HIGH. Once CKE is HIGH,the GDDR3(x32) must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and output calibration is to apply NOPs for 20K clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.



* Once the device enters the self refresh mode, it should be in NOP state at least for 10ns. The minimum duration for the power down mode once CKE brought to down should be at least 10ns.

DATA TERMINATOR DISABLE (BUS SNOOPING FOR READ COMMAND)

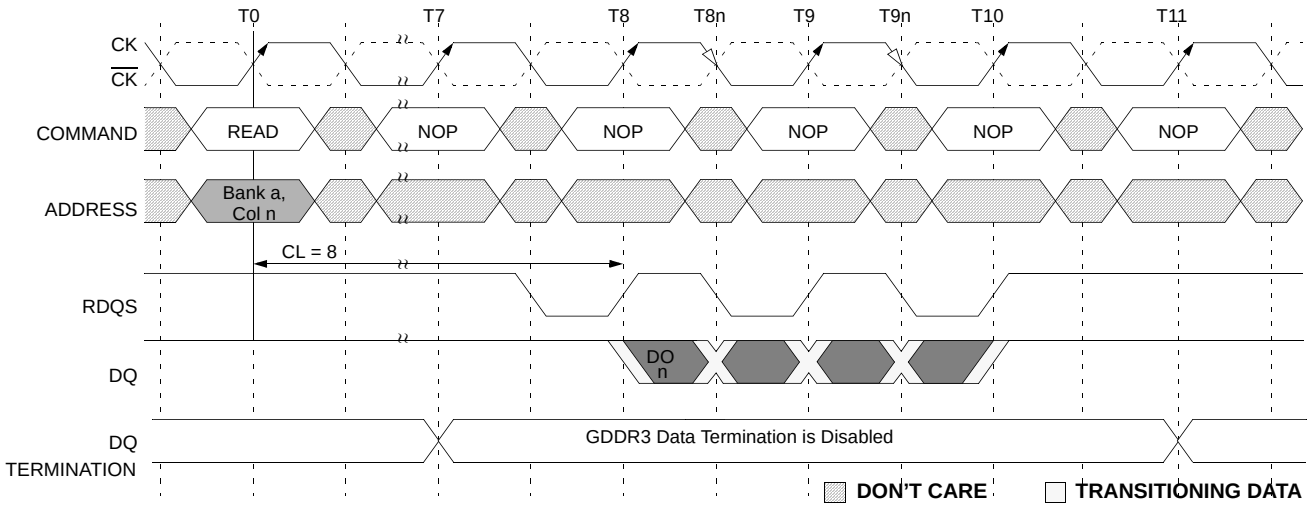
The DATA TERMINATOR DISABLE COMMAND is detected by the device by snooping the bus for READ commands excluding /CS. The GDDR3 SDRAM will disable its Data terminators when a READ command is detected. The terminators are disable CL-1 Clocks after the READ command is detected. In a two rank system both DRAM devices will snoop the bus for READ commands to either device and both will disable their terminators if a READ command is detected. The command and address terminators and always enabled.

ON-DIE TERMINATION

Bus snooping for READ commands other than $\overline{CS}$ is used to control the on-die termination in the dual load configuration. The GDDR3 SDRAM will disable the on-die termination when a READ command is detected, regardless of the state of $\overline{CS}$, when the ODT for the DQ pins are set for dual loads (120Ω). The on-die termination is disabled x clocks after the READ command where x equals CL-1 and stay off for a duration of BL/2 + 2, as below figure, Data Termination Disable Timing. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on-die termination if a READ command is detected. The on-die termination for all other pins on the device are always on for both a single-rank system and a dual-rank system.

The on-die termination value on address and control pins is determined during power-up in relation to the state of CKE on the first transition of RESET. On the rising edge of RESET, if CKE is sampled LOW, then the configuration is determined to be a single-rank system. The on-die termination is then set to one-half ZQ for the address pins. On the rising edge of RESET, if CKE is sampled HIGH, then the configuration is determined to be a dual-rank system. The on-die termination for the DQs, WDQS, and DM pins is set in the EMRS.

Data Termination Disable Timing



Note : 1. DO *n* = data-out from column *n*.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the specified order following DO *n*.
4. Shown with nominal t_{AC} and t_{DQSQ}.
5. RDQS will start driving high one-half cycle prior to the first falling edge.
6. The Data Terminators are disabled starting at CL-1 and the duration is BL/2 + 2
7. READS to either rank disable both ranks' termination regardless of the logic level of /CS.

OPERATIONS
BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a banks within the GDDR3 SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

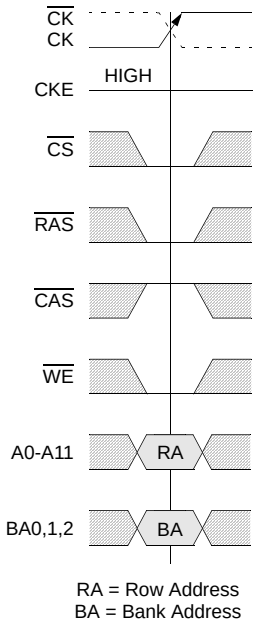
After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. $t_{RCD(min)}$ should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command in which a READ or WRITE command can be entered. For example, a t_{RCD} specification of 14ns with a 700MHz clock (1.4ns period) results in 10 clocks. This is reflected in below figure, which covers any case where $10<t_{RCD(min)}/t_{CK}\leq 11$.

The same procedure is used to convert other specification limits from time units to clock cycles.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed”(precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC}.

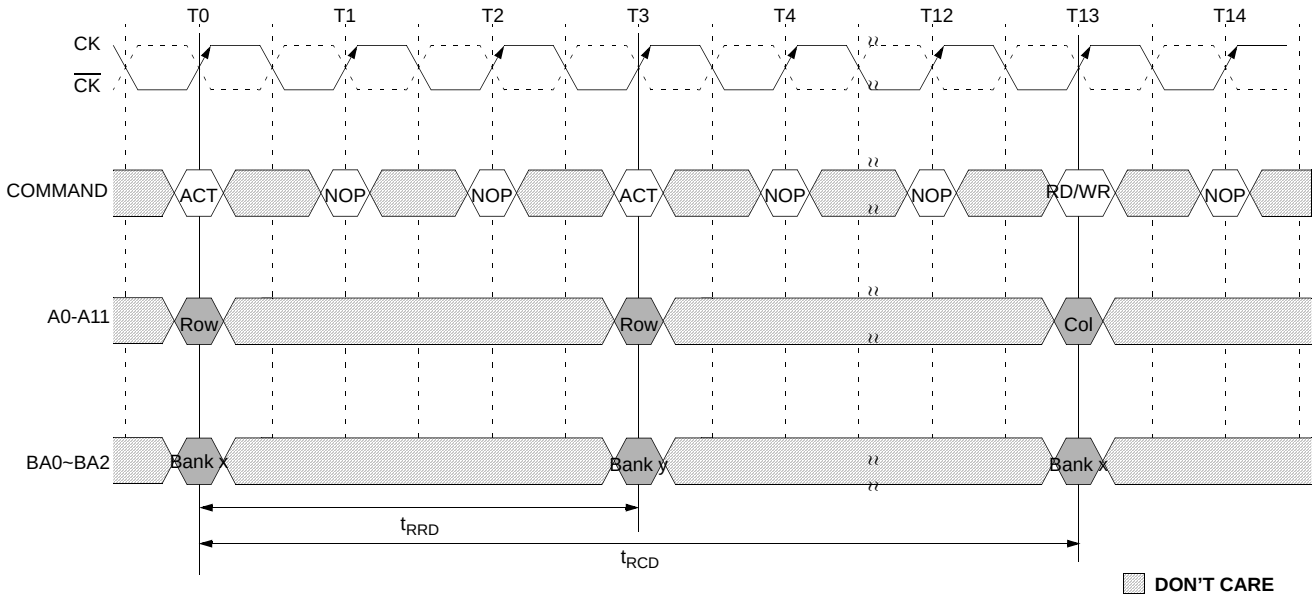
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

* Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.



Activating a Specific Row in a Specific Bank

Example : Meeting t_{RCD}



READs

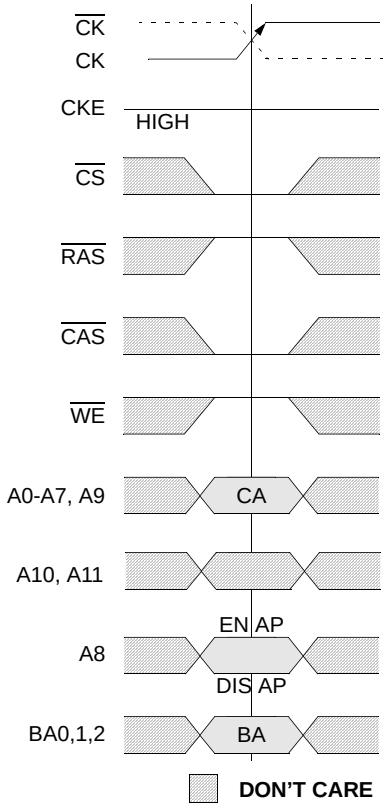
READ bursts are initiated with a READ command, as below figure. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after $t_{RAS(min)}$ has been met. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS Latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative strobe edge. READ burst figure shows general timing for 2 of the possible CAS latency settings. The GDDR3(x32) drives the output data edge aligned to the crossing of CK and $\overline{CK}$ and to RDQS. The initial HIGH transition LOW of RDQS is known as the read preamble; the half cycle coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of t_{DQSQ} (valid data-out skew), t_{DV} (data-out window hold), the valid data window are depicted in Data Output Timing (1) figure. A detailed explanation of t_{AC} (DQS and DQ transition skew to CK) is shown in Data Output Timing (2) figure.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued x cycles after the first READ command, where x equals the number of data element nibbles (nibbles are required by the 4*n*-prefetch architecture) depending on the burst length. This is shown in consecutive READ bursts figure. Nonconsecutive read data is shown for illustration in nonconsecutive READ bursts figure. Full-speed random read accesses within a page (or pages) can be performed as shown in Random READ accesses figure. Data from a READ burst cannot be terminated or truncated.

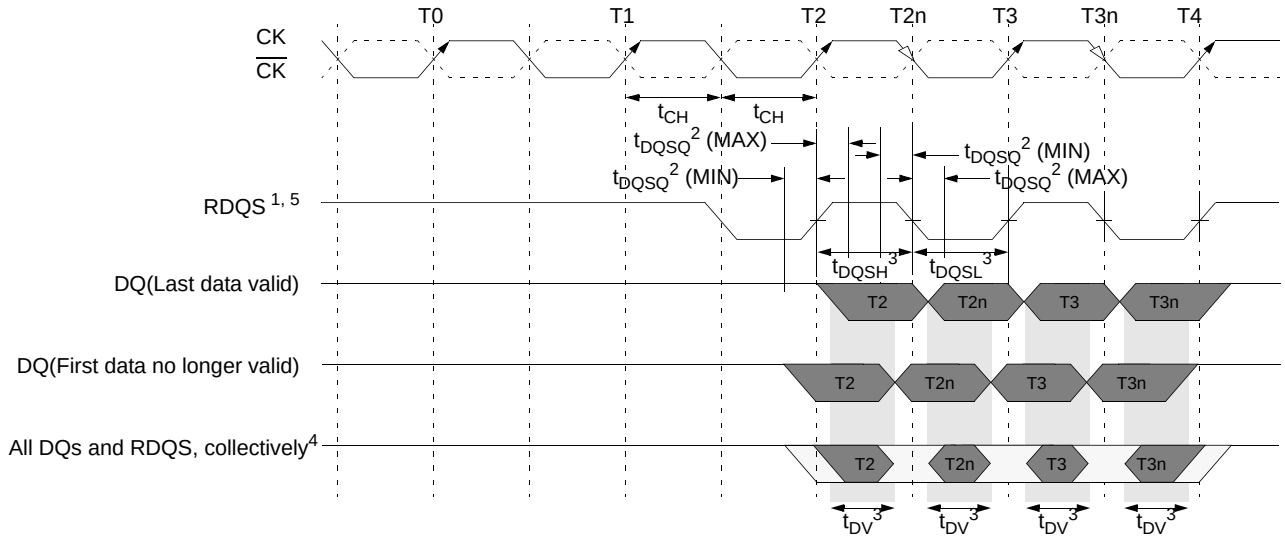
During READ commands the GDDR3 SDRAM disables its data terminators.



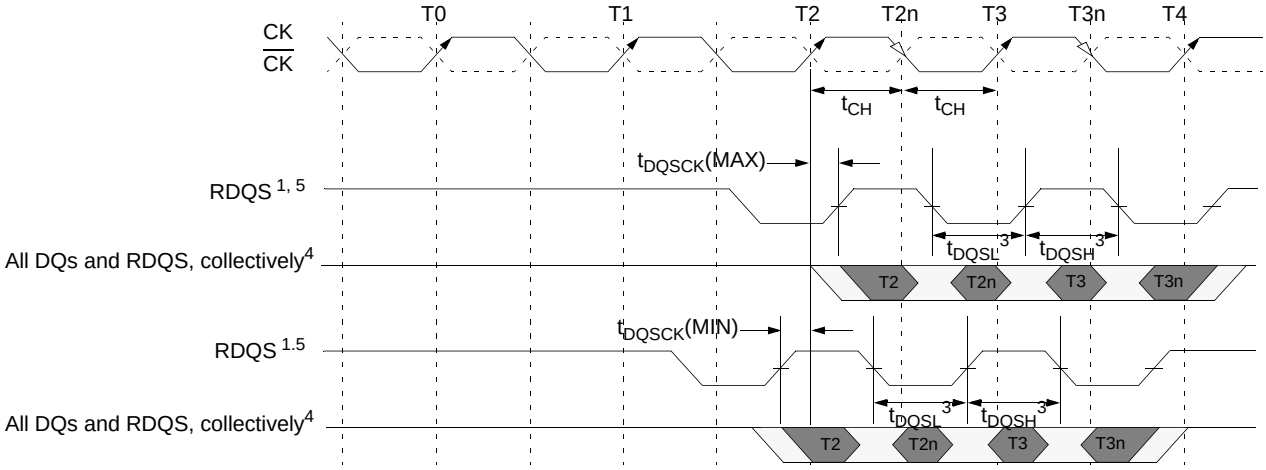
CA = Column Address
BA = Bank Address
EN AP = Enable Auto Precharge
DIS AP = Disable Auto Precharge

READ Command

Data Output Timing (1) - t_{DQSQ}, t_{QH} and Data Valid Window

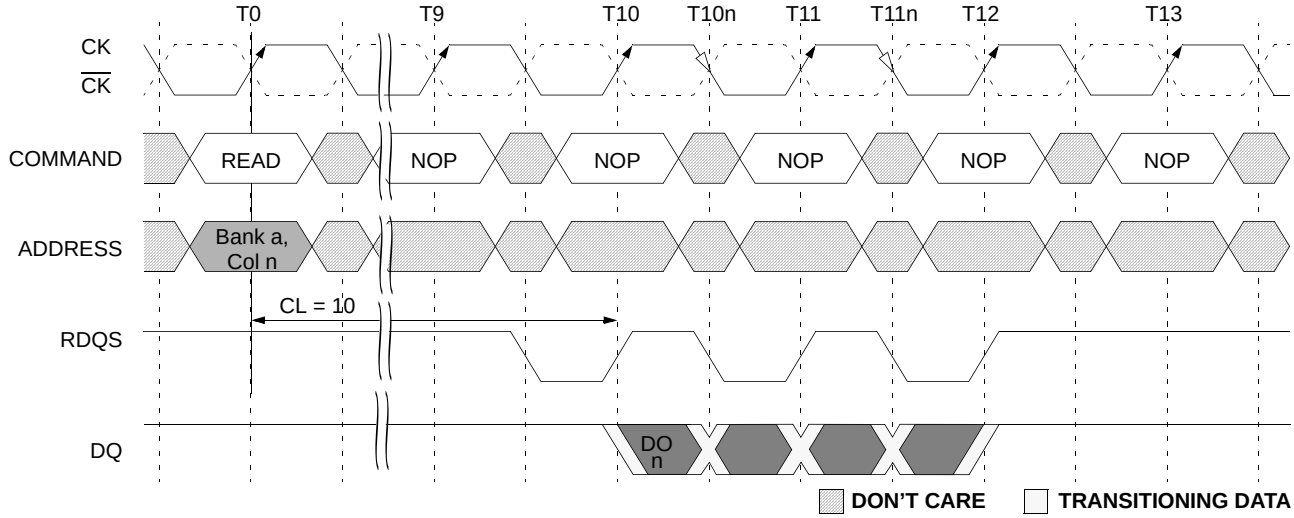


Data Output Timing (2) - t_{DQSQ}, t_{QH} and Data Valid Window



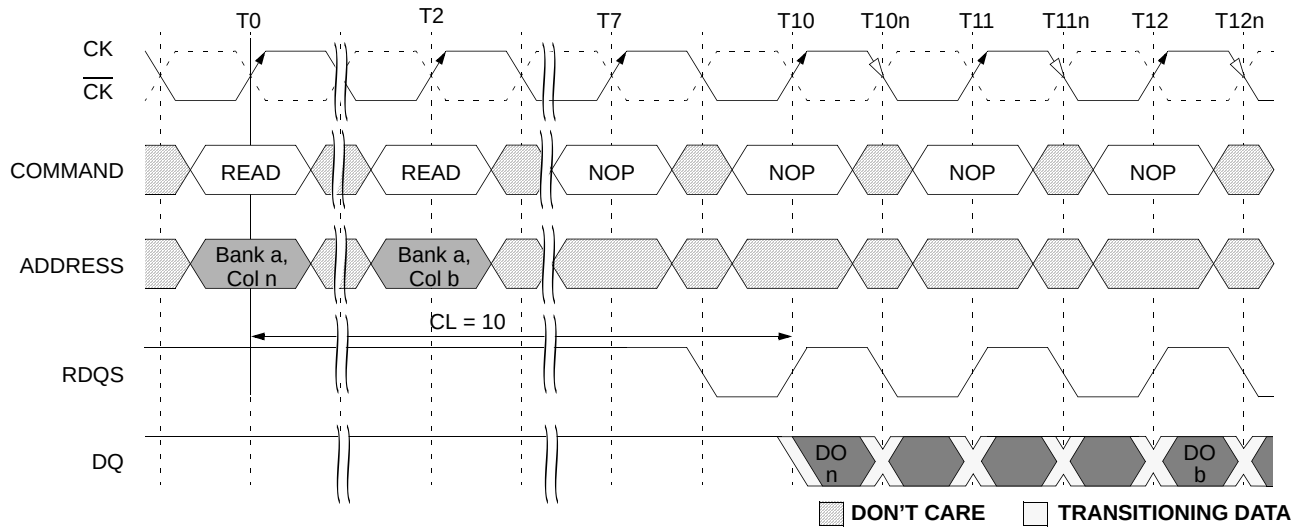
Note : 1. t_{DQSQ} represents the skew between the 8 DQ lines and the respective RDQS pin.
2. t_{DQSQ} is derived at each RDQS clock edge and is not cumulative over time and begins with first DQ transition and ends with the last valid transition of DQs.
3. The data valid window is derived for each RDQS transitions and is defined by t_{DV}.
4. There are 4 RDQS pins for this device with RDQS0 in relation to DQ0-DQ7, RDQS1 in relation DQ8-DQ15, RDQS2 in relation to DQ16-24 and RDQS3 in relation to DQ25-DQ31.
5. This diagram only represents one of the four byte lanes.

READ Burst



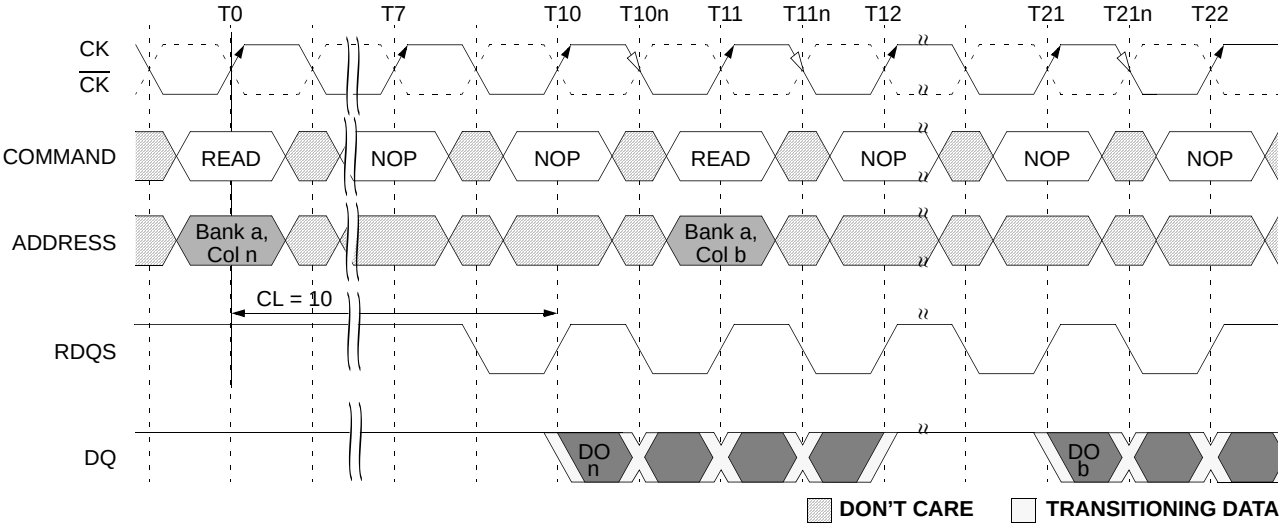
Note : 1. DO *n*=data-out from column *n*.
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Shown with nominal t_{AC} and t_{DQSQ}.
5. RDQS will start driving high 1/2 clock cycle prior to the first falling edge.

Consecutive READ Bursts



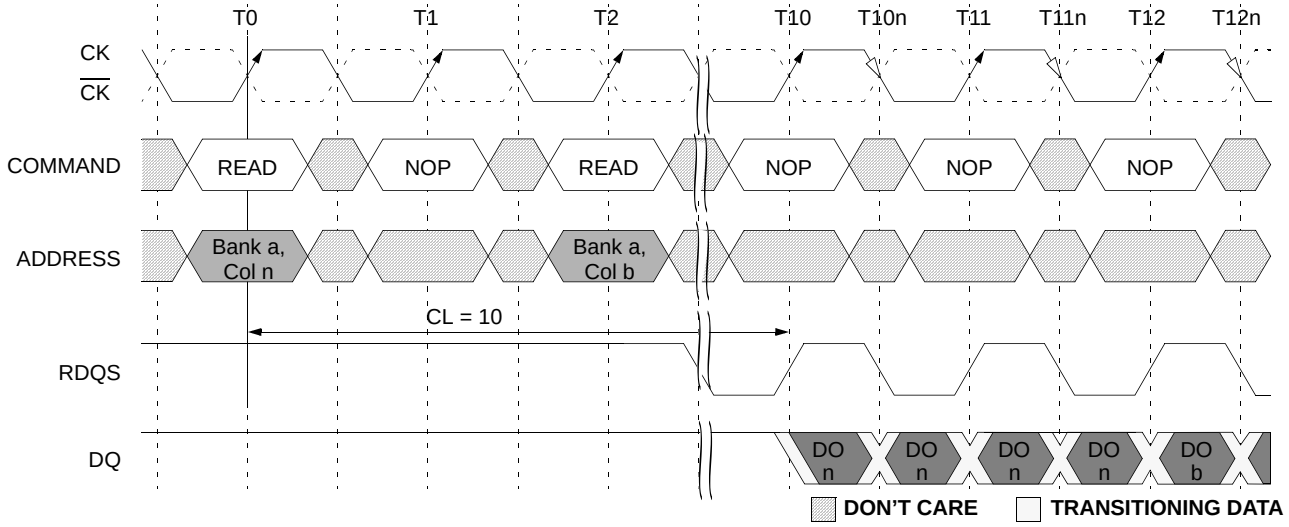
Note : 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Three subsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

Nonconsecutive READ Bursts



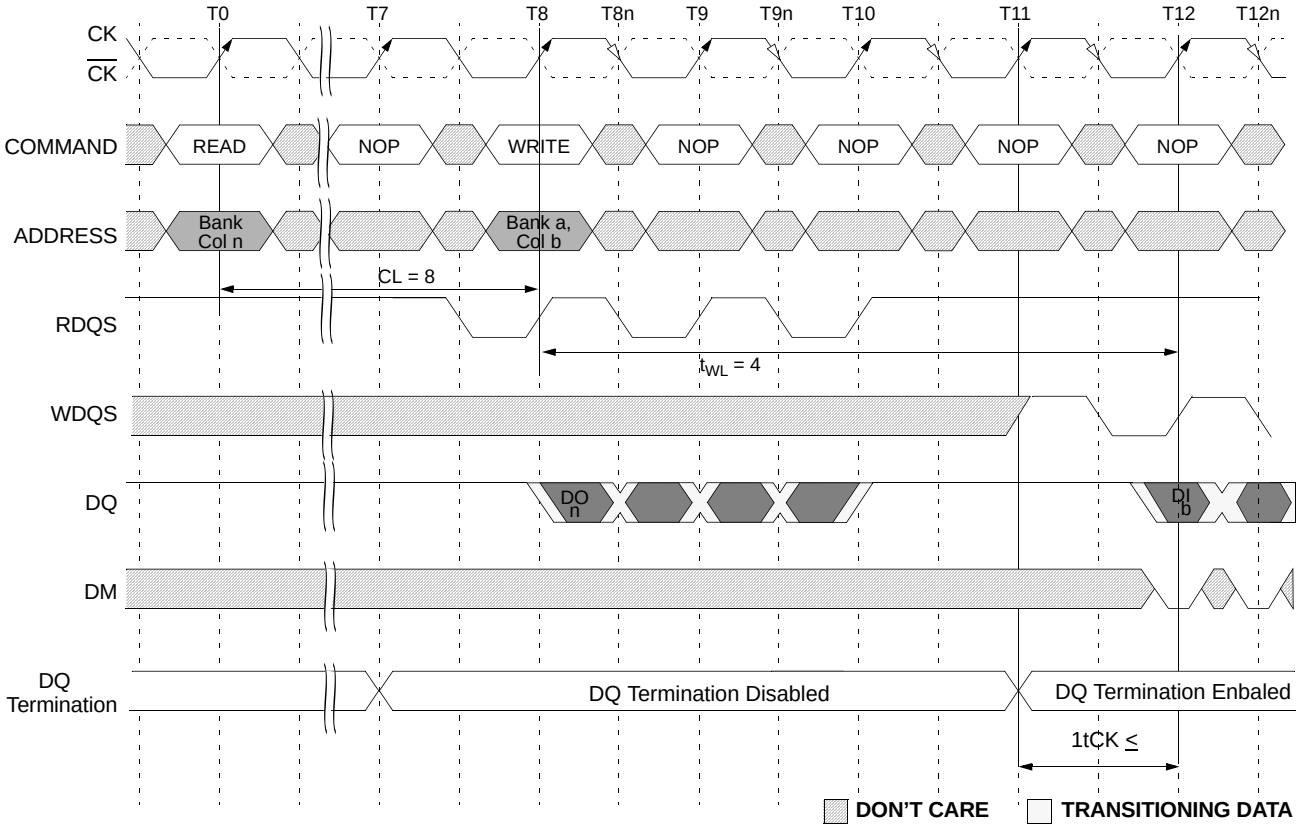
Note :
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Three subsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

Random READ Accesses



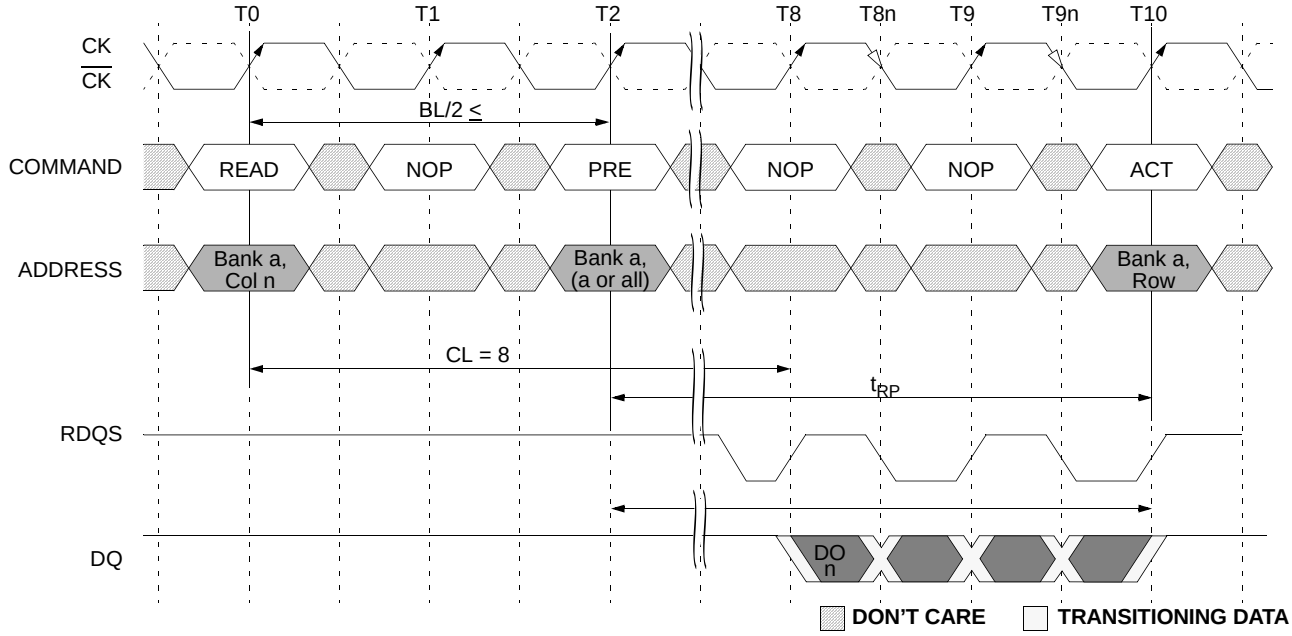
Note :
1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *b* or column *g*).
2. Burst length = 4
3. *n*' or x or *b*' or *g*' indicates the next data-out following DO *n* or DO *x* or DO *b* OR DO *g*, respectively
4. READs are to an active row in any bank.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

READ to WRITE



Note : 1. DO *n* = data-out from column *n*.
2. DI *b* = data-in from column *b*.
3. Burst length = 4
4. One subsequent element of data-out appears in the programmed order following DO *n*.
5. Data-in elements are applied following DI *b* in the programmed order.
6. Shown with nominal t_{AC} and t_{DQSQ}.
7. t_{DQSS} in nominal case.
8. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.
9. The gap between data termination enable to the first data-in should be greater than 1tCK

READ to PRECHARGE



Note : 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DQ *n.*
4. Three subsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.
8. Since GDDR3 is 4n prefetch and no interrupt support, the minimum required time between read and precharge command is equal to BL/2

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

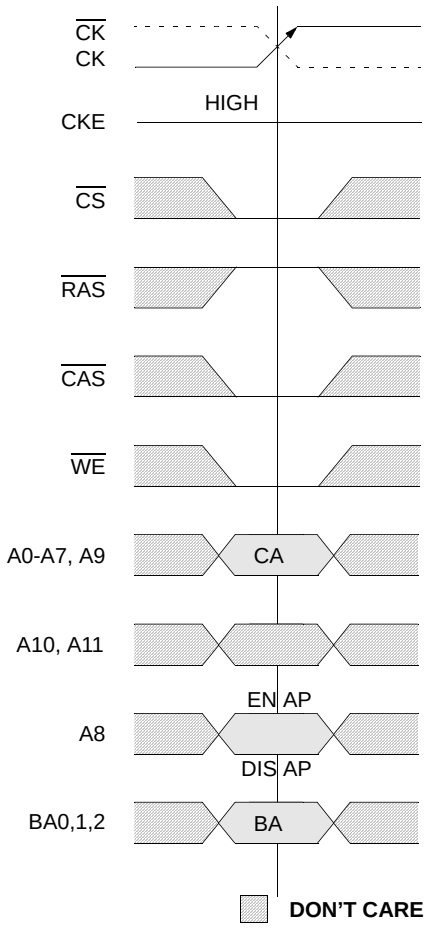
During WRITE bursts, the first valid data-in element will be registered in a rising edge of WDQS following the WRITE latency set in the mode register and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS edge a half cycle is needed and specified as the WRITE Preamble; the half cycle in WDQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first valid falling edge of WDQS (t_{DQSS}) is specified with a relative to the write latency. All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., $t_{DQSS(min)}$ and $t_{DQSS(max)}$) might not be intuitive, they have also been included. Write Burst figure shows the nominal case and the extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command after the burst has completed. The new WRITE command should be issued *x* cycles after the first WRITE command should be equals the number of desired nibbles (nibbles are required by 4n-prefetch architecture).

An example of nonconsecutive WRITEs is shown in Nonconsecutive WRITE to READ figure. Full-speed random write accesses within a page or pages can be performed as shown in Random WRITE cycles figure. Data for any WRITE burst may be followed by a subsequent READ command.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE the WRITE burst, t_{WR} should be met as shown in WRITE to PRECHARGE figure.

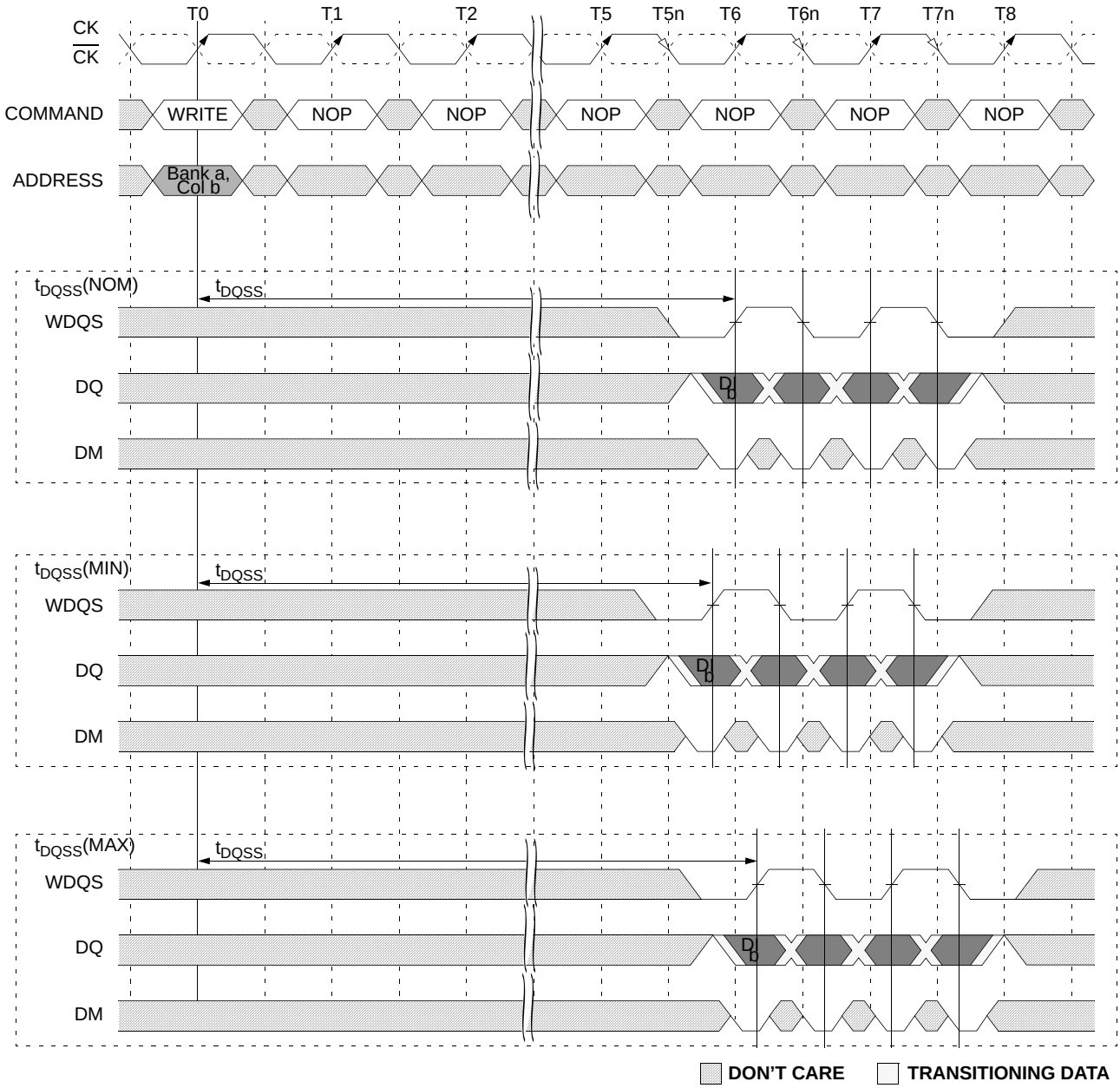
Data for any WRITE burst can not be truncated by a subsequent PRECHARGE command.



CA = Column Address
BA = Bank Address
EN AP = Enable Auto Precharge
DIS AP = Disable Auto Precharge

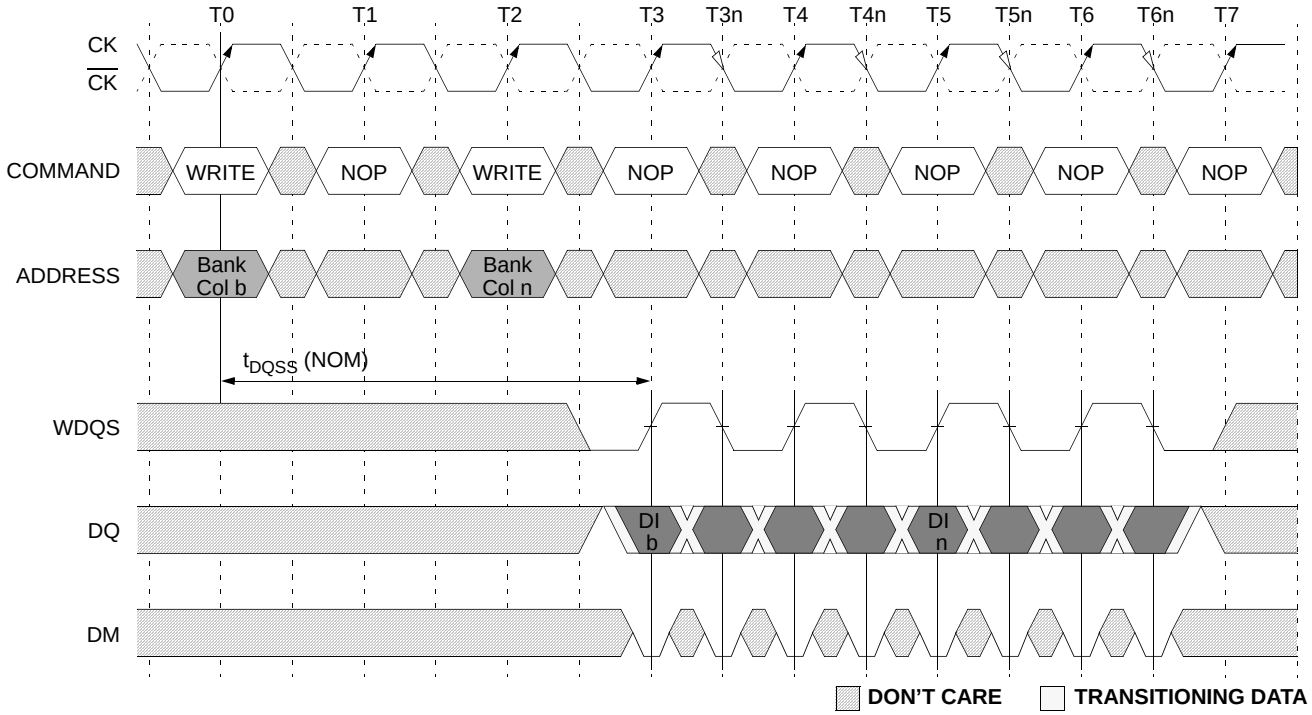
WRITE Command

WRITE Burst



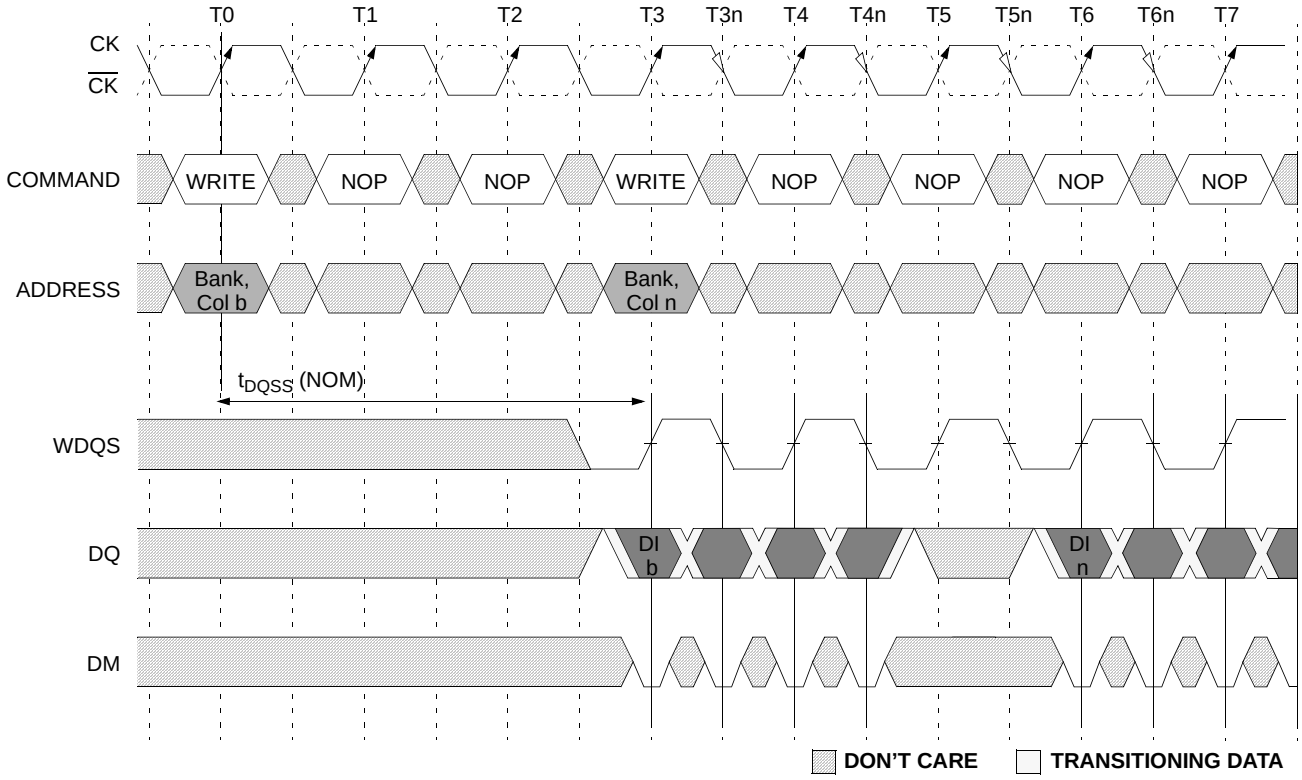
Note : 1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. Write latency is set to 6

Consecutive WRITE to WRITE



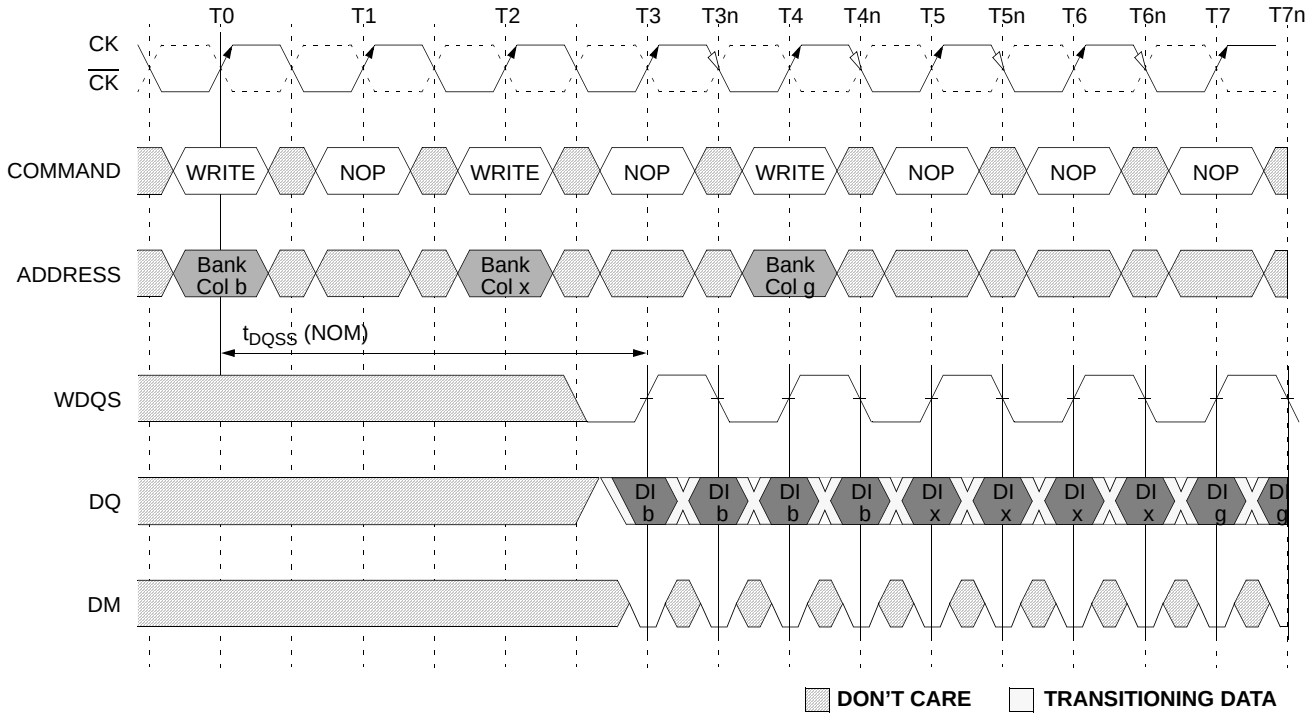
Note : 1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. Burst of 4 is shown.
5. Each WRITE command may be to any bank of the same device.
6. Write latency is set to 3

Nonconsecutive WRITE to WRITE



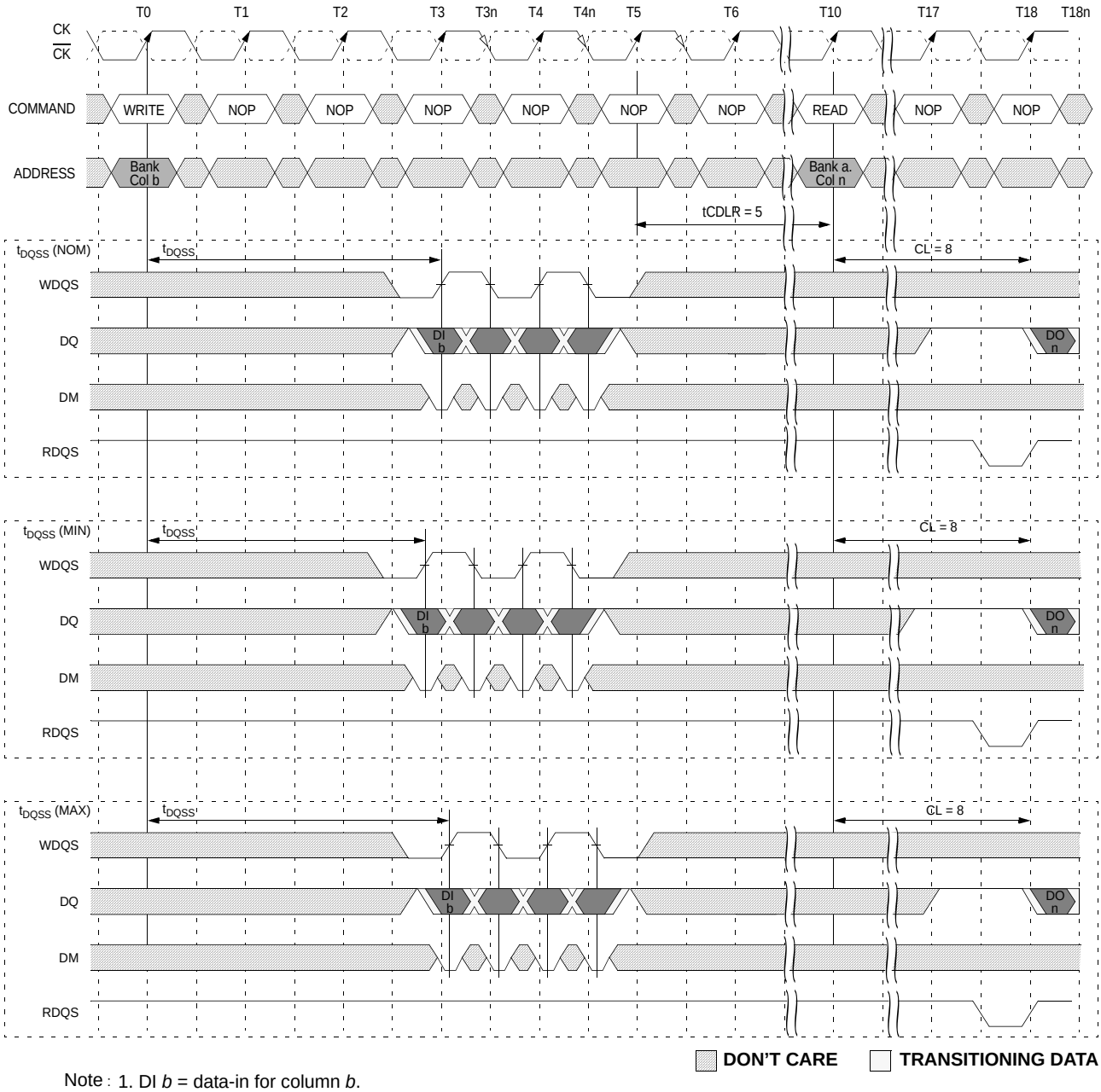
Note : 1. DI b, etc. = data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. burst of 4 is shown.
5. Each WRITE command may be to any bank.
6. Write latency is set to 3

Random WRITE Cycles



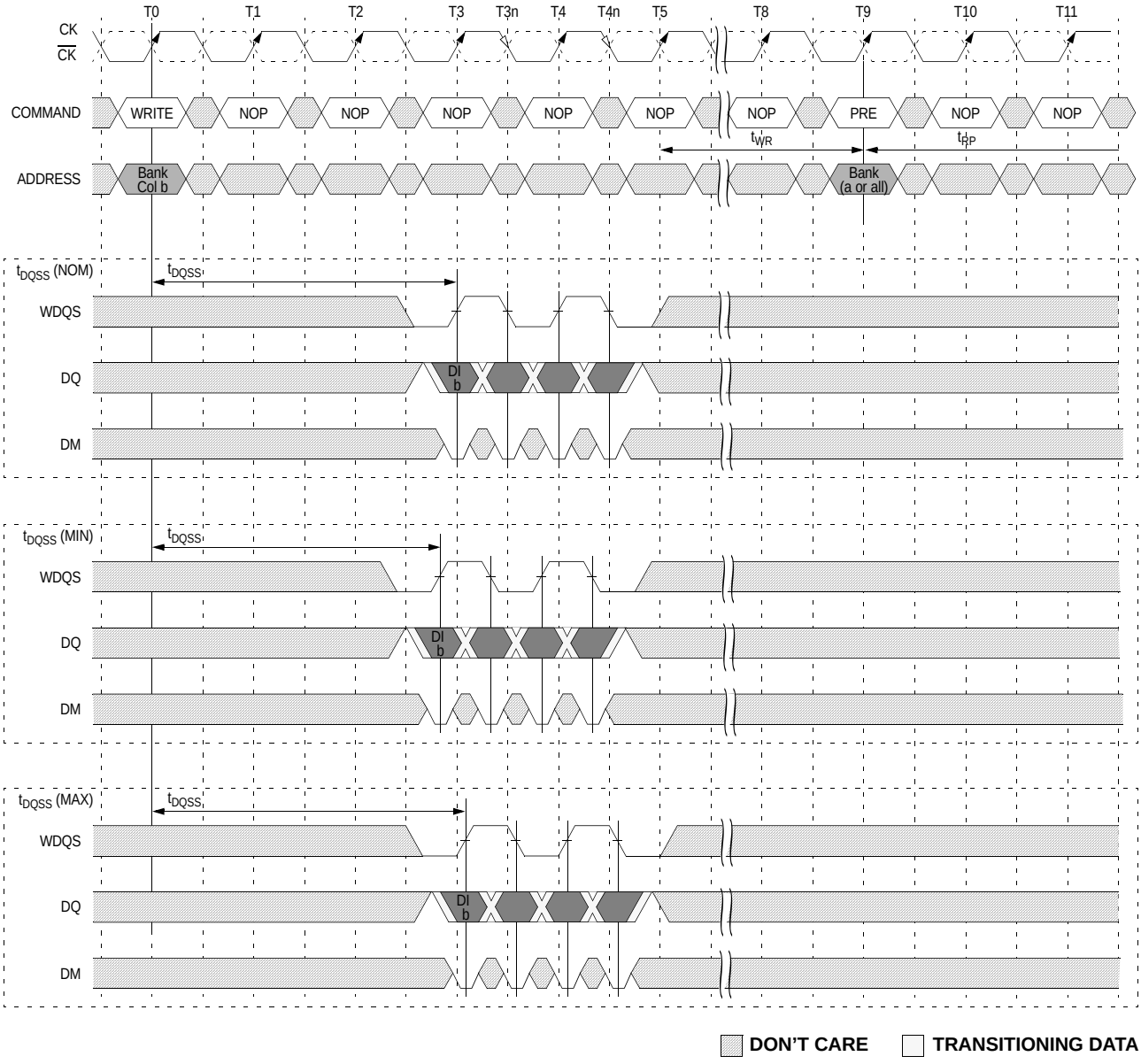
Note : 1. DI b, etc. = data-in for column b, etc.
2. b: etc. = the next data - in following DI b. etc., according to the programmed burst order.
3. Programmed burst length = 4 cases shown.
4. Each WRITE command may be to any bank.
5. Last write command will have the rest of the nibble on T7 and T7n
6. Write latency is set to 3

WRITE to READ



Note : 1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in the programmed order following DI *b*.
3. A burst of 4 is shown.
4. t_{CDLR} is referenced from the first positive CK edge after the last data-in pair.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case t_{CDLR} is not required and the READ command could be applied earlier.
6. A8 is LOW with the WRITE command (auto precharge is disabled).
7. WRITE latency is set to 3

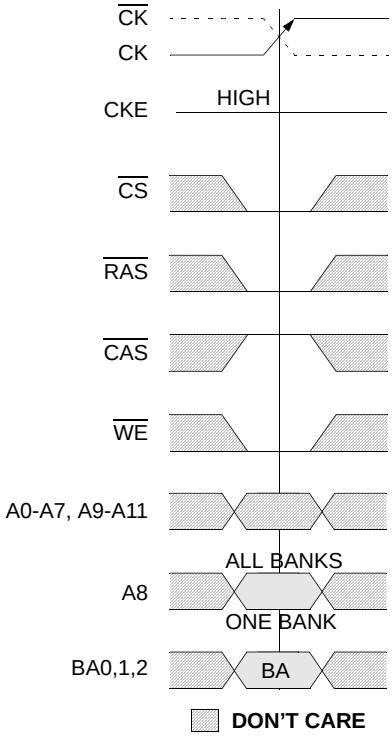
WRITE to PRECHARGE



Note : 1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in the programmed order following DI *b*.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. WRITE latency is set to 3

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1, BA2 select the bank. When all banks are to be precharged, inputs BA0, BA1, BA2 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to the bank.



BA=Bank Address
(if A8 is LOW; otherwise "Don’t Care")

PRECHARGE Command

POWER-DOWN (CKE NOT ACTIVE)

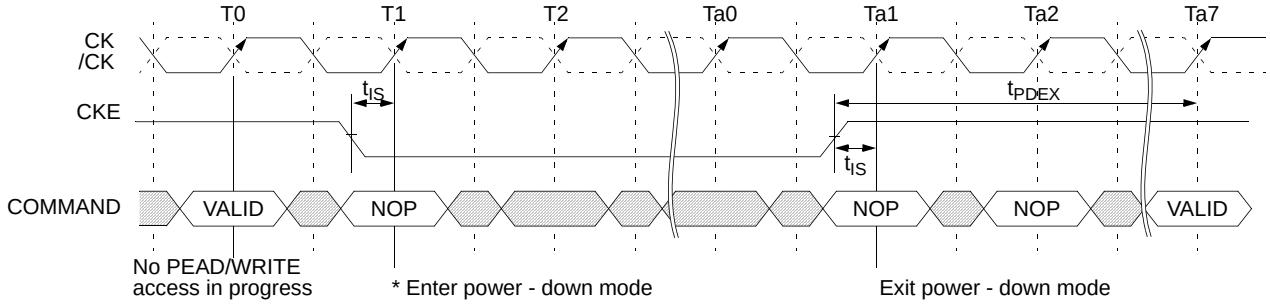
Unlike SDR SDRAMs,GDDR3(x32) SDRAM requires CKE to be active at all times an access is in progress; from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined BL/2 cycles after the Write Postamble is satisfied.

Power-down is entered when CKE is registered LOW. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK,$\overline{CK}$ and CKE. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self-refresh mode is preferred over the DLL-disabled power-down mode.

When in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the GDDR3 SDRAM, while all other input signals are “Don’t Care” except data terminator disable command.

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied tPDEX later.

Power-Down



* Once the device enters the power down mode, it should be in NOP state at least for 10ns. The minimum duration for the power down mode once CKE brought to down should be at least 10ns.

TRUTH TABLE - Clock Enable (CKE)

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	

Note :
1. CKEn is the logic state of CKE at clock edge *n*; CKEn-1was the state of CKE at the previous clock edge.
2. Current state is the state of the GDDR3(x32) immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n*, and ACTION*n* is a result of COMMAND*n*
4. All state and sequence not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XSA} period.

TRUTH TABLE - CURRENT STATE BANK *n* - COMMAND TO BANK *n*

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND/ ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/ continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATOR DISABLE	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
Row Active	L	L	L	L	LOAD MODE REGISTER	7
	L	H	L	H	READ (Select column and start READ burst)	9
	L	H	L	L	WRITE (Select Column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (Auto-Precharge Disable)	L	H	L	H	READ (Select column and start new READ burst)	9
	L	H	L	L	WRITE (Select column and start WRITE burst)	9, 11
	L	L	H	L	PRECHARGE (Only after the READ burst is complete)	8
Write (Auto-Precharge Disabled)	L	H	L	H	READ (Select column and start READ burst)	9, 10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (Only after the WRITE burst is complete)	8, 10

Note :

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see CKE Truth Table) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions :
   - Idle : The bank has been precharged, and t_{RP} has been met.
   - Row Active : A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   - Read : A READ burst has been initiated, with auto precharge disabled.
   - Write : A WRITE burst has been initiated, with auto precharge disabled.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and truth table- current state bank *n* command to bank *n*. and according to truth table - current state bank *n* -command to bank *m.*

   Precharging : Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.

   Row Activating : Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the row active state.

   Read w/ Auto- : Starts with registration of an READ command with auto precharge enabled and ends Precharge Enabled when tRP has been met. Once t_{RP} is met, the bank will be in the idle state.

   Write w/ Auto- : Starts with registration of a WRITE command with auto precharge enabled and ends Precharge Enabled when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command ; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing : Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met.
   Once t_{RC} is met, the GDDR3(x32) will be in the all banks idle state.

   Accessing Mode : Starts with registration of a LOAD MODE REGISTER command and ends when t_{MRD} has been met. Once t_{MRD} is met, the GDDR3(x32) SDRAM will be in the all banks idle state.

   Precharge All : Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met.
   Once t_{RP} is met, all banks will be in the idle state.

   READ or WRITE : Starts with registration of the ACTIVE command and ends the last valid data nibble.

6. All states and sequences not shown are illegal or reserved.

7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.

8. May or may not be bank-specific ; If multiple banks are to be precharged, each must be in a valid state for precharging.

9. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.

10. Requires appropriate DM masking.

11. A WRITE command may be applied after the completion of the READ burst.

TRUTH TABLE - CURRENT STATE BANK n - COMMAND TO BANK m

Function	CKE		$\overline{CS0}$	$\overline{CS1}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A9	A8	A7 - A0	Notes
	Previous Cycle	Current Cycle										
(Extended) Mode Register Set	H	H	L	X	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	X	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	X	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	X	1,6,7
			L	X	H	H	H					
Single Bank Precharge	H	H	H	L	L	H	L	BA	X	L	X	1,2
			L	H								
Precharge all Banks	H	H	H	L	L	H	L	X	X	H	X	1
			L	H								
Bank Activate	H	H	H	L	L	H	H	BA	Row Address			1,2
			L	H								
Write	H	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
			L	H								
Write with Auto Precharge	H	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
			L	H								
Read	H	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
			L	H								
Read with Auto-Precharge	H	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
			L	H								
No Operation	H	X	H	L	H	H	H	X	X	X	X	1
			L	H								
Device Deselect	H	X	H	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	X	1,4
			H	X	H	H	H					
			L	X								
Power Down Exit	L	H	H	X	X	X	X	X	X	X	X	1,4
			H	X	H	H	H					
			L	X								

Note:
1. 1Gbit GDDR3 SGRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register. 2CS mode -> Row Address A0 ~ A11, 1CS mode --> Row address A0 ~ A12.
3. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined
4. “X” means “H or L (but a defined logic level)”.
5. Self refresh exit is asynchronous.
6. VREF must be maintained during Self Refresh operation.
7. CS0 and CS1 are not enabled("Low") simultaneously for 1G GDDR3.

9. Current state definitions :

Idle : The bank has been precharged, and t_{RP} has been met.

Row Active : A row in the bank has been activated, and t_{RCD} has been met.
No data bursts/accesses and no register accesses are in progress.

Read : A READ burst has been initiated, with auto precharge disabled.

Write : A WRITE burst has been initiated, with auto precharge disabled.

Read w/ Auto- Precharge Enabled : See following text

Write w/ Auto- Precharge Enabled : See following text

9a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts : the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related Limitations apply (e.g., contention between read data write data must be avoided).

9b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE w/AP	READ or READ w/AP	[WL + (BL/2)] tCK + tWR
	WRITE or WRITE w/AP	(BL/2) * tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK
READ w/AP	READ or READ w/AP	(BL/2) * tCK
	WRITE or WRITE w/AP	[CL + (BL/2) + 2 - WL] * tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK

10. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.

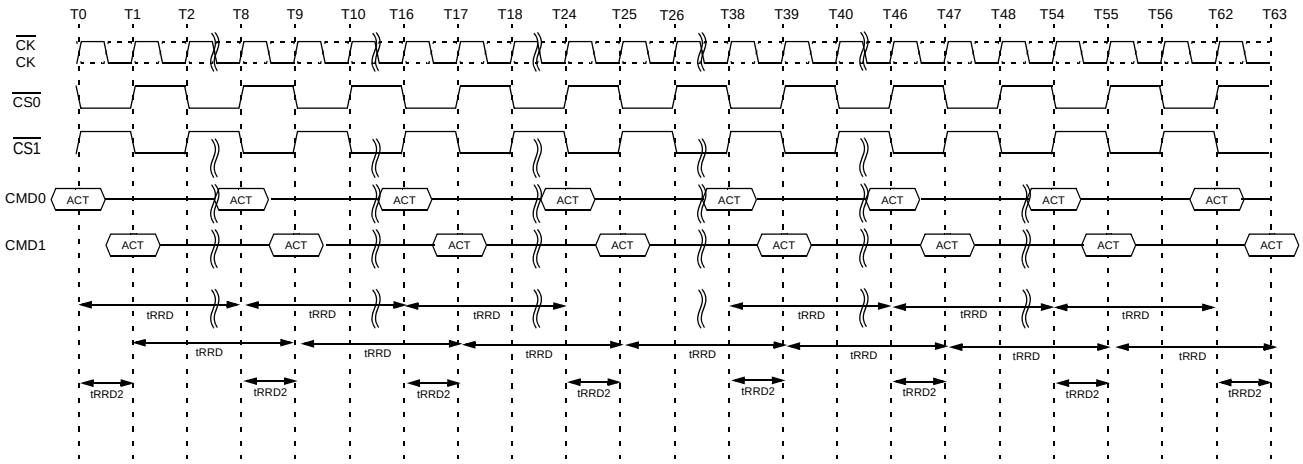
11. All states and sequences not shown are illegal or reserved.

12. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.

13. Requires appropriate DM masking.

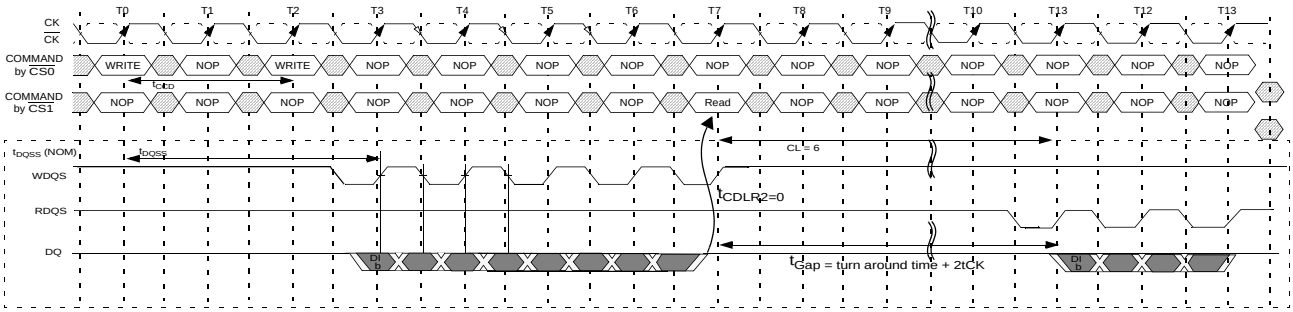
14. 1G GDDR3 timing definition for 2CS mode

Active Command timing



Write to Read timing

1Gb GDDR3 has two kinds of fully independent 8Banks, therefore 1Gb GDDR3 needs to be tCDLR2 which is new parameter to define Last data in to Read command for different rank(2CS mode).



Note : 1.tRRD2 is Row Active to Row Active Delay between two independent 8banks.(2CS mode)
2.tCDLR2 is Last Data In to Read Command Delay between two independent 8banks.(2CS mode)

AC & DC OPERATING CONDITIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-0.5 ~ VDDQ + 0.5V	V
Voltage on VDD supply relative to Vss	VDD	-0.5 ~ 2.5	V
Voltage on VDDQ supply relative to Vss	VDDQ	-0.5 ~ 2.5	V
MAX Junction Temperature	TJ	+125	°C
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	TBD	W
Short Circuit Output Current	IOS	50	mA

Note : Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure periods may affect reliability.

POWER & DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to 0°C ≤ Tc ≤ 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	1.7	1.8	1.9	V	1
Output Supply voltage	V_{DDQ}	1.7	1.8	1.9	V	1
Reference voltage	V_{REF}	0.69*V_{DDQ}	-	0.71*V_{DDQ}	V	2
DC Input logic high voltage	V_{IH} (DC)	V_{REF}+0.15	-	-	V	3
DC Input logic low voltage	V_{IL} (DC)	-	-	V_{REF}-0.15	V	3
Output logic low voltage	V_{OL}(DC)	-	-	0.76	V	
AC Input logic high voltage	V_{IH}(AC)	V_{REF}+0.25	-	-	V	3,4,5
AC Input logic low voltage	V_{IL}(AC)	-	-	V_{REF}-0.25	V	3,4,5
Input leakage current Any input 0V-<V_{IN} -< V_{DDQ} (All other pins not under test = 0V)	II	-5	-	5	uA	
Output leakage current (DQs are disabled; 0V-<V_{OUT} -< V_{DDQ})	IIOZ	-5	-	5	uA	

Note : 1. Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.

2. V_{REF} is expected to equal 70% of V_{DDQ} for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ± 2 percent of the DC value. Thus, from 70% of V_{DDQ}, V_{REF} is allowed ± 25mV for DC error and an additional ±25mV for AC noise.

3. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge and the driver should achieve the same slew rate through the AC values.

4. Input and output slew rate =3V/ns. If the input slew rate is less than 3V/ns, input timing may be compromised. All slew rate are measured between Vih(AC) and Vil(AC).
DQ and DM input slew rate must not deviate from DQS by more than 10%. If the DQ,DM and DQS slew rate is less than 3V/ns, timing is longer than referenced to the mid-point but to the VIL(AC) maximum and VIH(AC) minimum points.

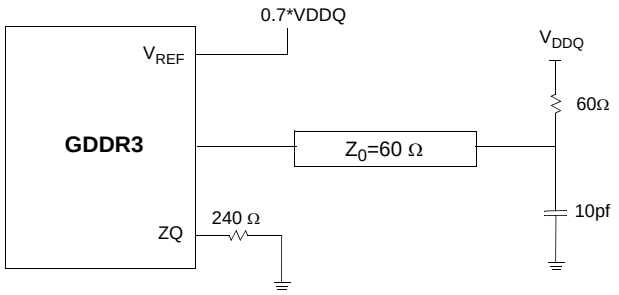
5. VIH overshoot: VIH(max) = VDDQ + 0.5V for a pulse width ≤ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.
VIL undershoot: VIL(min)=0.0V for a pulse width ≤ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.

CLOCK INPUT OPERATING CONDITIONS

Recommended operating conditions (0°C ≤ Tc ≤85°C)

Parameter/ Condition	Symbol	Min	Max	Unit	Note
Clock Input Mid-Point Voltage; CK and $\overline{CK}$	VMP(DC)	VDDQ*0.7-0.1V	VDDQ*0.7+0.1V	V	1,2,3
Clock Input Voltage Level; CK and $\overline{CK}$	VIN(DC)	0.42	VDDQ + 0.3	V	2
Clock Input Differential Voltage; CK and $\overline{CK}$	VID(DC)	0.22	VDDQ + 0.5	V	2,4
Clock Input Differential Voltage; CK and $\overline{CK}$	VID(AC)	0.22	VDDQ + 0.3	V	4
Clock Input Crossing Point Voltage; CK and $\overline{CK}$	VIX(AC)	VREF - 0.15	VREF + 0.15	V	3

Note: 1. This provides a minimum of 1.16V to a maximum of 1.36V for -HC part and 1.19V ~ 1.39V for -HJ part , and is always 70% of VDDQ
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of VIX is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
4. VID is the magnitude of the difference between the input level in CK and the input level on $\overline{CK}$.
5. The CK and $\overline{CK}$ input reference level (for timing referenced to CK and /CK) is the point at which CK and $\overline{CK}$ cross; the input reference level for signals other than CK and $\overline{CK}$ is VREF.
6. CK and $\overline{CK}$ input slew rate must be ≥ 3V/ns



Output Load Circuit

Note: 1. Outputs measured into equivalent load of 10pf at a driver impedance of 40 Ω.

CAPACITANCE (VDD=1.8V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK, $\overline{CK}$)	CIN1	1.0	2.5	pF
Input capacitance (A0~A11, BA0~BA2)	CIN2	1.0	2.5	pF
Input capacitance(CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN3	1.0	2.5	pF
Data & DQS input/output capacitance(DQ0~DQ31)	COUT	1.5	3.0	pF
Input capacitance(DM0 ~ DM3)	CIN4	1.5	3.0	pF

Thermal Characteristics(2.6/2.4/2.0/1.6/1.4Gbps at VDD=1.8V ± 0.1V, VDDQ=1.8V ± 0.1V)

Parameter	Description	Value	Units	Note
Theta_JA	Thermal resistance junction to ambient	27.9	°C/W	Thermal measurement : 1,2,3,5
Max_Tj	Maximum operating junction temperature	46.3. 47.9 51.3 54.6 56.3	°C	1.4Gbps@Max 1.9V(Pd =0.765W) 1.6Gbps@Max 1.9V(Pd =0.820W) 2.0Gbps@Max 1.9V(Pd =0.942W) 2.4Gbps@Max 1.9V(Pd =1.060W) 2.6Gbps@Max 1.9V(Pd =1.120W)
Max_Tc	Maximum operating case temperature	42.6 43.9 46.7 49.4 50.8	°C	1.4Gbps@Max 1.9V 1.6Gbps@Max 1.9V 2.0Gbps@Max 1.9V 2.4Gbps@Max 1.9V 2.6Gbps@Max 1.9V
Theta_Jc	Thermal resistance junction to case	4.88	°C/W	Thermal measurement : 1, 6
Theta_JB	Thermal resistance junction to board	17.40	°C/W	Thermal simulation : 1, 2, 6

Note 1.Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be documented for Theta JA.
4. Max_Tj and Max_Tc are documented for normal operation in this table. These are not intended to reflect reliablility limits.
5. Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction.
6. Theta_JB and Theta_JC are derived through a package thermal simulation and measurement.

DC CHARACTERISTICS-I

(0°C ≤ Tc ≤85°C ; VDD=1.8V ± 0.1V, VDDQ=1.8V ± 0.1V)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-HC7A		
Operating Current (One Bank Active)	ICC1	Burst Length=4 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	400	mA	1
Precharge Standby Current in Power-down mode	ICC2P	CKE ≤ VIL(max), tCC= tCC(min)	110	mA	1,3
Precharge Standby Current in Non Power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tCC= tCC(min)	190	mA	1,3
Active Standby Current power-down mode	ICC3P	CKE ≤ VIL(max), tCC= tCC(min)	145	mA	1,3
Active Standby Current in in Non Power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥VIH(min), tCC= tCC(min)	330	mA	1,3
Operating Current (Burst Mode)	ICC4	IOL=0mA ,tCC= tCC(min), Page Burst, All Banks activated.	700	mA	1
Refresh Current	ICC5	tRC≥ tRFC	450	mA	1,2
Self Refresh Current	ICC6	CKE ≤ 0.2V	40	mA	1
Operating Current (4Bank interleaving)	ICC7	Burst Length=4 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	800	mA	1

DC CHARACTERISTICS-II

(0°C ≤ Tc ≤85°C ; VDD=1.8V ± 0.1V, VDDQ=1.8V ± 0.1V)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-HC08	-HC1A		
Operating Current (One Bank Active)	ICC1	Burst Length=4 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	380	360	mA	1
Precharge Standby Current in Power-down mode	ICC2P	CKE ≤ VIL(max), tCC= tCC(min)	105	100	mA	1,3
Precharge Standby Current in Non Power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tCC= tCC(min)	180	160	mA	1,3
Active Standby Current power-down mode	ICC3P	CKE ≤ VIL(max), tCC= tCC(min)	140	135	mA	1,3
Active Standby Current in in Non Power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥VIH(min), tCC= tCC(min)	320	300	mA	1,3
Operating Current (Burst Mode)	ICC4	IOL=0mA ,tCC= tCC(min), Page Burst, All Banks activated.	670	620	mA	1
Refresh Current	ICC5	tRC≥ tRFC	440	400	mA	1,2
Self Refresh Current	ICC6	CKE ≤ 0.2V	40	40	mA	1
Operating Current (4Bank interleaving)	ICC7	Burst Length=4 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	760	700	mA	1

Note 1.Measured with outputs open and ODT off
2. Refresh period is 32ms
3. VIH(AC) and VIL(AC)

DC CHARACTERISTICS-III

(0°C ≤ Tc ≤85°C ; VDD=1.8V ± 0.1V, VDDQ=1.8V ± 0.1V)

Parameter	Symbol	Test Condition	Version		Unit	Note
			-HC12	-HC14		
Operating Current (One Bank Active)	ICC1	Burst Length=4 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	340	320	mA	1
Precharge Standby Current in Power-down mode	ICC2P	CKE ≤ VIL(max), tCC= tCC(min)	95	90	mA	1,3
Precharge Standby Current in Non Power-down mode	ICC2N	CKE ≥ VIH(min), CS ≥ VIH(min), tCC= tCC(min)	140	130	mA	1,3
Active Standby Current power-down mode	ICC3P	CKE ≤ VIL(max), tCC= tCC(min)	125	120	mA	1,3
Active Standby Current in in Non Power-down mode	ICC3N	CKE ≥ VIH(min), CS ≥VIH(min), tCC= tCC(min)	260	250	mA	1,3
Operating Current (Burst Mode)	ICC4	IOL=0mA ,tCC= tCC(min), Page Burst, All Banks activated.	540	520	mA	1
Refresh Current	ICC5	tRC≥ tRFC	360	330	mA	1,2
Self Refresh Current	ICC6	CKE ≤ 0.2V	40	40	mA	1
Operating Current (4Bank interleaving)	ICC7	Burst Length=4 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	620	580	mA	1

Note 1.Measured with outputs open and ODT off
2. Refresh period is 32ms
3. VIH(AC) and VIL(AC)

AC CHARACTERISTICS I-I

Parameter		Symbol	-HC7A		Unit	Note
			Min	Max		
DQS out access time from CK		tDQSCK	-0.18	0.18	ns	
CK high-level width		tCH	0.45	0.55	tCK	
CK low-level width		tCL	0.45	0.55	tCK	
CK cycle time	CL=15	tCK	0.77	3.3	ns	
	CL=14		0.83		ns	
	CL=12		1.0		ns	
	CL=11		1.25		ns	
	CL=10		1.4		ns	
WRITE Latency		tWL	1~7	-	tCK	1
DQ and DM input hold time relative to DQS		tDH	0.11	-	ns	
DQ and DM input setup time relative to DQS		tDS	0.11	-	ns	
Active termination setup time		tATS	10	-	ns	
Active termination hold time		tATH	10	-	ns	
DQS input high pulse width		tDQSH	0.48	0.52	tCK	
DQS input low pulse widthl		tDQSL	0.48	0.52	tCK	
Data strobe edge to Dout edge		tDQSQ	-0.10	0.10	ns	
DQS read preamble		tRPRE	0.4	0.6	tCK	
DQS read postamble		tRPST	0.4	0.6	tCK	
Write command to first DQS latching transition		tDQSS	WL-0.2	WL+0.2	tCK	
DQS write preamble		tWPRE	0.4	0.6	tCK	2
DQS write preamble setup time		tWPRES	0	-	ns	
DQS write postamble		tWPST	0.4	0.6	tCK	3
Half strobe period		tHP	tCLmin or tCHmin	-	tCK	
Data output hold time from DQS		tQH	t_{HP}-0.10	-	ns	
Data-out high-impedance window from CK and $\overline{CK}$		tHZ	-0.3	-	ns	4
Data-out low-impedance window from CK and $\overline{CK}$		tLZ	-0.3	-	ns	4
Address and control input hold time		tIH	0.23	-	ns	
Address and control input setup time		tIS	0.23	-	ns	
Address and control input pulse width		tIPW	0.60	-	ns	
Jitter over 1~6 clock cycle error		tJ	-	0.03	tCK	5
Cycle to cycle duty cycle error		tDCERR	-	0.03	tCK	
Rise and fall times of CK		tR, tF	-	0.2	tCK	

Note : 1. The WRITE latency can be set from 1 to 7 clocks.
2. A low to high transition on the WDQS line is not allowed in the half clock prior to the write preamble.
3. The last rising edge of WDQS after the write postamble must be driven high by the controller. WDQS can not be pulled high by the on-die termination alone.
4. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
5. The cycle to cycle jitter over 1~6 cycle short term jitter

AC CHARACTERISTICS I-II

Parameter		Symbol	-HC08		-HC1A		Unit	Note
			Min	Max	Min	Max		
DQS out access time from CK		tDQSCK	-0.19	+0.19	-0.20	+0.20	ns	
CK high-level width		tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width		tCL	0.45	0.55	0.45	0.55	tCK	
CK cycle time	CL=14	tCK	0.83	3.3	-	3.3	ns	
	CL=12		1.0		1.0		ns	
	CL=11		1.25		1.1/1.25		ns	
	CL=10		1.4		1.4		ns	
WRITE Latency		tWL	1~7	-	1~7	-	tCK	1
DQ and DM input hold time relative to DQS		tDH	0.12	-	0.13	-	ns	
DQ and DM input setup time relative to DQS		tDS	0.12	-	0.13	-	ns	
Active termination setup time		tATS	10	-	10	-	ns	
Active termination hold time		tATH	10	-	10	-	ns	
DQS input high pulse width		tDQSH	0.48	0.52	0.48	0.52	tCK	
DQS input low pulse widthl		tDQSL	0.48	0.52	0.48	0.52	tCK	
Data strobe edge to Dout edge		tDQSQ	-0.11	0.11	-0.13	0.13	ns	
DQS read preamble		tRPRE	0.4	0.6	0.4	0.6	tCK	
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
Write command to first DQS latching transition		tDQSS	WL-0.2	WL+0.2	WL-0.2	WL+0.2	tCK	
DQS write preamble		tWPRE	0.4	0.6	0.4	0.6	tCK	2
DQS write preamble setup time		tWPRES	0	-	0	-	ns	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	3
Half strobe period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCK	
Data output hold time from DQS		tQH	t_{HP}-0.11	-	t_{HP}-0.12	-	ns	
Data-out high-impedance window from CK and $\overline{CK}$		tHZ	-0.3	-	-0.3	-	ns	4
Data-out low-impedance window from CK and $\overline{CK}$		tLZ	-0.3	-	-0.3	-	ns	4
Address and control input hold time		tIH	0.24	-	0.27	-	ns	
Address and control input setup time		tIS	0.24	-	0.27	-	ns	
Address and control input pulse width		tIPW	0.65	-	0.8	-	ns	
Jitter over 1~6 clock cycle error		tJ	-	0.03	-	0.03	tCK	5
Cycle to cycle duty cycle error		tDCERR	-	0.03	-	0.03	tCK	
Rise and fall times of CK		tR, tF	-	0.2	-	0.2	tCK	

Note : 1. The WRITE latency can be set from 1 to 7 clocks.
2. A low to high transition on the WDQS line is not allowed in the half clock prior to the write preamble.
3. The last rising edge of WDQS after the write postamble must be driven high by the controller. WDQS can not be pulled high by the on-die termination alone.
4. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
5. The cycle to cycle jitter over 1~6 cycle short term jitter

AC CHARACTERISTICS I-III

Parameter		Symbol	-HC12		-HC14		Unit	Note
			Min	Max	Min	Max		
DQS out access time from CK		tDQSCK	-0.23	+0.23	-0.26	+0.26	ns	
CK high-level width		tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width		tCL	0.45	0.55	0.45	0.55	tCK	
CK cycle time	CL=11	tCK	1.25	3.3	-	3.3	ns	
	CL=10		1.4		1.4		ns	
WRITE Latency		tWL	1~7	-	1~7	-	tCK	1
DQ and DM input hold time relative to DQS		tDH	0.16	-	0.18	-	ns	
DQ and DM input setup time relative to DQS		tDS	0.16	-	0.18	-	ns	
Active termination setup time		tATS	10	-	10	-	ns	
Active termination hold time		tATH	10	-	10	-	ns	
DQS input high pulse width		tDQSH	0.48	0.52	0.48	0.52	tCK	
DQS input low pulse widthl		tDQSL	0.48	0.52	0.48	0.52	tCK	
Data strobe edge to Dout edge		tDQSQ	-0.140	0.140	-0.160	0.160	ns	
DQS read preamble		tRPRE	0.4	0.6	0.4	0.6	tCK	
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
Write command to first DQS latching transition		tDQSS	WL-0.2	WL+0.2	WL-0.2	WL+0.2	tCK	
DQS write preamble		tWPRE	0.35	-	0.4	0.6	tCK	2
DQS write preamble setup time		tWPRES	0	-	0	-	ns	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	3
Half strobe period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCK	
Data output hold time from DQS		tQH	t_{HP}-0.14	-	t_{HP}-0.16	-	ns	
Data-out high-impedance window from CK and $\overline{CK}$		tHZ	-0.3	-	-0.3	-	ns	4
Data-out low-impedance window from CK and $\overline{CK}$		tLZ	-0.3	-	-0.3	-	ns	4
Address and control input hold time		tIH	0.3	-	0.35	-	ns	
Address and control input setup time		tIS	0.3	-	0.35	-	ns	
Address and control input pulse width		tIPW	0.9	-	1.0	-	ns	
Jitter over 1~6 clock cycle error		tJ	-	0.03	-	0.03	tCK	5
Cycle to cycle duty cycle error		tDCERR	-	0.03	-	0.03	tCK	
Rise and fall times of CK		tR, tF	-	0.2	-	0.2	tCK	

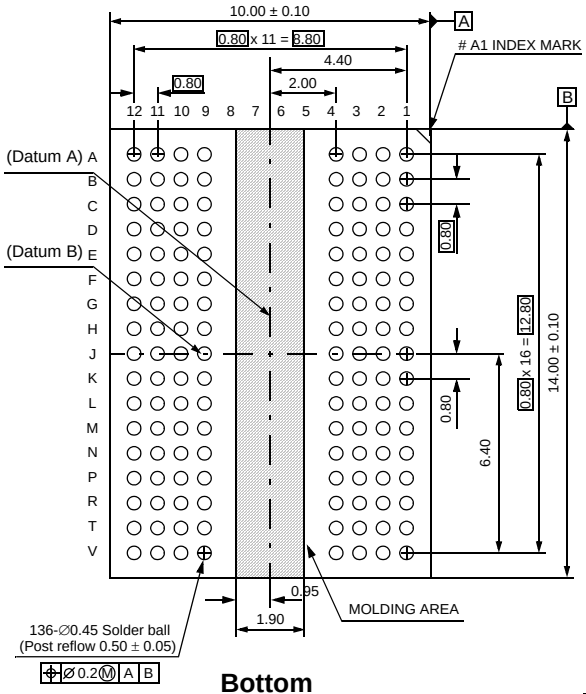
Note : 1. The WRITE latency can be set from 1 to 7 clocks.
2. A low to high transition on the WDQS line is not allowed in the half clock prior to the write preamble.
3. The last rising edge of WDQS after the write postamble must be driven high by the controller. WDQS can not be pulled high by the on-die termination alone.
4. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
5. The cycle to cycle jitter over 1~6 cycle short term jitter

AC CHARACTERISTICS II

Parameter	Symbol	-HC7A		-HC08		-HC1A		-HC12		-HC14		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row active time	tRAS	36	100K	34	100K	29	100K	25	100K	22	100K	tCK	
Row cycle time	tRC	51	-	48	-	41	-	35	-	31	-	tCK	
Refresh row cycle time	tRFC	66	-	62	-	52	-	45	-	39	-	tCK	
RAS to CAS delay for Read	tRCDR	17	-	16	-	14	-	12	-	10	-	tCK	
RAS to CAS delay for Write	tRCDW	13	-	12	-	10	-	8	-	6	-	tCK	
Row precharge time	tRP	15	-	14	-	12	-	10	-	9	-	tCK	
Row active to Row active	tRRD	13	-	12	-	10	-	8	-	8	-	tCK	
Row active to Row active for 2CS mode	tRRD2	1	-	1	-	1	-	1	-	1	-	tCK	1
Last data in to Row precharge (PRE or Auto-PRE)	tWR	15	-	15	-	13	-	11	-	10	-	tCK	
Last data in to Read command	tCDLR	8	-	8	-	7	-	6	-	5	-	tCK	
Last data in to Read command for 2CS mode	tCDLR2	BL/2-2	-	BL/2-2	-	BL/2-2	-	BL/2-2	-	BL/2-2	-	tCK	1
CAS to CAS command delay	tCCD	BL/2	-	BL/2	-	BL/2	-	BL/2	-	BL/2	-	tCK	
Mode register set cycle time	tMRD	10	-	10	-	9	-	7	-	6	-	tCK	
Auto precharge write recovery time + Precharge	tDAL	30	-	29	-	25	-	21	-	19	-	tCK	
Exit self refresh to Read command	tXSR	20000	-	20000	-	20000	-	20000	-	20000	-	tCK	
Exit self refresh to Non-Read command	tXSNR	100	-	100	-	100	-	100	-	100	-	tCK	
Power-down exit time	tPDEX	10tCK +tIS	-	10tCK +tIS	-	8tCK +tIS	-	7tCK +tIS	-	6tCK +tIS	-	tCK	
Refresh interval time	tREF	-	3.9	-	3.9	-	3.9	-	3.9	-	3.9	us	
CKE minimum pulse width (High and Low pulse width)	tCKE	5	-	5	-	5	-	5	-	5	-	tCK	

Note 1 : t_{RRD2} and t_{CDLR2} are only specification for 2CS mode.(between different Rank)

PACKAGE DIMENSIONS (FBGA)



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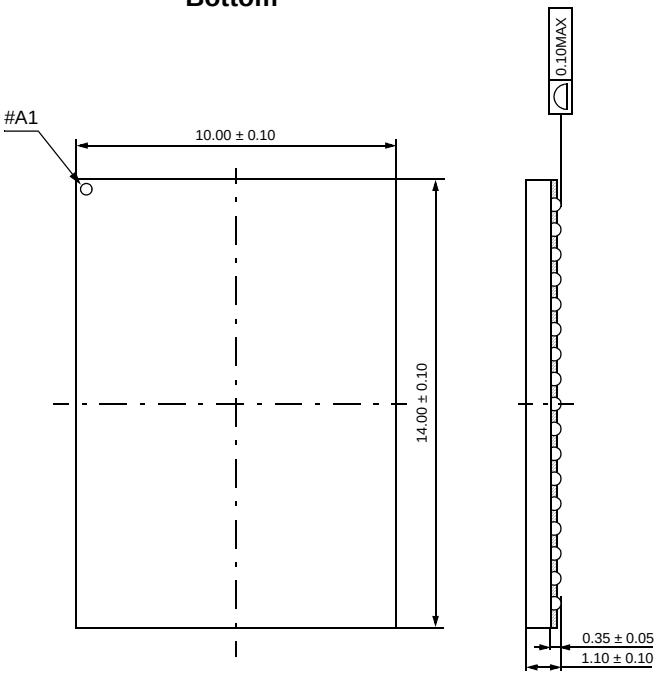

Top

Unit: mm