# *Stacked 512Mbit SDRAM*

32M x 4bit x 4 Banks
Synchronous DRAM
LVTTL

Revision 0.0

Apr. 2002

**Revision History**

**Revision 0.0 (Apr., 2002)**

## *32M x 4Bit x 4 Banks Synchronous DRAM*

### FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)

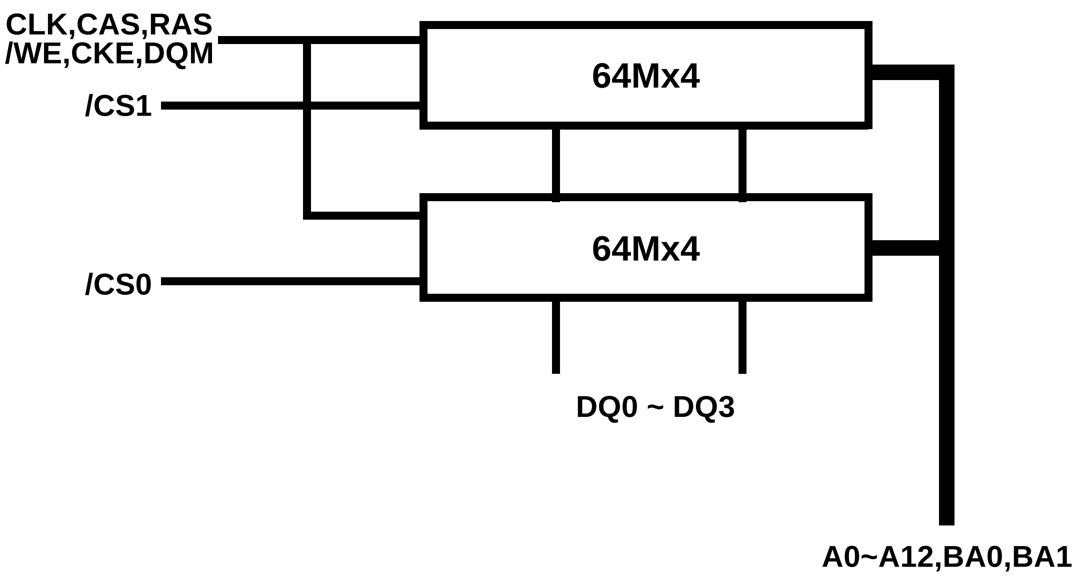
### GENERAL DESCRIPTION

The K4S510632D is 536,870,912 bits synchronous high data rate Dynamic RAM organized as 4 x 33,554,432 words by 4 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

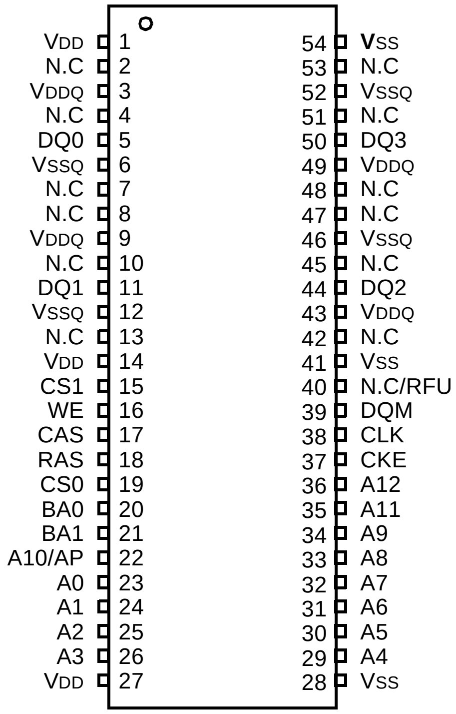
### ORDERING INFORMATION

| Part No. | Max Freq. | Interface | Package |
|---|---|---|---|
| K4S510632D-TC/L7C | 133MHz(CL=2) | LVTTL | 54pin TSOP(II) |
| K4S510632D-TC/L75 | 133MHz(CL=3) | | |
| K4S510632D-TC/L1H | 100MHz(CL=2) | | |
| K4S510632D-TC/L1L | 100MHz(CL=3) | | |

### FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION (Top view)




54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

## PIN FUNCTION DESCRIPTION

| Pin | Name | Input Function |
|---|---|---|
| CLK | System clock | Active on the positive going edge to sample all inputs. |
| CS0~1 | Chip select | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM |
| CKE | Clock enable | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. |
| $A_0$ ~ $A_{12}$ | Address | Row/column addresses are multiplexed on the same pins. Row address : $RA_0$ ~ $RA_{12}$, Column address : $CA_0$ ~ $CA_9$, $CA_{11}$ |
| $BA_0$ ~ $BA_1$ | Bank select address | Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time. |
| RAS | Row address strobe | Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge. |
| CAS | Column address strobe | Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access. |
| WE | Write enable | Enables write operation and row precharge. Latches data in starting from CAS, WE active. |
| DQM | Data input/output mask | Makes data output Hi-Z, $t_{SHZ}$ after the clock and masks the output. Blocks data input when DQM active. |
| $DQ_{0 \sim 3}$ | Data input/output | Data inputs/outputs are multiplexed on the same pins. |
| $V_{DD}/V_{SS}$ | Power supply/ground | Power and ground for the input buffers and the core logic. |
| $V_{DDQ}/V_{SSQ}$ | Data output power/ground | Isolated power supply and ground for the output buffers to provide improved noise immunity. |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -1.0 ~ 4.6 | V |
| Voltage on $V_{DD}$ supply relative to Vss | $V_{DD}$, $V_{DDQ}$ | -1.0 ~ 4.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power dissipation | $P_D$ | 2 | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to $V_{SS}$ = 0V, $T_A$ = 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$, $V_{DDQ}$ | 3.0 | 3.3 | 3.6 | V | |
| Input logic high voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{DD}$+0.3 | V | 1 |
| Input logic low voltage | $V_{IL}$ | -0.3 | 0 | 0.8 | V | 2 |
| Output logic high voltage | $V_{OH}$ | 2.4 | - | - | V | $I_{OH}$ = -2mA |
| Output logic low voltage | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 2mA |
| Input leakage current | $I_{LI}$ | -10 | - | 10 | uA | 3 |

Notes :
1. $V_{IH}$ (max) = 5.6V AC. The overshoot voltage duration is $\leq$ 3ns.
2. $V_{IL}$ (min) = -2.0V AC. The undershoot voltage duration is $\leq$ 3ns.
3. Any input 0V $\leq V_{IN} \leq V_{DDQ}$.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF =1.4V ± 200 mV)

| Pin | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Clock | $C_{CLK}$ | 5.0 | 9.0 | pF | |
| RAS, CAS, WE, DQM | $C_{IN}$ | 5.0 | 10.0 | pF | |
| Address,CKE | $C_{ADD}$ | 5.0 | 10.0 | pF | |
| CS0~1 | $C_{CS}$ | 2.5 | 6.5 | pF | |
| $DQ_0$ ~ $DQ_8$ | $C_{OUT}$ | 8.0 | 14.0 | pF | |

## DC CHARACTERISTICS

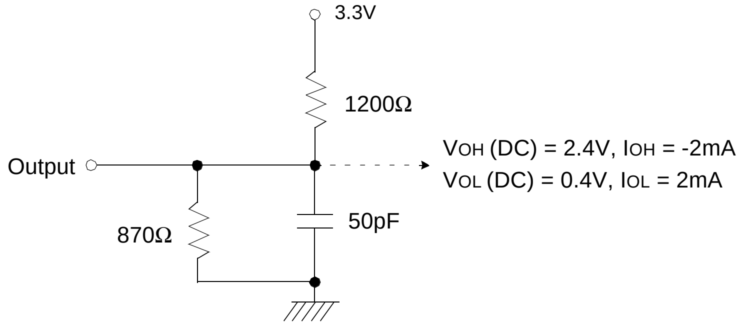
(Recommended operating condition unless otherwise noted, $T_A$ = 0 to 70°C)

| Parameter | Symbol | Test Condition | Version -7C | Version -75 | Version -1H | Version -1L | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Operating current (One bank active) | $I_{CC1}$ | Burst length = 1<br>$t_{RC} \geq t_{RC}$(min)<br>$I_O$ = 0 mA | 120 | 110 | 110 | 110 | mA | 1 |
| Precharge standby current in power-down mode | $I_{CC2}P$ | CKE $\leq V_{IL}$(max), $t_{CC}$ = 10ns | 4 | | | | mA | |
| | $I_{CC2}PS$ | CKE & CLK $\leq V_{IL}$(max), $t_{CC}$ = $\infty$ | 4 | | | | | |
| Precharge standby current in non power-down mode | $I_{CC2}N$ | CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), $t_{CC}$ = 10ns<br>Input signals are changed one time during 20ns | 40 | | | | mA | |
| | $I_{CC2}NS$ | CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC}$ = $\infty$<br>Input signals are stable | 20 | | | | | |
| Active Standby current in power-down mode | $I_{CC3}P$ | CKE $\leq V_{IL}$(max), $t_{CC}$ = 10ns | 8 | | | | mA | |
| | $I_{CC3}PS$ | CKE & CLK $\leq V_{IL}$(max), $t_{CC}$ = $\infty$ | 8 | | | | | |
| Active standby current in non power-down mode (One bank active) | $I_{CC3}N$ | CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), $t_{CC}$ = 10ns<br>Input signals are changed one time during 20ns | 50 | | | | mA | |
| | $I_{CC3}NS$ | CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC}$ = $\infty$<br>Input signals are stable | 35 | | | | mA | |
| Operating current (Burst mode) | $I_{CC4}$ | $I_O$ = 0 mA<br>Page burst<br>4banks activated.<br>$t_{CCD}$ = 2CLKs | 140 | 140 | 130 | 130 | mA | 1 |
| Refresh current | $I_{CC5}$ | $t_{RC} \geq t_{RC}$(min) | 240 | 220 | 210 | 210 | mA | 2 |
| Self refresh current | $I_{CC6}$ | CKE $\leq$ 0.2V — C | 6 | | | | mA | 3 |
| | | CKE $\leq$ 0.2V — L | 3 | | | | mA | 4 |

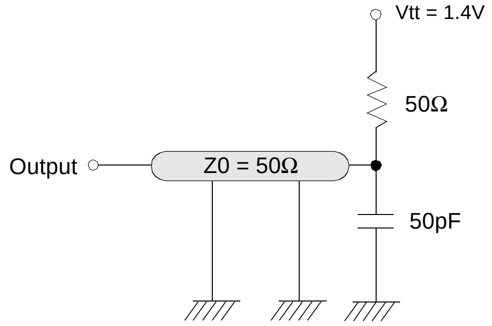
**Notes :** 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S510632D-TC**
4. K4S510632D-TL**
5. Unless otherwise noticed, input swing level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$).

## AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

| Parameter | Value | Unit |
|---|---|---|
| AC input levels (Vih/Vil) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | tr/tf = 1/1 | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

## OPERATING AC PARAMETER
(AC operating conditions unless otherwise noted)

| Parameter | | Symbol | Version -7C | Version -75 | Version -1H | Version -1L | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Row active to row active delay | | tRRD(min) | 15 | 15 | 20 | 20 | ns | 1 |
| $\overline{RAS}$ to $\overline{CAS}$ delay | | tRCD(min) | 15 | 20 | 20 | 20 | ns | 1 |
| Row precharge time | | tRP(min) | 15 | 20 | 20 | 20 | ns | 1 |
| Row active time | | tRAS(min) | 45 | 45 | 50 | 50 | ns | 1 |
| | | tRAS(max) | 100 | | | | us | |
| Row cycle time | | tRC(min) | 60 | 65 | 70 | 70 | ns | 1 |
| Last data in to row precharge | | tRDL(min) | 2 | | | | CLK | 2, 5 |
| Last data in to Active delay | | tDAL(min) | 2 CLK + tRP | | | | - | 5 |
| Last data in to new col. address delay | | tCDL(min) | 1 | | | | CLK | 2 |
| Last data in to burst stop | | tBDL(min) | 1 | | | | CLK | 2 |
| Col. address to col. address delay | | tCCD(min) | 1 | | | | CLK | 3 |
| Number of valid output data | CAS latency=3 | | 2 | | | | ea | 4 |
| | CAS latency=2 | | 1 | | | | | |

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

## AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -7C | | -75 | | -1H | | -1L | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| CLK cycle time | CAS latency=3 | $t_{CC}$ | 7.5 | 1000 | 7.5 | 1000 | 10 | 1000 | 10 | 1000 | ns | 1 |
| | CAS latency=2 | | 7.5 | | 10 | | 10 | | 12 | | | |
| CLK to valid output delay | CAS latency=3 | $t_{SAC}$ | | 5.4 | | 5.4 | | 6 | | 6 | ns | 1,2 |
| | CAS latency=2 | | | 5.4 | | 6 | | 6 | | 7 | | |
| Output data hold time | CAS latency=3 | $t_{OH}$ | 3 | | 3 | | 3 | | 3 | | ns | 2 |
| | CAS latency=2 | | 3 | | 3 | | 3 | | 3 | | | |
| CLK high pulse width | | $t_{CH}$ | 2.5 | | 2.5 | | 3 | | 3 | | ns | 3 |
| CLK low pulse width | | $t_{CL}$ | 2.5 | | 2.5 | | 3 | | 3 | | ns | 3 |
| Input setup time | | $t_{SS}$ | 1.5 | | 1.5 | | 2 | | 2 | | ns | 3 |
| Input hold time | | $t_{SH}$ | 0.8 | | 0.8 | | 1 | | 1 | | ns | 3 |
| CLK to output in Low-Z | | $t_{SLZ}$ | 1 | | 1 | | 1 | | 1 | | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | $t_{SHZ}$ | | 5.4 | | 5.4 | | 6 | | 6 | ns | |
| | CAS latency=2 | | | 5.4 | | 6 | | 6 | | 7 | | |

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

## SIMPLIFIED TRUTH TABLE

| Command | | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | BA0,1 | A10/AP | A11,A12, A9 ~ A0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Mode register set | | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | | H | H | L | L | L | H | X | X | | | 3 |
| Refresh | Self refresh | Entry | H | L | L | L | L | H | X | X | | | 3 |
| Refresh | Self refresh | Exit | L | H | L | H | H | H | X | X | | | 3 |
| Refresh | Self refresh | Exit | L | H | H | X | X | X | X | X | | | 3 |
| Bank active & row addr. | | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column address (A0~A9, A11) | 4 |
| Read & column address | Auto precharge enable | | H | X | L | H | L | H | X | V | H | Column address (A0~A9, A11) | 4,5 |
| Write & column address | Auto precharge disable | | H | X | L | H | L | L | X | V | L | Column address (A0~A9, A11) | 4 |
| Write & column address | Auto precharge enable | | H | X | L | H | L | L | X | V | H | Column address (A0~A9, A11) | 4,5 |
| Burst stop | | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank selection | | H | X | L | L | H | L | X | V | L | X | |
| Precharge | All banks | | H | X | L | L | H | L | X | X | H | X | |
| Clock suspend or active power down | | Entry | H | L | H | X | X | X | X | X | | | |
| Clock suspend or active power down | | Entry | H | L | L | V | V | V | X | X | | | |
| Clock suspend or active power down | | Exit | L | H | X | X | X | X | X | X | | | |
| Precharge power down mode | | Entry | H | L | H | X | X | X | X | X | | | |
| Precharge power down mode | | Entry | H | L | L | H | H | H | X | X | | | |
| Precharge power down mode | | Exit | L | H | H | X | X | X | X | X | | | |
| Precharge power down mode | | Exit | L | H | L | V | V | V | X | X | | | |
| DQM | | | H | X | | | | | V | X | | | 7 |
| No operation command | | | H | X | H | X | X | X | X | X | | | |
| No operation command | | | H | X | L | H | H | H | X | X | | | |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :**
1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at $t_{RP}$ after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)