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4Mx16 SDRAM

D-die, 3.0V, CSP

Rev. 0.1
October, 2000

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Revision History

Revision 0.0 (September, 2000)

- First published.

Revision 0.1 (October, 2000)

- Changed AC/DC test output load condition from 50pF to 30pF
- Deleted *"DQ BUFFER OUTPUT DRIVE CHARACTERISTICS"*

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1M x 16Bit x 4 Banks Synchronous DRAM with CSP

FEATURES

- 3.0V Vdd/Vddq
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS latency (2 & 3)
  - Burst length (1, 2, 4, 8 & Full page)
  - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)
- Available in **CSP** package
- Extended Temperature(T_A = -25 to 85°C)
- Low Power

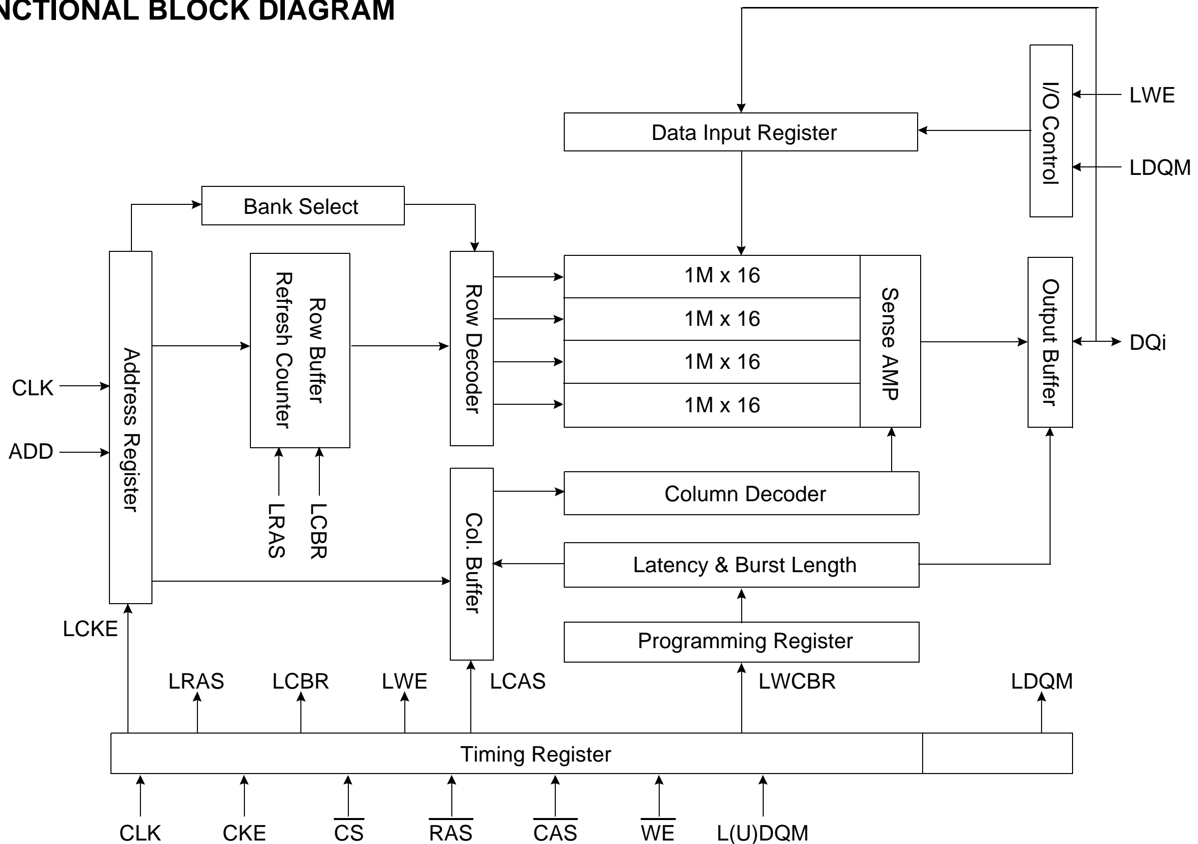
GENERAL DESCRIPTION

The K4S641633D is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4x1,048,576 words by 16 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

Part No.	Max Freq.	Temp.	Interface
K4S641633D-GN96	104MHz(CL=3)	Extended	LVTTL

FUNCTIONAL BLOCK DIAGRAM



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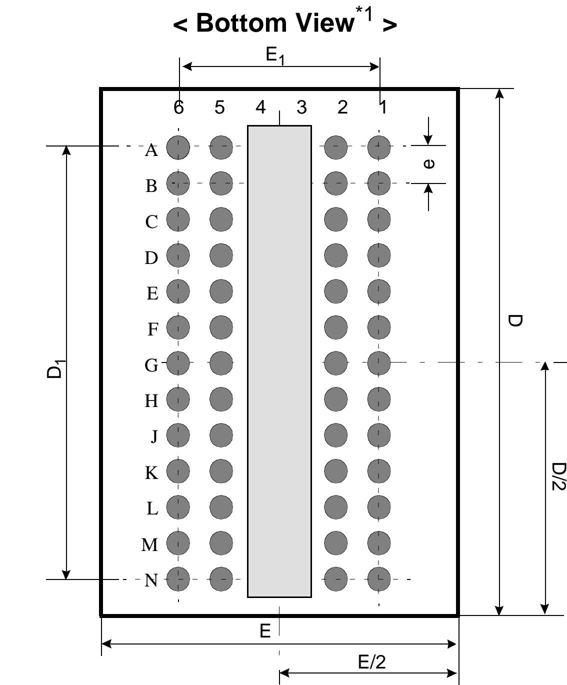
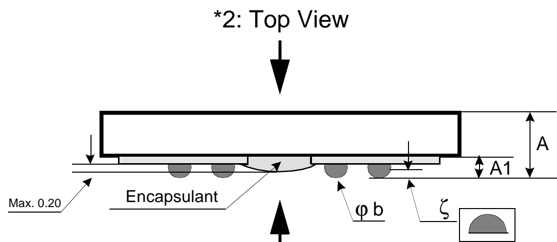
Package Dimension and Pin Configuration

< Bottom View*1 >

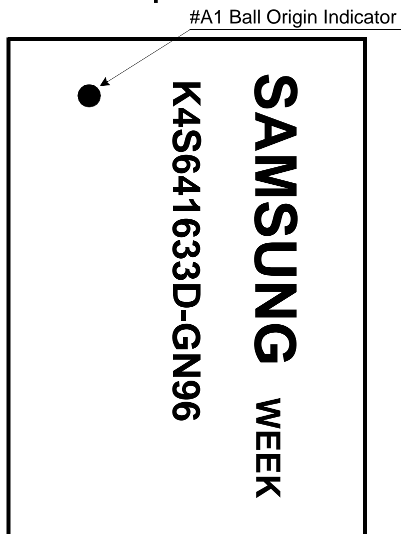


*2: Top View



*1: Bottom View

< Top View*2 >



< Top View*2 >

52Ball(4x13) CSP				
	1	2	5	6
A	Vss	DQ15	DQ0	VDD
B	DQ14	VSSQ	VDDQ	DQ1
C	DQ13	VDDQ	VSSQ	DQ2
D	DQ12	DQ11	DQ4	DQ3
E	DQ10	VSSQ	VDDQ	DQ5
F	DQ9	VDDQ	VSSQ	DQ6
G	DQ8	VDD	Vss	DQ7
H	CLK	UDQM	LDQM	$\overline{\text{WE}}$
J	CKE	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$
K	A11	A9	BA1	BA0
L	A8	A7	A0	A10
M	A6	A5	A2	A1
N	Vss	A4	A3	VDD

Pin Name	Pin Function
CLK	*System Clock*
$\overline{\text{CS}}$	*Chip Select*
CKE	*Clock Enable*
A0 ~ A11	*Address*
BA0 ~ BA1	*Bank Select Address*
$\overline{\text{RAS}}$	*Row Address Strobe*
$\overline{\text{CAS}}$	*Column Address Strobe*
$\overline{\text{WE}}$	*Write Enable*
L(U)DQM	*Data Input/Output Mask*
DQ0 ~ 15	*Data Input/Output*
VDD/VSS	*Power Supply/Ground*
VDDQ/VSSQ	*Data Output Power/Ground*

[Unit:mm]

Symbol	Min	Typ	Max
A	1.00	1.05	1.10
A_1	-	0.35	-
E	-	6.60	-
E_1	-	3.75	-
D	-	11.00	-
D_1	-	9.0	-
e	-	0.75	-
b	0.40	0.45	0.5
ζ	-	-	0.08

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 3.3	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 3.3	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, Extended Temperature : T_A = -25 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	2.7	3.0	3.3	V	
Input logic high votlage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current(Inputs)	I_{IL}	-5	-	5	uA	3
Input leakage current (I/O pins)	I_{IL}	-5	-	5	uA	3,4

Note :
1. V_{IH} (max) = 5.3V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include HI-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Dout is disabled, 0V ≤ V_{OUT} ≤ V_{DDQ}.

CAPACITANCE (VDD = 3.0V, TA = 23°C, f = 1MHz, VREF =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.0	3.5	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, L(U)DQM	C_{IN}	2.0	4.5	pF
Address	C_{ADD}	2.0	4.5	pF
DQ_0 ~ DQ_{15}	C_{OUT}	3.5	6.0	pF

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DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, Extended Temperature : T_A = -25 to 85°C)

Parameter	Symbol	Test Condition	CAS Latency	Version	Unit	Note
				-96		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_{OL} = 0 mA		70	mA	1
Precharge standby current in power-down mode	I_{CC2}P	CKE $\leq V_{IL}$(max), t_{CC} = 15ns		1	mA	
	I_{CC2}PS	CKE & CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		1		
Precharge standby current in non power-down mode	I_{CC2}N	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns		12	mA	
	I_{CC2}NS	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		6		
Active standby current in power-down mode	I_{CC3}P	CKE $\leq V_{IL}$(max), t_{CC} = 15ns		2	mA	
	I_{CC3}PS	CKE & CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		2		
Active standby current in non power-down mode (One bank active)	I_{CC3}N	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 15ns Input signals are changed one time during 30ns		20	mA	
	I_{CC3}NS	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		10	mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2Banks activated t_{CCD} = 2CLKs	3	90	mA	1
			2	85		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		125	mA	2
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V		450	uA	3

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. Low Power Self refresh Current

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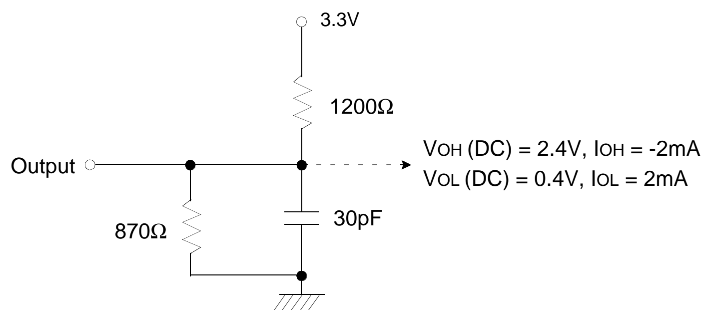
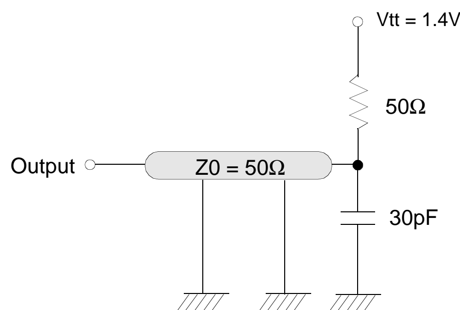
AC OPERATING TEST CONDITIONS (V_{DD} = 3.0V ± 0.3V, Extended Temperature : T_A = -25 to 85°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version -96	Unit	Note
Row active to row active delay		t_{RRD}(min)	19.2(2)	ns(CLK)	
$\overline{RAS}$ to $\overline{CAS}$ delay		t_{RCD}(min)	28.8(3)	ns(CLK)	
Row precharge time		t_{RP}(min)	28.8(3)	ns(CLK)	
Row active time		t_{RAS}(min)	48.0(5)	ns(CLK)	
		t_{RAS}(max)	100	us	
Row cycle time		t_{RC}(min)	76.8(8)	ns(CLK)	
Last data in to row precharge		t_{RDL}(min)	9.6(1)	ns(CLK)	1
Last data in to new col. address Delay		t_{CDL}(min)	1	CLK	1
Last data in to burst stop		t_{BDL}(min)	1	CLK	1
Col. address to col. address delay		t_{CCD}(min)	1	CLK	2
Number of valid output data	CAS latency=3		2	ea	3
	CAS latency=2		1		

Notes : 1. Minimum delay is required to complete write.
2. All parts allow every cycle column address change.
3. In case of row precharge interrupt, auto precharge and read burst stop.

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AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-96		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	9.6	1000	ns	1
	CAS latency=2		19.2			
CLK to valid output delay	CAS latency=3	tSAC		6	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3		ns	3
CLK low pulse width		tCL	3		ns	3
Input setup time		tSS	2		ns	3
Input hold time		tSH	1		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		6	ns	
	CAS latency=2			7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

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SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
Refresh	Self refresh	Entry	H	L	L	L	L	H	X	X			3
Refresh	Self refresh	Exit	L	H	L	H	H	H	X	X			3
Refresh	Self refresh	Exit	L	H	H	X	X	X	X	X			3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address (A_0 ~ A_7)	4
Read & column address	Auto precharge enable		H	X	L	H	L	H	X	V	H	Column address (A_0 ~ A_7)	4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address (A_0 ~ A_7)	4
Write & column address	Auto precharge enable		H	X	L	H	L	L	X	V	H	Column address (A_0 ~ A_7)	4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
Precharge	All banks		H	X	L	L	H	L	X	X	H	X	
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
Clock suspend or active power down		Entry	H	L	L	V	V	V	X	X			
Clock suspend or active power down		Exit	L	H	X	X	X	X	X	X			
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
Precharge power down mode		Entry	H	L	L	H	H	H	X	X			
Precharge power down mode		Exit	L	H	H	X	X	X	X	X			
Precharge power down mode		Exit	L	H	L	V	V	V	X	X			
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
No operation command			H	X	L	H	H	H	X	X			

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :
1. OP Code : Operand code
   A_0 ~ A_{11} & BA_0 ~ BA_1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)