Document Title

8M DDR SYNCHRONOUS SRAM

Revision History

Rev No.	History	DraftData	Remark
Rev. 0.0	-Initial document.	July. 2000	Advance
Rev. 0.1	-ZQ tolerance changed from 10% to 15%	Aug. 2000	Advance
Rev. 0.2	-Stop Clock Standby Current condition changed from $V_{IN}=V_{DD}$-0.2V or 0.2V fixed to $V_{IN}=V_{IH}$ or V_{IH}	Oct. 2000	Advance
Rev. 0.3	-V_{DDQ} Max. changed to 2.0V SA0, SA1 defined for Boundary Scan Order	Nov. 2000	Advance
Rev. 0.5	-Deleted -HC16 part(Part Number, Idd, AC Characterisctics)	Jan. 2001	Prelimary
Rev. 0.6	- Absolute Maximum ratings V_{DDQ} changed from 3.13V to 2.825V	Feb. 2001	Prelimary
Rev. 0.7	- $\overline{LBO}$ input level changed from High/Low to V_{DDQ}/V_{SS} - Stop Clock Standby Current condition changed from K=Low, $\overline{K}$=High to K=Low, $\overline{K}$=Low - t_{CHQV}/t_{CLQV} changed from 0.1ns to 0.2ns for -33 part from 0.1ns to 0.2ns for -30 part from 0.1ns to 0.25ns for -25part - t_{CHQX}/t_{CLQX} changed from -0.3ns to -0.2ns for -33 part from -0.3ns to -0.2ns for -30 part from -0.4ns to -0.25ns for -25part - t_{CHQZ}/t_{CLQZ} changed from 0.1ns to 0.2ns for -33 part from 0.1ns to 0.2ns for -30 part from 0.1ns to 0.25ns for -25part - t_{KXCH} changed from 1.8ns to 1.7ns for -33 part - t_{KXCL} changed from 1.8ns to 1.7ns for -33 part	Mar. 2001	Prelimary
Rev. 1.0	- Clarification on the features and the timing waveforms regarding the burst controllability. - Recommended DC operating conditions for Clock added. - AC test conditions for V_{DDQ}=1.8V and Single ended clock added. (AC Test Conditions 2) - Package thermal characteristics added.	May. 2001	Final
Rev. 2.0	- Add-HC35 part(Part Number, Idd, AC Characteristics)	Sep. 2001	Final
Rev. 3.0	- Absolute Maximum Rating VDDQ changed from 2.825V to 2.4V - V_{CM-CLK} Min changed from 0.6V to 0.68V	Jan. 2002	Final
Rev. 4.0	- Add-HC37 part(Part Number, Idd, AC Characteristics)	Jan. 2002	Final

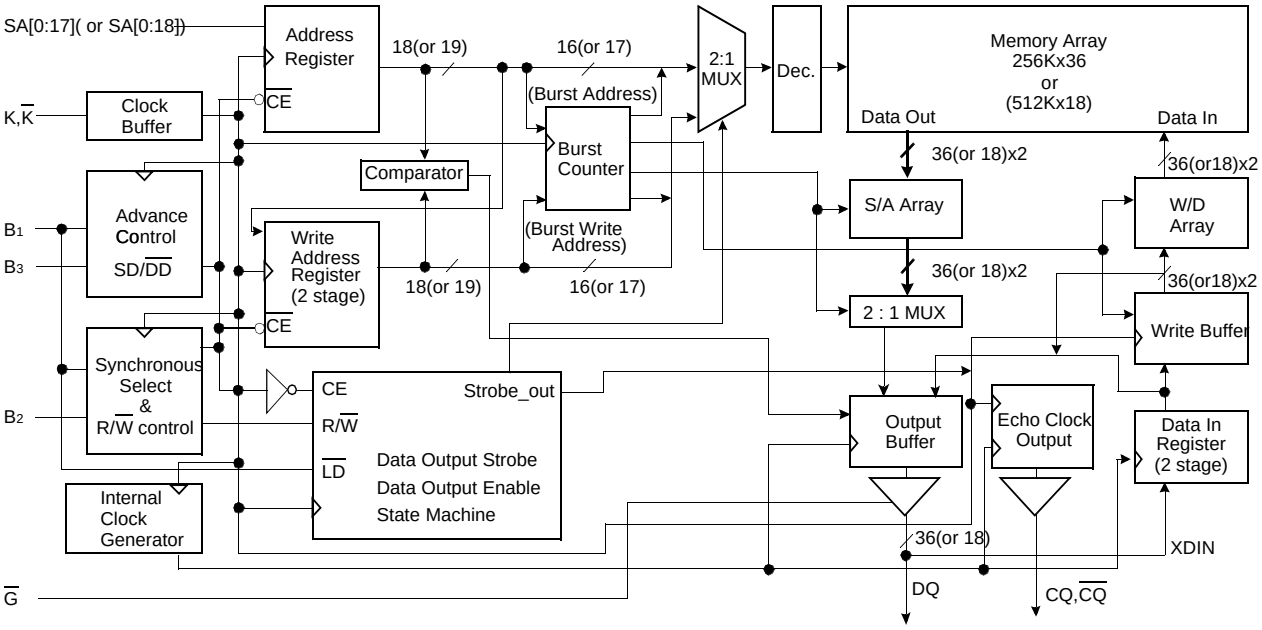
FEATURES

- 256Kx36 or 512Kx18 Organizations.
- Maximum Frequency : 370MHz (Data Rate : 740Mbps)
- 2.5V V_{DD}/1.5V V_{DDQ} (2.0V max V_{DDQ}).
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write
- Free Running Active High and Active Low Echo Clock Output Pin.
- Asynchronous Output Enable.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Single and Double Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Pin Ball Grid Array Package(14mm x 22mm).

Organization	Part Number	Maximum Frequency	Access Time
256Kx36	K7D803671B-HC37	370MHz	1.7*
	K7D803671B-HC35	357MHz	1.7*
	K7D803671B-HC33	333MHz	1.7*
	K7D803671B-HC30	300MHz	1.9*
	K7D803671B-HC25	250MHz	2.0*
512Kx18	K7D801871B-HC37	370MHz	1.7*
	K7D801871B-HC35	357MHz	1.7*
	K7D801871B-HC33	333MHz	1.7*
	K7D801871B-HC30	300MHz	1.9*
	K7D801871B-HC25	250MHz	2.0*

NOTE : *Access time equals t_{KXCH}/t_{KXCL}

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks	ZQ	Output Driver Impedance Control Input
SA	Synchronous Address Input	TCK	JTAG Test Clock
SA_0, SA_1	Synchronous Burst Address Input (SA_0 = LSB)	TMS	JTAG Test Mode Select
DQ	Synchronous Data I/O	TDI	JTAG Test Data Input
CQ, $\overline{CQ}$	Differential Output Echo Clocks	TDO	JTAG Test Data Output
B_1	Load External Address	V_{REF}	HSTL Input Reference Voltage
B_2	Burst R/$\overline{W}$ Enable	V_{DD}	Power Supply
B_3	Single/Double Data Selection	V_{DDQ}	Output Power Supply
$\overline{G}$	Asynchronous Output Enable	V_{SS}	GND
$\overline{LBO}$	Linear Burst Order	NC	No Connection

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D803671B(256Kx36)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	DQ	DQ	SA	V_{SS}	B_1	V_{SS}	SA	DQ	DQ
C	V_{SS}	V_{DDQ}	SA	SA	$\overline{G}$	SA	SA	V_{DDQ}	V_{SS}
D	DQ	DQ	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	DQ
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	DQ	CQ_1	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	CQ_2	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	K	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	DQ	DQ	V_{DD}	$\overline{K}$	V_{DD}	DQ	DQ	DQ
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	DQ	DQ	DQ	V_{SS}	B_2	V_{SS}	DQ	DQ	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B_3	MODE	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	$\overline{CQ_1}$	DQ	V_{DD}	V_{DD}	V_{DD}	DQ	$\overline{CQ_2}$	DQ
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	DQ	DQ	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	DQ
R	V_{SS}	V_{DDQ}	V_{DD}	SA	SA_1	SA	V_{DD}	V_{DDQ}	V_{SS}
T	DQ	DQ	SA	V_{SS}	SA_0	V_{SS}	SA	DQ	DQ
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

* Mode Pin(6L) is a internally NC.

K7D801871B(512Kx18)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	SA	SA	ZQ	SA	SA	V_{DDQ}	V_{SS}
B	NC	DQ	SA	V_{SS}	B_1	V_{SS}	SA	NC	DQ
C	V_{SS}	V_{DDQ}	SA	SA	$\overline{G}$	SA	SA	V_{DDQ}	V_{SS}
D	DQ	NC	NC	V_{SS}	V_{DD}	V_{SS}	SA	DQ	NC
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	NC	CQ_1	NC	V_{DD}	V_{DD}	V_{DD}	DQ	NC	DQ
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	K	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	DQ	NC	DQ	V_{DD}	$\overline{K}$	V_{DD}	NC	DQ	NC
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	NC	DQ	NC	V_{SS}	B_2	V_{SS}	DQ	NC	DQ
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B_3	MODE	V_{SS}	V_{DDQ}	V_{SS}
M	DQ	NC	DQ	V_{DD}	V_{DD}	V_{DD}	NC	$\overline{CQ_1}$	NC
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{REF}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	NC	DQ	SA	V_{SS}	V_{DD}	V_{SS}	SA	NC	DQ
R	V_{SS}	V_{DDQ}	V_{DD}	SA	SA_1	SA	V_{DD}	V_{DDQ}	V_{SS}
T	DQ	NC	SA	V_{SS}	SA_0	V_{SS}	SA	DQ	NC
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

* Mode Pin(6L)is a internally NC.

FUNCTION DESCRIPTION

The K7D803671B and K7D801871B are 9,437,184 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 262,144 words by 36 bits for K7D803671B and 524,288 words by 18 bits for K7D801871B, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level clock, K and $\overline{K}$ are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted(Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.

Data outputs are updated from output registers off the rising edges of K clock for SDR read operations, and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representive of data output access time for all SDR and DDR operations.

The chip is operated with a single +2.5V power supply and is compatible with Extended HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.

Interleave and linear burst operation is controlled by $\overline{LBO}$ pin and the burst count is controllable with the maximum burst length of 4.

To avoid data contention,at least one NOP operations are required between the last read and the first write operation.

Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write opeation are data inputs fully written into SRAM array.

Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.

Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs outputs.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, RQ, connected between ZQ pin and V_{SS}, and are equal to RQ/5. For example, 250Ω resistor will give an output impedance of 50Ω. Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with $\overline{G}$ high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time $\overline{G}$ are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

TRUTH TABLE

K	$\overline{G}$	B1	B2	B3	DQ	Operation
L	X	X	X	X	Hi-Z	Clock Stop
↑	X	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	L	H	H	DOUT	Load Address, Single Read
↑	L	L	H	L	DOUT	Load Address, Double Read
↑	X	L	L	H	DIN	Load Address, Single Write
↑	X	L	L	L	DIN	Load Address, Double Write
↑	X	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".
- K & $\overline{K}$ are complementary.

BURST SEQUENCE TABLE

4 Burst Operation for Interleaved Burst ($\overline{LBO}$ = V_{DDQ})

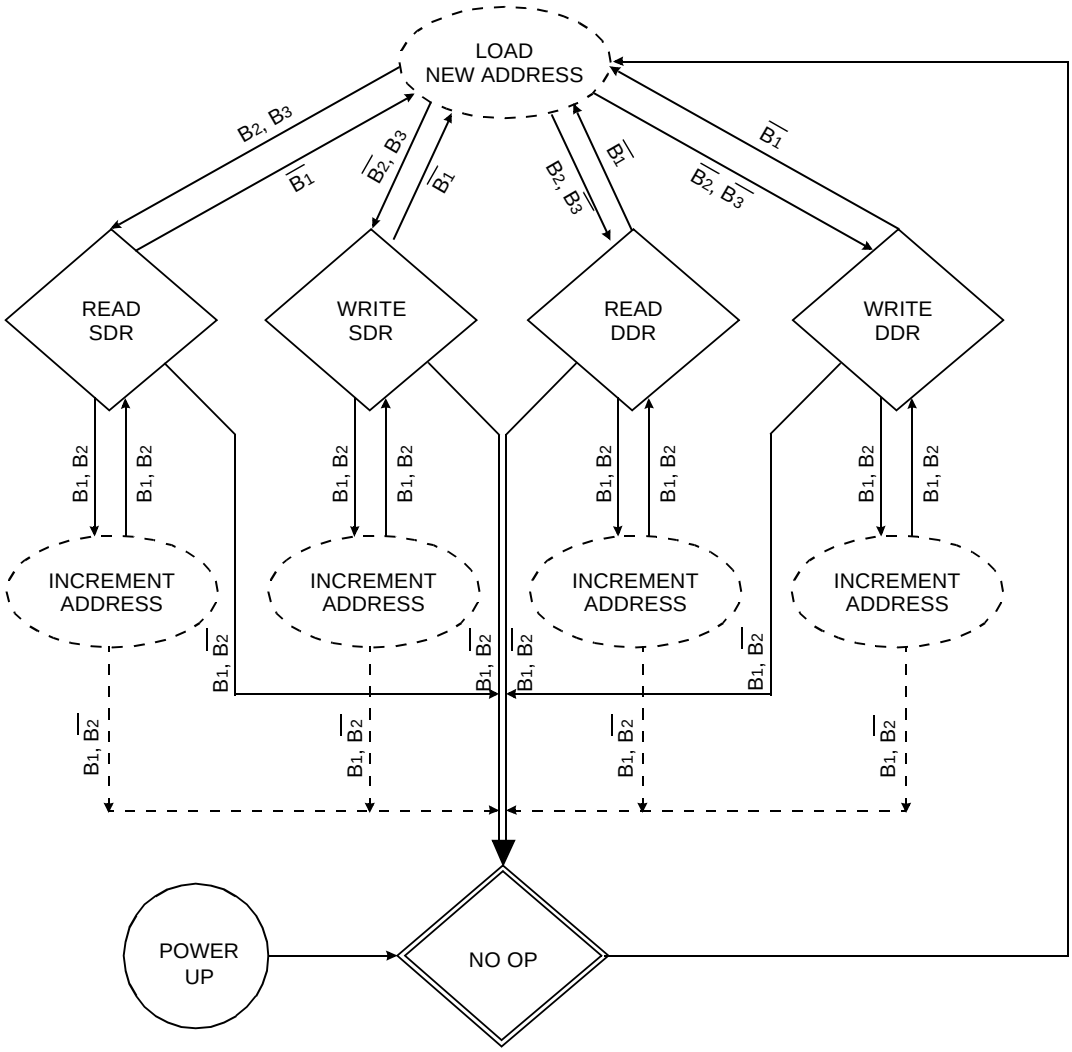
Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst $\overline{LBO}$ = V_{DDQ} is recommended. If $\overline{LBO}$ = V_{DD}, it must not exceed 2.63V.

4 Burst Operation for Linear Burst ($\overline{LBO}$ = V_{SS})

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

1. State transitions ; $\overline{B_1}$ =(Load Address), B_1=(Increment Address, Continue)
   B_2 =(Read), $\overline{B_2}$ =(Write)
   B_3 =(Single Data Rate), $\overline{B_3}$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to V_{SS}	V_{DD}	-0.5 to 3.13	V
Output Supply Voltage Relative to V_{SS}	V_{DDQ}	-0.5 to 2.4	V
Voltage on any pin Relative to V_{SS}	V_{IN}	-0.5 to V_{DDQ}+0.5 (2.4V MAX)	V
Output Short-Circuit Current(per I/O)	I_{OUT}	25	mA
Storage Temperature	T_{STR}	-55 to 125	°C

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	2.37	2.5	2.63	V	
Output Power Supply Voltage	V_{DDQ}	1.4	1.5	2.0	V	
Input High Level Voltage	V_{IH}	V_{REF}+0.1	-	V_{DDQ}+0.3	V	1, 2
Input Low Level Voltage	V_{IL}	-0.3	-	V_{REF}-0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	1.0	V	
Clock Input Signal Voltage	V_{IN-CLK}	-0.3	-	V_{DDQ}+0.3	V	1, 4
Clock Input Differential Voltage	$V_{DIF-CLK}$	0.1	-	V_{DDQ}+0.6	V	1, 5
Clock Input Common Mode Voltage	V_{CM-CLK}	0.68	0.75	0.9	V	1, 6

NOTE : 1. These are DC test criteria. DC design criteria is V_{REF}±50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC=V_{DDQ}+0.3, V_{IH} (Max)AC=2.6V (2.1V for DQs) (pulse width ≤ 20% of cycle time).
3. V_{IL} (Min)DC=-0.3V, V_{IL} (Min)AC=-1.0V (-0.5V for DQs) (pulse width ≤ 20% of cycle time).
4. V_{IN-CLK} specifies the maximum allowable DC level for the differential clock. i.e V_{IL-CLK} and V_{IH-CLK}.
5. $V_{DIF-CLK}$ specifies the minimum Clock differential voltage required for switching. i.e DC voltage difference between V_{IL-CLK} and V_{IH-CLK}.
6. V_{CM-CLK} specifies the Clock crossing point for the differential clock or the allowable common clock level for a single ended clock.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = t_{KHKH} min)	I_{DD37} I_{DD35} I_{DD33} I_{DD30} I_{DD25}	-	880 850 750 670 600	mA	1,2
Average Power Supply Operating Current(x18) (Cycle time = t_{KHKH} min)	I_{DD37} I_{DD35} I_{DD33} I_{DD30} I_{DD25}	-	830 800 700 620 550	mA	1,2
Stop Clock Standby Current (V_{IN}=V_{IH} or V_{IL}, K=Low, $\overline{K}$=Low)	I_{SB1}	-	150	mA	1
Input Leakage Current (V_{IN}=V_{SS} or V_{DDQ})	I_{LI}	-1	1	µA	
Output Leakage Current (V_{OUT}=V_{SS} or V_{DDQ})	I_{LO}	-1	1	µA	
Output High Voltage(Programmable Impedance Mode)	V_{OH1}	V_{DDQ}/2	V_{DDQ}	V	3
Output Low Voltage(Programmable Impedance Mode)	V_{OL1}	V_{SS}	V_{DDQ}/2	V	4
Output High Voltage(I_{OH}=-0.1mA)	V_{OH2}	V_{DDQ}-0.2	V_{DDQ}	V	5
Output Low Voltage(I_{OL}=0.1mA)	V_{OL2}	V_{SS}	0.2	V	5

NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.
3. $|I_{OH}|$=(V_{DDQ}/2)/(RQ/5)±15% @V_{OH}=V_{DDQ}/2 for 175Ω ≤ RQ ≤ 350Ω.
4. $|I_{OL}|$=(V_{DDQ}/2)/(RQ/5)±15% @V_{OL}=V_{DDQ}/2 for 175Ω ≤ RQ ≤ 350Ω.
5. Minimum Impedance Mode when ZQ pin is connected to V_{ss}.

PIN CAPACITANCE

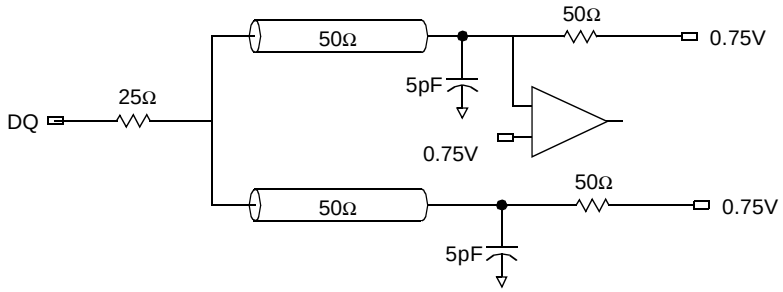
Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	4	pF
Data Output Capacitance	C_{OUT}	V_{OUT}=0V	-	5	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=1MHz)

AC TEST CONDITIONS 1 (T_A=0 to 70°C, V_{DD}=2.37 -2.63V, V_{DDQ}=1.5V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.25/0.25	V	-
Input Reference Level	V_{REF}	0.75	V	-
Input Rise/Fall Time	T_R/T_F	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load	See Below			-

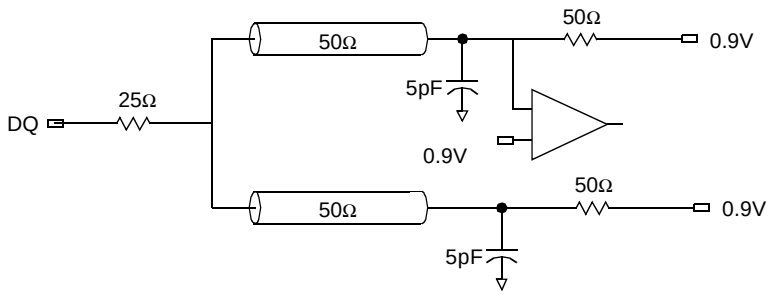
AC TEST OUTPUT LOAD 1



AC TEST CONDITIONS 2 (T_A=0 to 70°C, V_{DD}=2.37 -2.63V, V_{DDQ}=1.8V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.64/0.18	V	-
Input Reference Level	V_{REF}	0.9	V	-
Input Rise/Fall Time	T_R/T_F	0.5/0.5	ns	-
Output Timing Reference Level		0.9	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load	See Below			-

AC TEST OUTPUT LOAD 2



AC CHARACTERISTICS(For both AC test condition 1 and 2)

Parameter	Symbol	-33		-30		-25		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	3.0	-	3.3	-	4.0	-	ns	
Clock High Pulse Width	t_{KHKL}	1.3	-	1.5	-	1.7	-	ns	
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.5	-	1.7	-	ns	
CQ High Pulse Width	t_{CHCL}	t_{KHKL}-0.1	t_{KHKL}+0.1	t_{KHKL}-0.2	t_{KHKL}+0.2	t_{KHKL}-0.3	t_{KHKL}+0.3	ns	
CQ Low Pulse Width	t_{CLCH}	t_{KLKH}-0.1	t_{KLKH}+0.1	t_{KLKH}-0.2	t_{KLKH}+0.2	t_{KLKH}-0.3	t_{KLKH}+0.3	ns	
Clock to Echo Clock(CQ) High	t_{KXCH}	0.5	1.7	0.5	1.9	0.5	2.0	ns	1
Clock to Echo Clock(CQ) Low	t_{KXCL}	0.5	1.7	0.5	1.9	0.5	2.0	ns	
Echo Clock to Output Valid	t_{CHQV}/t_{CLQV}	-	0.2	-	0.2	-	0.25	ns	1,2
Echo Clock to Output Hold	t_{CHQX}/t_{CLQX}	-0.2	-	-0.2	-	-0.25	-	ns	1
Echo Clock to Output High-Z	t_{CHQZ}/t_{CLQZ}		0.2		0.2		0.25	ns	1
$\overline{G}$ Low to Output Low-Z	t_{GLQX}	0.5	-	0.5	-	0.5	-	ns	1
$\overline{G}$ High to Output High-Z	t_{GHQZ}	-	2.1	-	2.3	-	2.5	ns	1
$\overline{G}$ Low to Output Valid	t_{GLQV}	-	2.1	-	2.3	-	2.5	ns	1
Address Setup Time	t_{AVKH}	0.4	-	0.4	-	0.5	-	ns	
Address Hold Time	t_{KHAX}	0.4	-	0.4	-	0.5	-	ns	
Burst Control Setup Time	t_{BVKH}	0.4	-	0.4	-	0.5	-	ns	
Burst Control Hold Time	t_{KHBX}	0.4	-	0.4	-	0.5	-	ns	
Data Setup Time	t_{DVKH}	0.4	-	0.4	-	0.5	-	ns	
Data Hold Time	t_{KHDX}	0.4	-	0.4	-	0.5	-	ns	

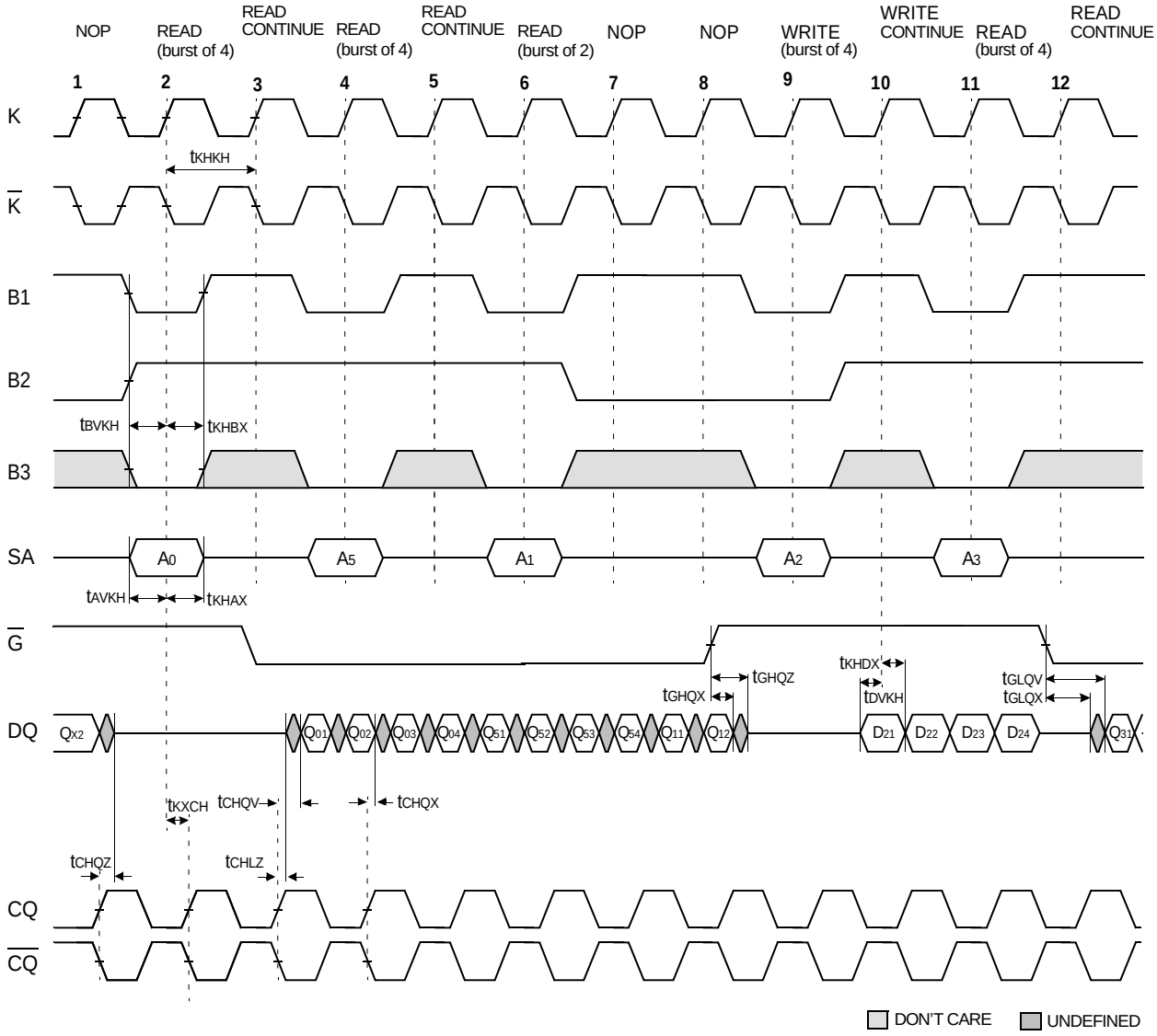
NOTE : 1. See AC Test Output Load figure
2. Design target is 0ns

AC CHARACTERISTICS(For AC test condition 1)

Parameter	Symbol	-37		-35		Unit	Note
		Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	2.7	-	2.8	-	ns	
Clock High Pulse Width	t_{KHKL}	1.3	-	1.3	-	ns	
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.3	-	ns	
CQ High Pulse Width	t_{CHCL}	t_{KHKL}-0.1	t_{KHKL}+0.1	t_{KHKL}-0.1	t_{KHKL}+0.1	ns	
CQ Low Pulse Width	t_{CLCH}	t_{KLKH}-0.1	t_{KLKH}+0.1	t_{KLKH}-0.1	t_{KLKH}+0.1	ns	
Clock to Echo Clock(CQ) High	t_{KXCH}	0.5	1.7	0.5	1.7	ns	1
Clock to Echo Clock(CQ) Low	t_{KXCL}	0.5	1.7	0.5	1.7	ns	
Echo Clock to Output Valid	t_{CHQV}/t_{CLQV}	-	0.2	-	0.2	ns	1,2
Echo Clock to Output Hold	t_{CHQX}/t_{CLQX}	-0.2	-	-0.2	-	ns	1
Echo Clock to Output High-Z	t_{CHQZ}/t_{CLQZ}		0.2		0.2	ns	1
$\overline{G}$ Low to Output Low-Z	t_{GLQX}	0.5	-	0.5	-	ns	1
$\overline{G}$ High to Output High-Z	t_{GHQZ}	-	2.1	-	2.1	ns	1
$\overline{G}$ Low to Output Valid	t_{GLQV}	-	2.1	-	2.1	ns	1
Address Setup Time	t_{AVKH}	0.4	-	0.4	-	ns	
Address Hold Time	t_{KHAX}	0.4	-	0.4	-	ns	
Burst Control Setup Time	t_{BVKH}	0.4	-	0.4	-	ns	
Burst Control Hold Time	t_{KHBX}	0.4	-	0.4	-	ns	
Data Setup Time	t_{DVKH}	0.4	-	0.4	-	ns	
Data Hold Time	t_{KHDX}	0.4	-	0.4	-	ns	

NOTE : 1. See AC Test Output Load figure
2. Design target is 0ns

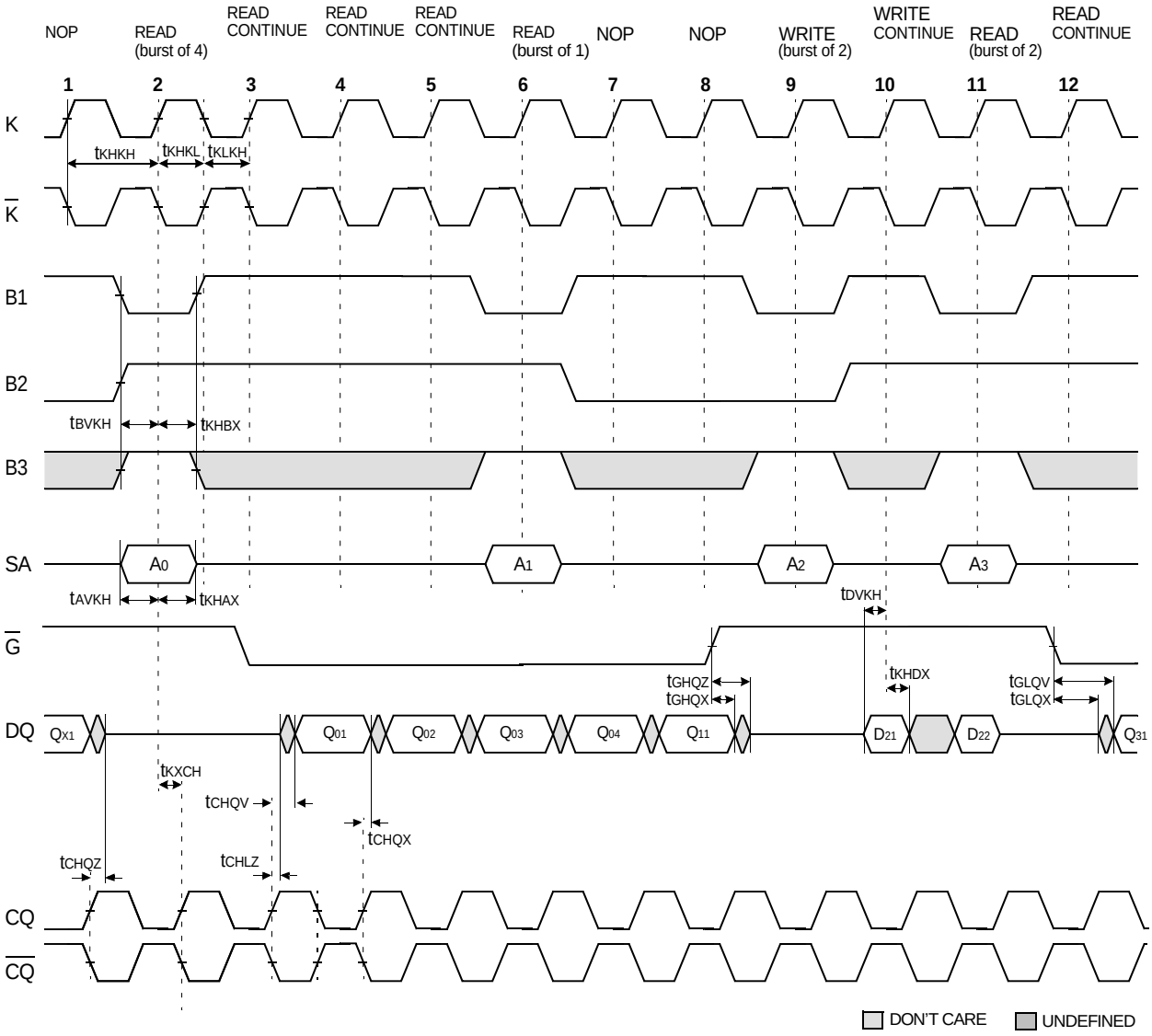
TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES (Burst Length=4, 2)



NOTE

1. Q_{01} refers to output from address A. Q_{02} refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES (Burst Length=4, 2, 1)



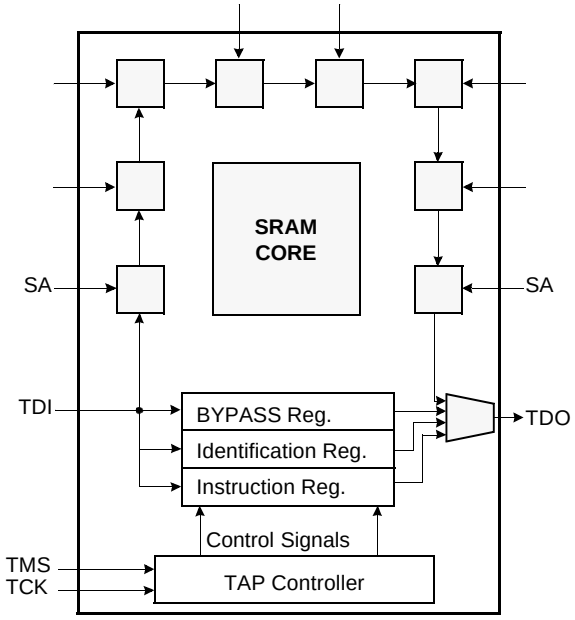
NOTE :

1. Q_{01} refers to output from address A_0. Q_{02} refers to output from the next internal burst address following A_0, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This devices supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM. TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram

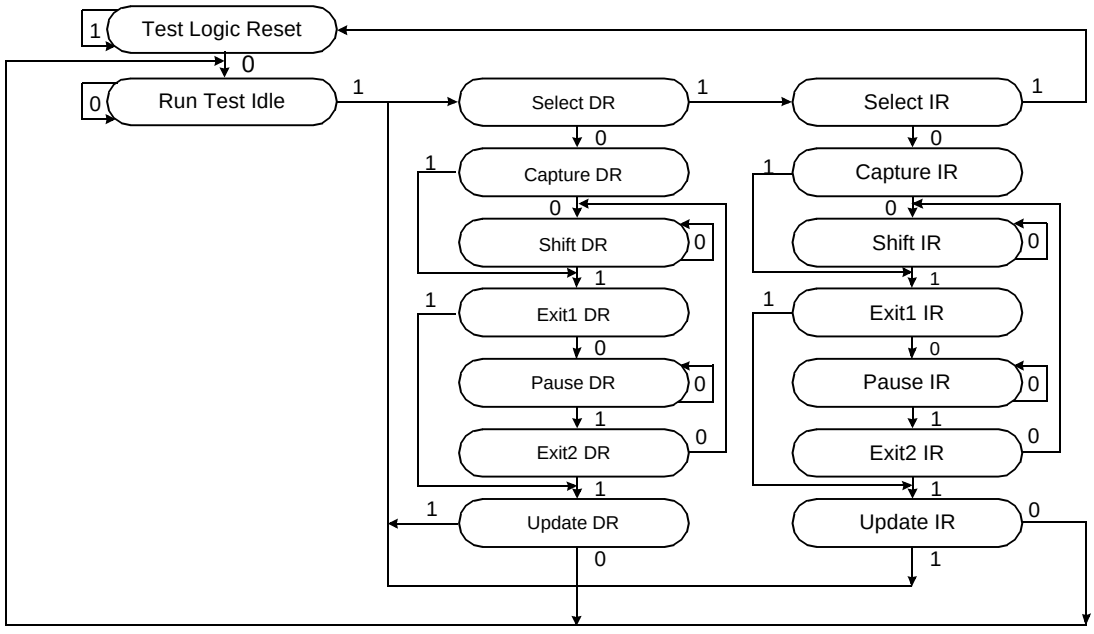


JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :
1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked.
   The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx36	3 bits	1 bits	32 bits	68 bits
512Kx18	3 bits	1 bits	32 bits	49 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
256Kx36	0000	00110 00100	XXXXXX	00001001110	1
512Kx18	0000	00111 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	4A	SA		SA	6A	35
37	4C	SA		SA	6C	34
38	3A	SA		SA	7A	33
39	3B	SA		SA	7B	32
40	3C	SA		SA	7C	31
41	3D	NC		SA	7D	30
42	2B	DQ		DQ	8B	29
43	1B	DQ		DQ	9B	28
44	2D	DQ		DQ	8D	27
45	3F	DQ		DQ	7F	26
46	1D	DQ		DQ	9D	25
47	2F	CQ		CQ	8F	24
48	1F	DQ		DQ	9F	23
49	3H	DQ		DQ	7H	22
50	2H	DQ		DQ	8H	21
51	1H	DQ		DQ	9H	20
52	5A	ZQ		$\overline{G}$	5C	19
53	5B	B_1		K	5G	18
54	5K	B_2		$\overline{K}$	5H	17
55	5L	B_3		NC	6L	16
56	4L	$\overline{LBO}$		DQ	9K	15
57	1K	DQ		DQ	8K	14
58	2K	DQ		DQ	7K	13
59	3K	DQ		DQ	9M	12
60	1M	DQ		$\overline{CQ}$	8M	11
61	2M	$\overline{CQ}$		DQ	9P	10
62	1P	DQ		DQ	7M	9
63	3M	DQ		DQ	8P	8
64	2P	DQ		DQ	9T	7
65	1T	DQ		DQ	8T	6
66	2T	DQ		SA	7P	5
67	3T	SA		SA	7T	4
68	4R	SA		SA	6R	3
				SA_0	5T	2
				SA_1	5R	1

1.Pin 6L is reserved for Mode Pin and the scanned data is fixed to "0"
2.Pin 3D is reserved for Address bit for 16Mb density and
the scanned data is fixed to "0"

BOUNDARY SCAN EXIT ORDER(x18)

26	4A	SA		SA	6A	25
27	4C	SA		SA	6C	24
28	3A	SA		SA	7A	23
29	3B	SA		SA	7B	22
30	3C	SA		SA	7C	21
31	3D	NC		SA	7D	20
32	2B	DQ				
				DQ	9B	19
				DQ	8D	18
				DQ	7F	17
33	1D	DQ				
34	2F	CQ				
				DQ	9F	16
35	3H	DQ				
				DQ	8H	15
36	1H	DQ				
37	5A	ZQ		$\overline{G}$	5C	14
38	5B	B_1		K	5G	13
39	5K	B_2		$\overline{K}$	5H	12
40	5L	B_3		NC	6L	11
41	4L	$\overline{LBO}$		DQ	9K	10
42	2K	DQ		DQ	7K	9
43	1M	DQ		$\overline{CQ}$	8M	8
				DQ	9P	7
44	3M	DQ				
45	2P	DQ				
46	1T	DQ		DQ	8T	6
				SA	7P	5
47	3P	SA		SA	7T	4
48	3T	SA		SA	6R	3
49	4R	SA		SA_0	5T	2
				SA_1	5R	1

1.Pin 6L is reserved for Mode Pin and the scanned data is fixed to "0"
2.Pin 3D is reserved for Address bit for 16Mb density and
the scanned data is fixed to "0"

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.37	2.5	2.63	V	
Input High Level	V_{IH}	1.7	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.7	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	2.1	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

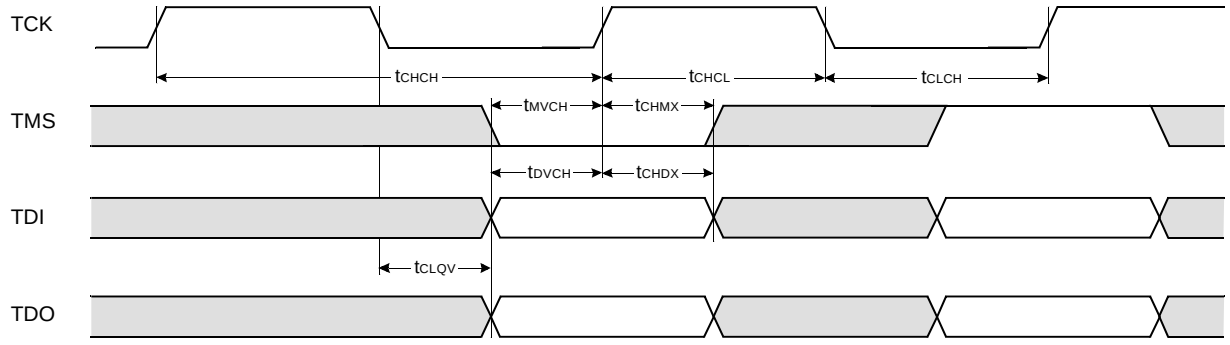
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.25	V	1

NOTE : 1. See SRAM AC test output load on page 5.

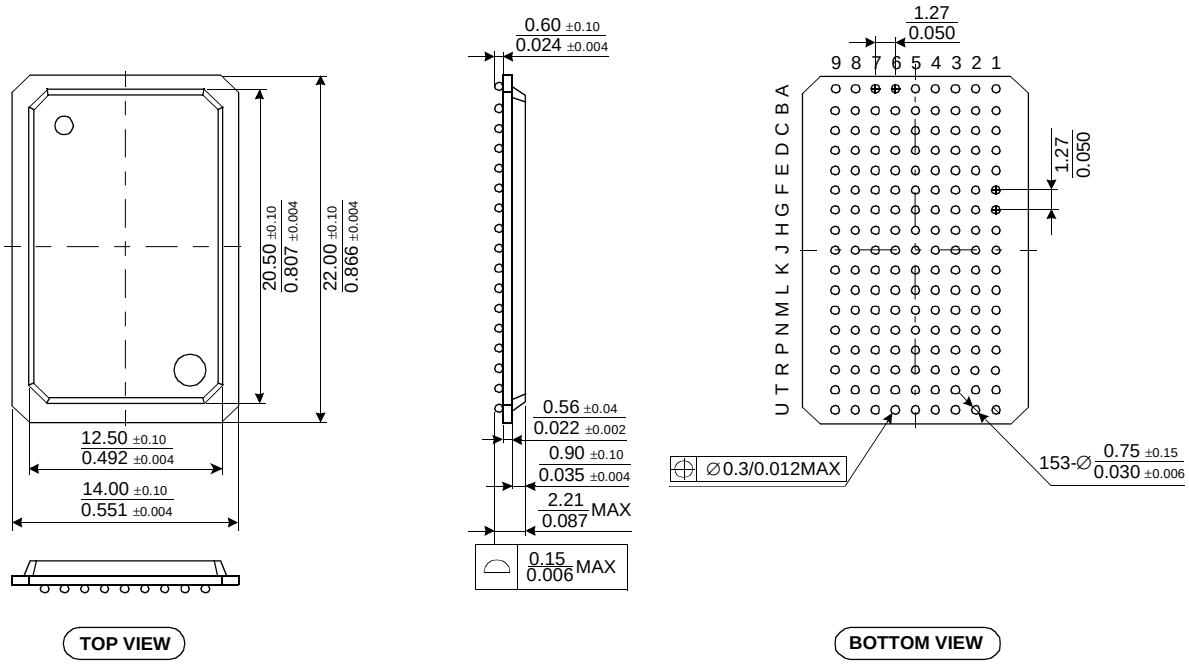
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



153 BGA PACKAGE DIMENSIONS



NOTE :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCS Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

153 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient(at still air)	Theta_JA	30.0	°C/W	1W Heating
Junction to Case	Theta_JC	5.9	°C/W	
Junction to Board	Theta_JB	4.8	°C/W	2W Heating

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times Theta\_JA$.