# Buffered 8Mx64 DIMM

(4Mx16 base)

Revision 0.1

June 1998

## Revision History

### Version 0.0 (Sept. 1997)

• Removed two AC parameters $t_{CACP}$(access time from $\overline{CAS}$) and $t_{AAP}$(access time from col. addr.) in *AC CHARACTERISTICS*.
• Changed the parameter $t_{CAC}$(access time from $\overline{CAS}$) from 18ns to 20ns @ -5 in *AC CHARACTERISTICS.*

### Version 0.1 (June 1998)

• The 3rd. generation of 64M components are applied for this module.

# M364C080(8)4BT0-C Fast Page Mode

8M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 5V

## GENERAL DESCRIPTION

The Samsung M364C080(8)4BT0-C is a 4Mx64bits Dynamic RAM high density memory module. The Samsung M364C080(8)4BT0-C consists of eight CMOS 4Mx16bits DRAMs in TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M364C080(8)4BT0-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

## PERFORMANCE RANGE

| Speed | $t_{RAC}$ | $t_{CAC}$ | $t_{RC}$ | $t_{PC}$ |
|---|---|---|---|---|
| -C50 | 50ns | 18ns | 90ns | 35ns |
| -C60 | 60ns | 20ns | 110ns | 40ns |

## FEATURES

- Part Identification

| Part number | PKG | Ref. | CBR Ref. | ROR Ref. |
|---|---|---|---|---|
| M364C0804BT0-C | TSOPII | 4K | 4K/64ms | |
| M364C0884BT0-C | TSOPII | 8K | 4K/64ms | 8K/64ms |

- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single 5V±10% power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : Height(1000mil), double sided component

## PIN CONFIGURATIONS

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Vss | 29 | $\overline{CAS2}$ | 57 | DQ22 | 85 | Vss | 113 | $\overline{CAS3}$ | 141 | DQ58 |
| 2 | DQ0 | 30 | $\overline{RAS0}$ | 58 | DQ23 | 86 | DQ36 | 114 | $\overline{RAS1}$ | 142 | DQ59 |
| 3 | DQ1 | 31 | $\overline{OE0}$ | 59 | Vcc | 87 | DQ37 | 115 | RFU | 143 | Vcc |
| 4 | DQ2 | 32 | Vss | 60 | DQ24 | 88 | DQ38 | 116 | Vss | 144 | DQ60 |
| 5 | DQ3 | 33 | A0 | 61 | RFU | 89 | DQ39 | 117 | A1 | 145 | RFU |
| 6 | Vcc | 34 | A2 | 62 | RFU | 90 | Vcc | 118 | A3 | 146 | RFU |
| 7 | DQ4 | 35 | A4 | 63 | RFU | 91 | DQ40 | 119 | A5 | 147 | RFU |
| 8 | DQ5 | 36 | A6 | 64 | RFU | 92 | DQ41 | 120 | A7 | 148 | RFU |
| 9 | DQ6 | 37 | A8 | 65 | DQ25 | 93 | DQ42 | 121 | A9 | 149 | DQ61 |
| 10 | DQ7 | 38 | A10 | 66 | *DQ26 | 94 | DQ43 | 122 | A11 | 150 | *DQ62 |
| 11 | *DQ8 | 39 | A12 | 67 | DQ27 | 95 | *DQ44 | 123 | *A13 | 151 | DQ63 |
| 12 | Vss | 40 | Vcc | 68 | Vss | 96 | Vss | 124 | Vcc | 152 | Vss |
| 13 | DQ9 | 41 | RFU | 69 | DQ28 | 97 | DQ45 | 125 | RFU | 153 | DQ64 |
| 14 | DQ10 | 42 | RFU | 70 | DQ29 | 98 | DQ46 | 126 | B0 | 154 | DQ65 |
| 15 | DQ11 | 43 | Vss | 71 | DQ30 | 99 | DQ47 | 127 | Vss | 155 | DQ66 |
| 16 | DQ12 | 44 | $\overline{OE2}$ | 72 | DQ31 | 100 | DQ48 | 128 | RFU | 156 | DQ67 |
| 17 | DQ13 | 45 | $\overline{RAS2}$ | 73 | Vcc | 101 | DQ49 | 129 | $\overline{RAS3}$ | 157 | Vcc |
| 18 | Vcc | 46 | $\overline{CAS4}$ | 74 | DQ32 | 102 | Vcc | 130 | $\overline{CAS5}$ | 158 | DQ68 |
| 19 | DQ14 | 47 | $\overline{CAS6}$ | 75 | DQ33 | 103 | DQ50 | 131 | $\overline{CAS7}$ | 159 | DQ69 |
| 20 | DQ15 | 48 | $\overline{W2}$ | 76 | DQ34 | 104 | DQ51 | 132 | $\overline{PDE}$ | 160 | DQ70 |
| 21 | DQ16 | 49 | Vcc | 77 | *DQ35 | 105 | DQ52 | 133 | Vcc | 161 | *DQ71 |
| 22 | *DQ17 | 50 | RSVD | 78 | Vss | 106 | *DQ53 | 134 | RSVD | 162 | Vss |
| 23 | Vss | 51 | RSVD | 79 | PD1 | 107 | Vss | 135 | RSVD | 163 | PD2 |
| 24 | RSVD | 52 | DQ18 | 80 | PD3 | 108 | RSVD | 136 | DQ54 | 164 | PD4 |
| 25 | RSVD | 53 | DQ19 | 81 | PD5 | 109 | RSVD | 137 | DQ55 | 165 | PD6 |
| 26 | Vcc | 54 | Vss | 82 | PD7 | 110 | Vcc | 138 | Vss | 166 | PD8 |
| 27 | $\overline{W0}$ | 55 | DQ20 | 83 | ID0 | 111 | RFU | 139 | DQ56 | 167 | ID1 |
| 28 | $\overline{CAS0}$ | 56 | DQ21 | 84 | Vcc | 112 | $\overline{CAS1}$ | 140 | DQ57 | 168 | Vcc |

NOTE : A12 is used for only M364C0884BT0-C (8K Ref.)

PD Note :PD & ID Terminals must each be pulled up through a resistor to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

## PIN NAMES

| Pin Names | Function |
|---|---|
| A0, B0, A1 - A11 | Address Input(4K ref.) |
| A0, B0, A1 - A12 | Address Input(8K ref.) |
| DQ0 - DQ71 | Data In/Out |
| $\overline{W0}$, $\overline{W2}$ | Read/Write Enable |
| $\overline{OE0}$, $\overline{OE2}$ | Output Enable |
| $\overline{RAS0}$ - $\overline{RAS3}$ | Row Address Strobe |
| $\overline{CAS0}$ - $\overline{CAS7}$ | Column Address Strobe |
| Vcc | Power(+5V) |
| Vss | Ground |
| NC | No Connection |
| $\overline{PDE}$ | Presence Detect Enable |
| PD1 - 8 | Presence Detect |
| ID0 - 1 | ID bit |
| RSVD | Reserved Use |
| RFU | Reserved for Future |

Pins marked '*' are not used in this module.

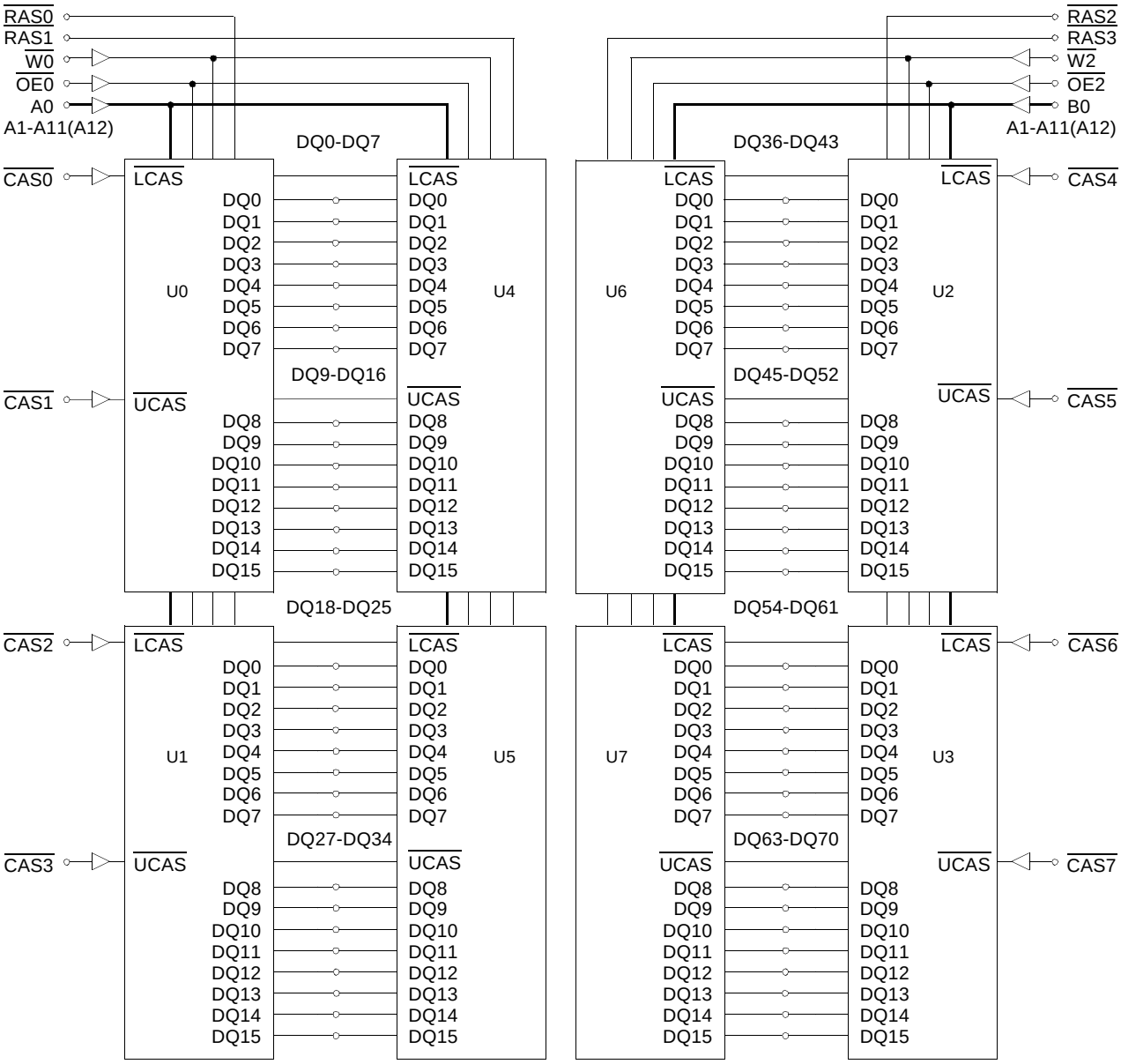
## PD & ID Table

| Pin | 50NS | 60NS |
|---|---|---|
| PD1 | 0 | 0 |
| PD2 | 0 | 0 |
| PD3 | 1 | 1 |
| PD4 | 1 | 1 |
| PD5 | 0 | 0 |
| PD6 | 0 | 1 |
| PD7 | 0 | 1 |
| PD8 | 1 | 1 |
| ID0 | 0 | 0 |
| ID1 | 0 | 0 |

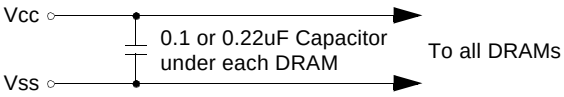
PD : 0 for Vol of Drive IC & 1 for N.C

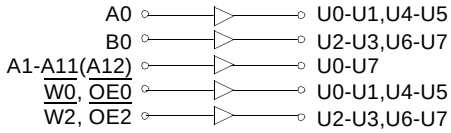
ID : 0 for Vss & 1 for N.C

## FUNCTIONAL BLOCK DIAGRAM




Note : A12 is used for only M364C0884BT (8K ref.)



## ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Voltage on any pin relative $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1 to +7.0 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | -1 to +7.0 | V |
| Storage Temperature | $T_{stg}$ | -55 to +125 | °C |
| Power Dissipation | $P_D$ | 8 | W |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltage referenced to $V_{SS}$, $T_A$ = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.4 | - | $V_{CC}$*1 | V |
| Input Low Voltage | $V_{IL}$ | -1.0*2 | - | 0.8 | V |

*1 : $V_{CC}$+2.0V at pulse width≤20ns, which is measured at $V_{CC}$.

*2 : -2.0V at pulse width≤20ns, which is measured at $V_{SS}$.

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | M364C0804BT0 | | M364C0884BT0 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $I_{CC1}$ | -50<br>-60 | -<br>- | 580<br>540 | -<br>- | 460<br>420 | mA<br>mA |
| $I_{CC2}$ | Don't care | - | 100 | - | 100 | mA |
| $I_{CC3}$ | -50<br>-60 | -<br>- | 580<br>540 | -<br>- | 460<br>420 | mA<br>mA |
| $I_{CC4}$ | -50<br>-60 | -<br>- | 380<br>340 | -<br>- | 340<br>300 | mA<br>mA |
| $I_{CC5}$ | Don't care | - | 30 | - | 30 | mA |
| $I_{CC6}$ | -50<br>-60 | -<br>- | 580<br>540 | -<br>- | 460<br>420 | mA<br>mA |
| $I_{I(L)}$<br>$I_{O(L)}$ | Don't care | -10<br>-10 | 10<br>10 | -10<br>-10 | 10<br>10 | uA<br>uA |
| $V_{OH}$<br>$V_{OL}$ | Don't care | 2.4<br>- | -<br>0.4 | 2.4<br>- | -<br>0.4 | V<br>V |

$I_{CC1}$*: Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @$t_{RC}$=min)

$I_{CC2}$ : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=$V_{IH}$)

$I_{CC3}$*: $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=$V_{IH}$, $\overline{RAS}$ cycling @$t_{RC}$=min)

$I_{CC4}$*: Fast Page Mode Current * ($\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ cycling : $t_{PC}$=min)

$I_{CC5}$ : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vcc-0.2V)

$I_{CC6}$*: $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @$t_{RC}$=min)

$I_{(IL)}$ : Input Leakage Current (Any input 0≤$V_{IN}$≤Vcc+0.5V, all other pins not under test=0 V)

$I_{(OL)}$ : Output Leakage Current(Data Out is disabled, 0V≤$V_{OUT}$≤Vcc)

$V_{OH}$ : Output High Voltage Level ($I_{OH}$ = -5mA)

$V_{OL}$ : Output Low Voltage Level ($I_{OL}$ = 4.2mA)

*** NOTE** : $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. $I_{CC}$ is specified as an average current. In $I_{CC1}$ and $I_{CC3}$, address can be changed maximum once while $\overline{RAS}$=$V_{IL}$. In $I_{CC4}$, address can be changed maximum once within one Fast page mode cycle time, $t_{PC}$.

## CAPACITANCE ($T_A$ = 25°C, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance[A0, B0, A1 - A12] | $C_{IN1}$ | - | 20 | pF |
| Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$] | $C_{IN2}$ | - | 20 | pF |
| Input capacitance[$\overline{RAS0}$ - $\overline{RAS3}$] | $C_{IN3}$ | - | 24 | pF |
| Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$] | $C_{IN4}$ | - | 20 | pF |
| Input/Output capacitance[DQ0 - 71] | $C_{DQ}$ | - | 24 | pF |

## AC CHARACTERISTICS (0°C≤$T_A$≤70°C, $V_{CC}$=5.0V±10%. See notes 1,2.)

Test condition : $V_{ih}/V_{il}$=2.6/0.8V, $V_{oh}/V_{ol}$=2.4/0.4V, output loading CL=100pF

| Parameter | Symbol | -50 | | -60 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | $t_{RC}$ | 90 | | 110 | | ns | |
| Read-modify-write cycle time | $t_{RWC}$ | 133 | | 153 | | ns | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | | 50 | | 60 | ns | 3,4 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | | 18 | | 20 | ns | 3,4,5,11 |
| Access time from column address | $t_{AA}$ | | 25 | | 30 | ns | 3,10,11 |
| $\overline{CAS}$ to output in Low-Z | $t_{CLZ}$ | 0 | | 0 | | ns | 3,11 |
| Output buffer turn-off delay | $t_{OFF}$ | 0 | 13 | 0 | 13 | ns | 6,11 |
| Transition time(rise and fall) | $t_T$ | 1 | 50 | 1 | 50 | ns | 2 |
| $\overline{RAS}$ precharge time | $t_{RP}$ | 30 | | 40 | | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | 50 | 10K | 60 | 10K | ns | |
| $\overline{RAS}$ hold time | $t_{RSH}$ | 13 | | 15 | | ns | 11 |
| $\overline{CAS}$ hold time | $t_{CSH}$ | 50 | | 60 | | ns | 11 |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | 13 | 10K | 15 | 10K | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | 20 | 37 | 20 | 45 | ns | 4,11 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | 15 | 25 | 15 | 30 | ns | 10,11 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | 5 | | 5 | | ns | 11 |
| Row address set-up time | $t_{ASR}$ | 0 | | 0 | | ns | 11 |
| Row address hold time | $t_{RAH}$ | 10 | | 10 | | ns | 11 |
| Column address set-up time | $t_{ASC}$ | 0 | | 0 | | ns | 12 |
| Column address hold time | $t_{CAH}$ | 10 | | 10 | | ns | 12 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | 25 | | 30 | | ns | 11 |
| Read command set-up time | $t_{RCS}$ | 0 | | 0 | | ns | |
| Read command hold referencde to $\overline{CAS}$ | $t_{RCH}$ | 0 | | 0 | | ns | 8 |
| Read command hold referenced to $\overline{RAS}$ | $t_{RRH}$ | 0 | | 0 | | ns | 8,11 |
| Write command hold time | $t_{WCH}$ | 10 | | 10 | | ns | |
| Write command pulse width | $t_{WP}$ | 10 | | 10 | | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | 15 | | 15 | | ns | 11 |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | 13 | | 15 | | ns | 15 |
| Data in set-up time | $t_{DS}$ | 0 | | 0 | | ns | 9,11 |
| Data in hold time | $t_{DH}$ | 10 | | 10 | | ns | 9,11 |
| Refresh period | $t_{REF}$ | | 64 | | 64 | ms | |
| Write command set-up time | $t_{WCS}$ | 0 | | 0 | | ns | 7 |
| $\overline{CAS}$ to $\overline{W}$ delay time | $t_{CWD}$ | 36 | | 38 | | ns | 7,15 |
| Column address to $\overline{W}$ delay time | $t_{AWD}$ | 48 | | 53 | | ns | 7 |
| $\overline{CAS}$ prechange to $\overline{W}$ delay time | $t_{CPWD}$ | 53 | | 60 | | ns | 7 |

## AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

| Parameter | Symbol | -50 | | -60 | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $\overline{RAS}$ ro $\overline{W}$ delay time | $t_{RWD}$ | 73 | | 83 | | ns | 7,11 |
| $\overline{CAS}$ setup time($\overline{CAS}$-before-$\overline{RAS}$ refresh) | $t_{CSR}$ | 5 | | 5 | | ns | 11,16 |
| $\overline{CAS}$ hold time($\overline{CAS}$-before-$\overline{RAS}$ refresh) | $t_{CHR}$ | 10 | | 10 | | ns | 11 |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | $t_{RPC}$ | 5 | | 5 | | ns | 11 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | | 30 | | 35 | ns | 3,11 |
| Fast page mode cycle time | $t_{PC}$ | 35 | | 40 | | ns | |
| Fast page mode read-modify-write cycle time | $t_{PRWC}$ | 76 | | 85 | | ns | |
| $\overline{CAS}$ precharge time(Fast page cycle) | $t_{CP}$ | 10 | | 10 | | ns | 13 |
| $\overline{RAS}$ pulse width(Fast page cycle) | $t_{RASP}$ | 50 | 200K | 60 | 200K | ns | |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{RHCP}$ | 30 | | 35 | | ns | 11 |
| $\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh) | $t_{WRP}$ | 10 | | 10 | | ns | 11 |
| $\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh) | $t_{WRH}$ | 10 | | 10 | | ns | 11 |
| $\overline{OE}$ access time | $t_{OEA}$ | | 13 | | 15 | ns | 11 |
| $\overline{OE}$ to data delay | $t_{OED}$ | 13 | | 13 | | ns | 11 |
| Output buffer turn off delay time from $\overline{OE}$ | $t_{OEZ}$ | 0 | 13 | 0 | 13 | ns | 11 |
| $\overline{OE}$ command hold time | $t_{OEH}$ | 13 | | 15 | | ns | |
| **Present Detect Read Cycle** | | | | | | | |
| $\overline{PDE}$ to Valid PD bit | $t_{PD}$ | | 10 | | 10 | ns | |
| $\overline{PDE}$ to PD bit Inactive | $t_{PDOFF}$ | 2 | 7 | 2 | 7 | ns | |

## NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are $V_{ih}/V_{il}$. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min) and $V_{IL}$(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 2 TTL loads and 100pF.

4. Operation within the $t_{RCD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RCD}$(max) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max) limit, then access time is controlled exclusively by $t_{CAC}$.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.

7. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min) and $t_{CPWD} \geq t_{CPWD}$(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.

8. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.

10. Operation within the $t_{RAD}$(max) limit insures that $t_{RAC}$(max) can be met. $t_{RAD}$(max) is specified as reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$(max) limit, then access time is controlled by $t_{AA}$.

11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

12. $t_{ASC}$, $t_{CAH}$ are referenced to the earlier $\overline{CAS}$ falling edge.

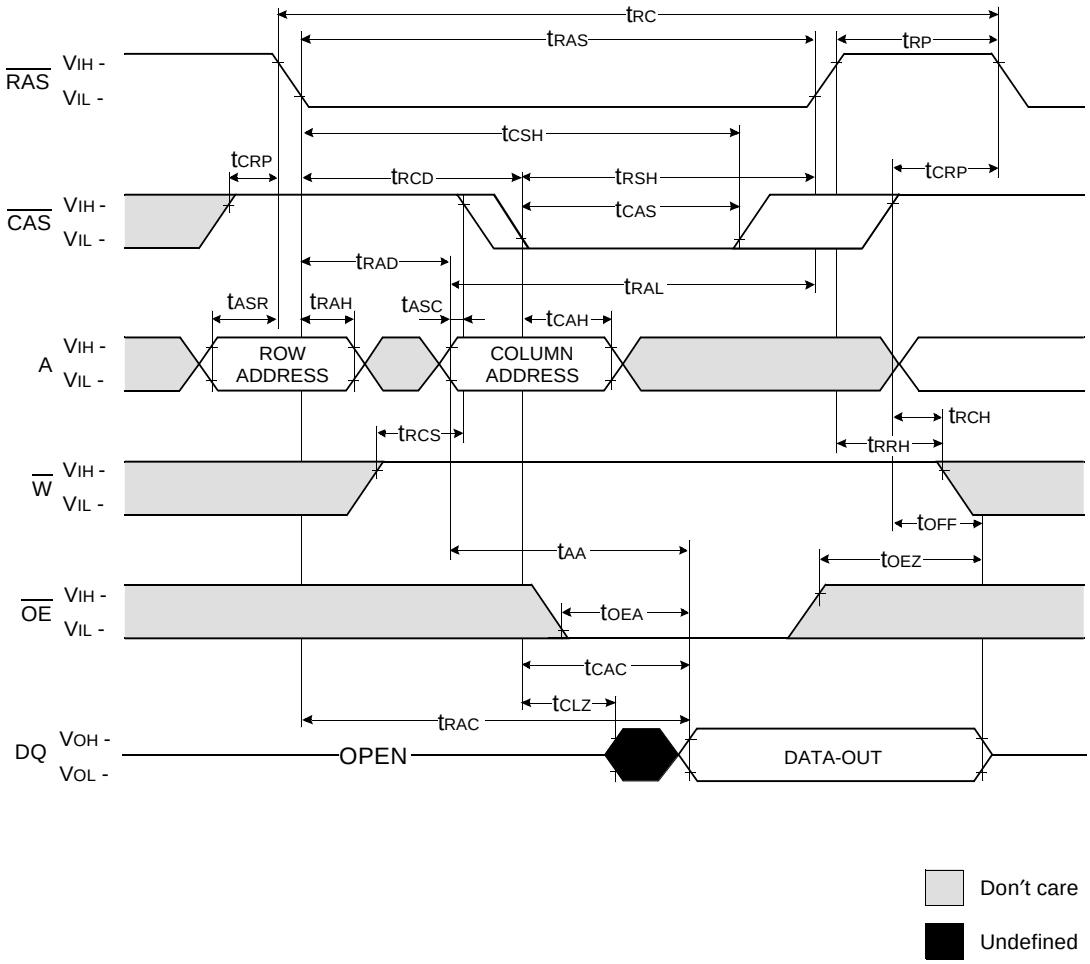
13. $t_{CP}$ is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

14. $t_{CWD}$ is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

15. $t_{CWL}$ is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

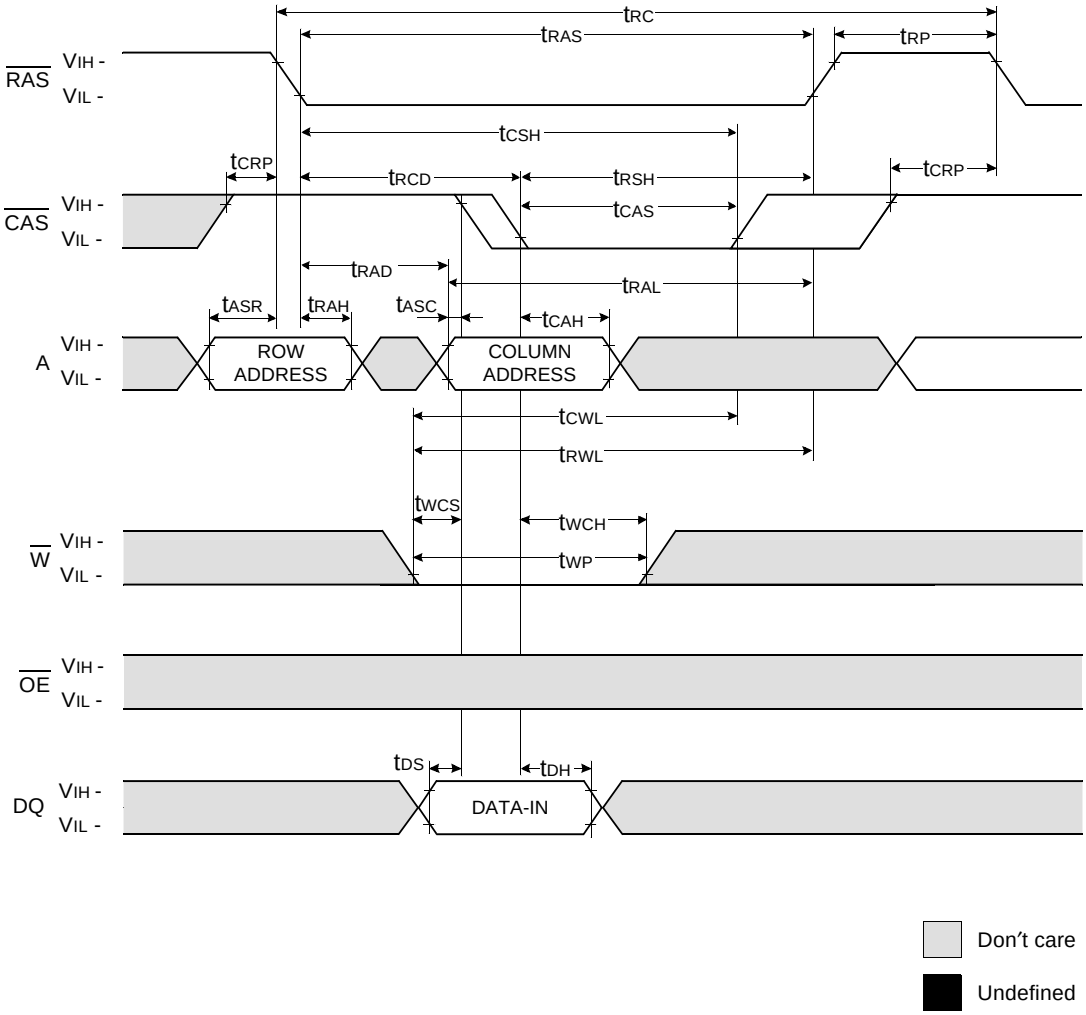
16. $t_{CSR}$ is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

### READ CYCLE



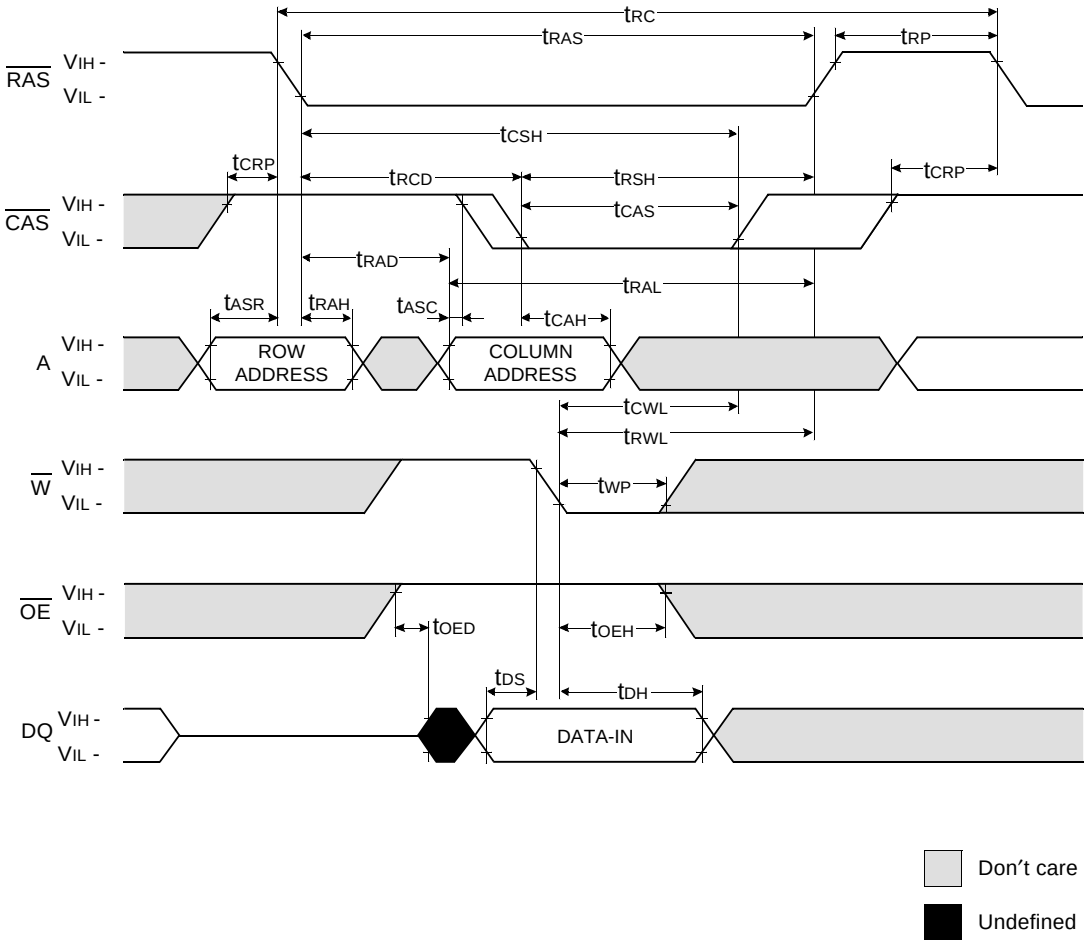
### WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

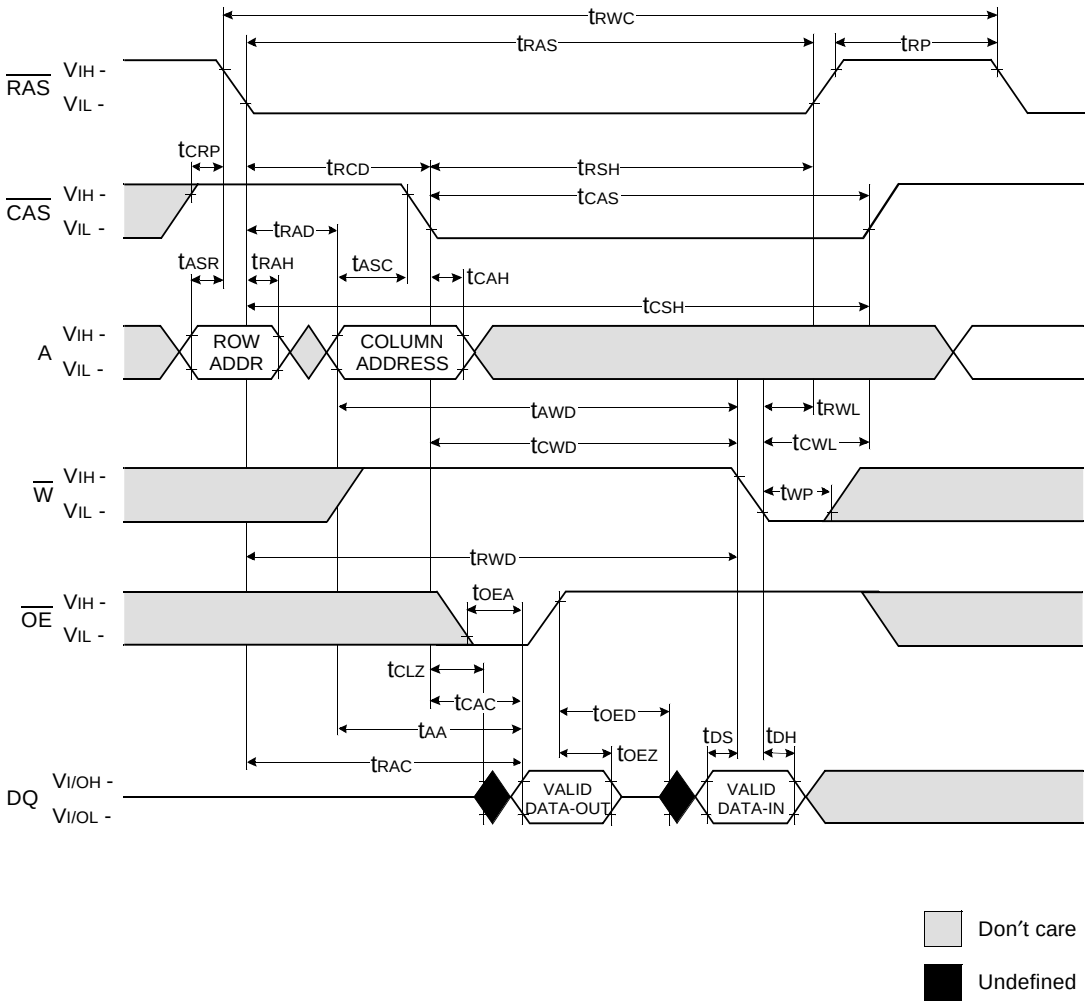


### WRITE CYCLE ( $\overline{OE}$ CONTROLLED WRITE )

NOTE : DOUT = OPEN

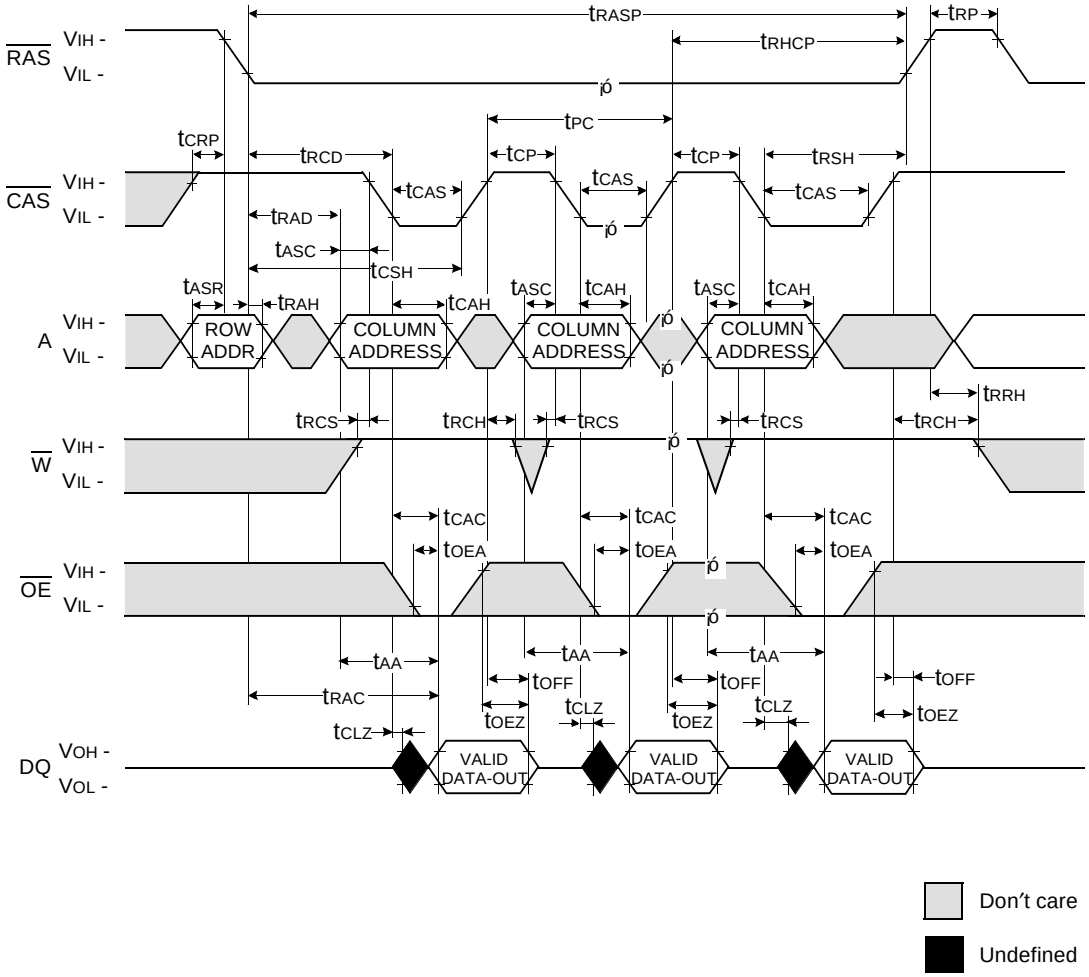


### READ - MODIFY - WRTIE CYCLE



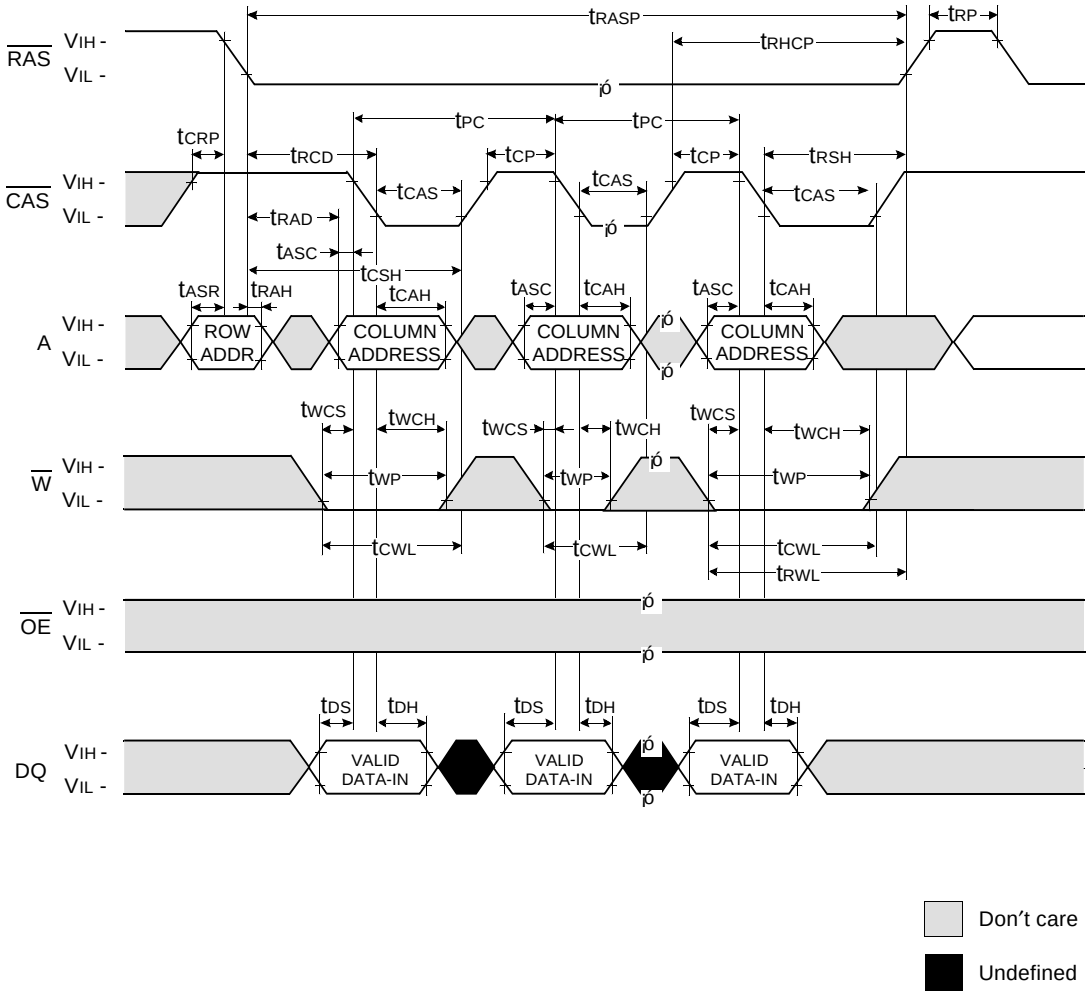
### FAST PAGE READ CYCLE

NOTE : DOUT = OPEN

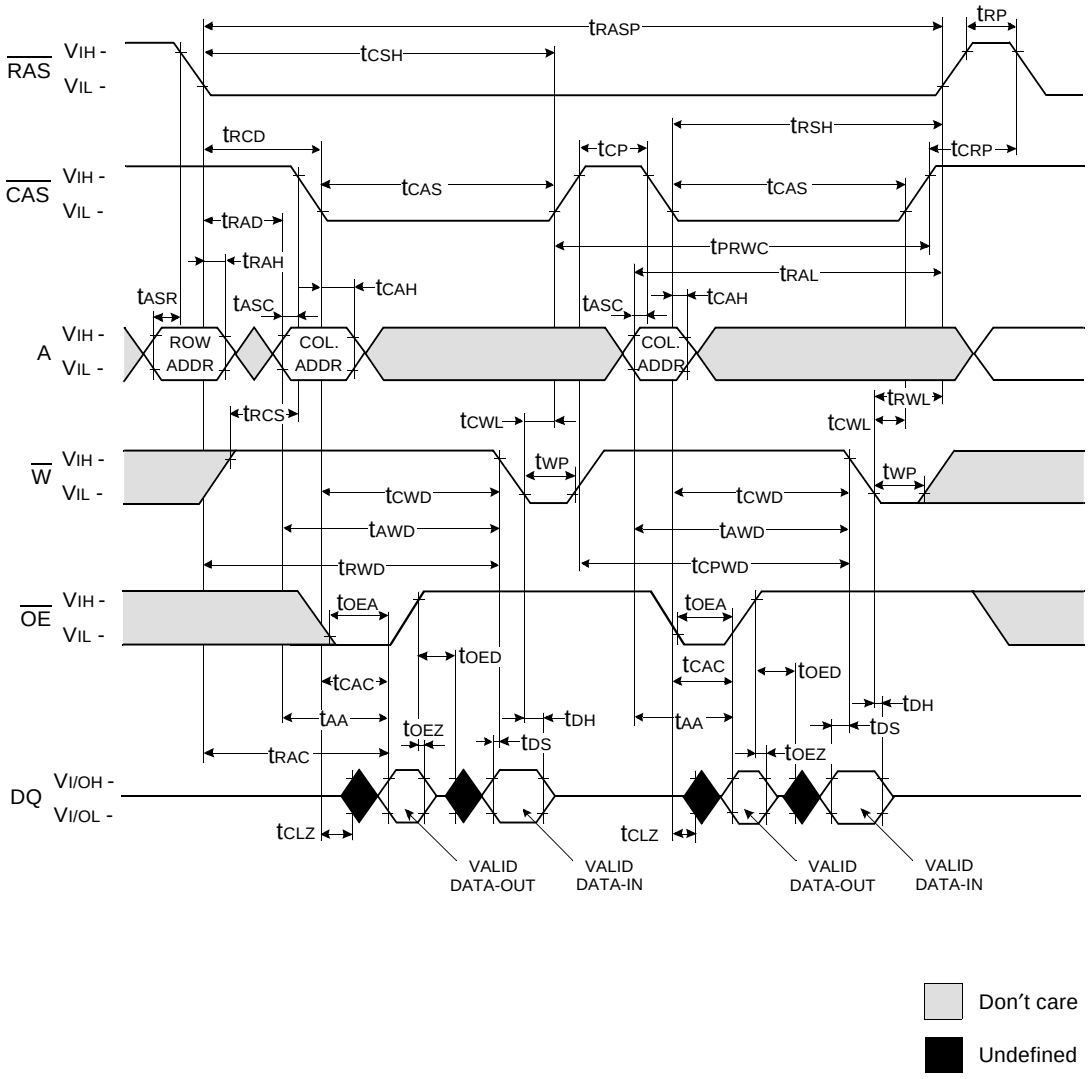


## FAST PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



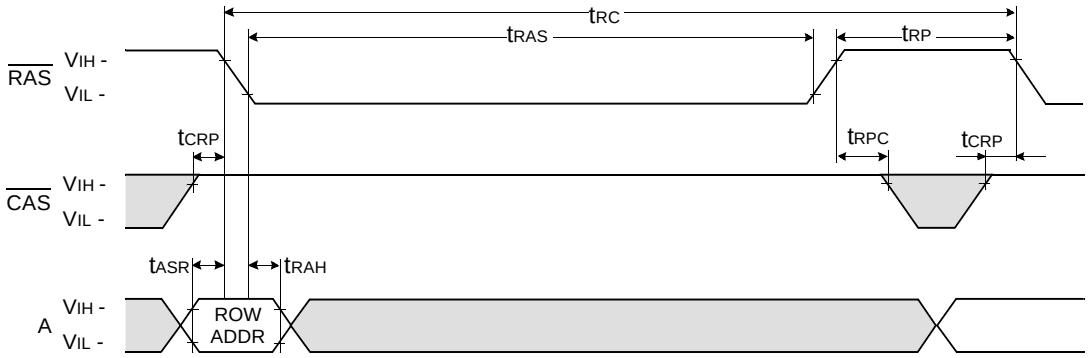
## FAST PAGE READ - MODIFY - WRITE CYCLE



## $\overline{RAS}$ - ONLY REFRESH CYCLE

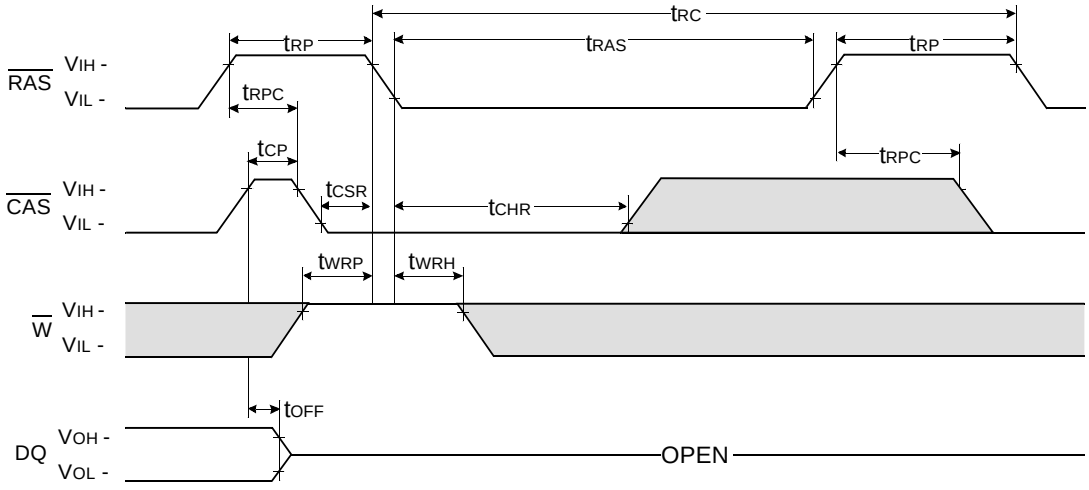
NOTE : $\overline{W}$, $\overline{OE}$, $D_{IN}$ = Don't care

$D_{OUT}$ = OPEN

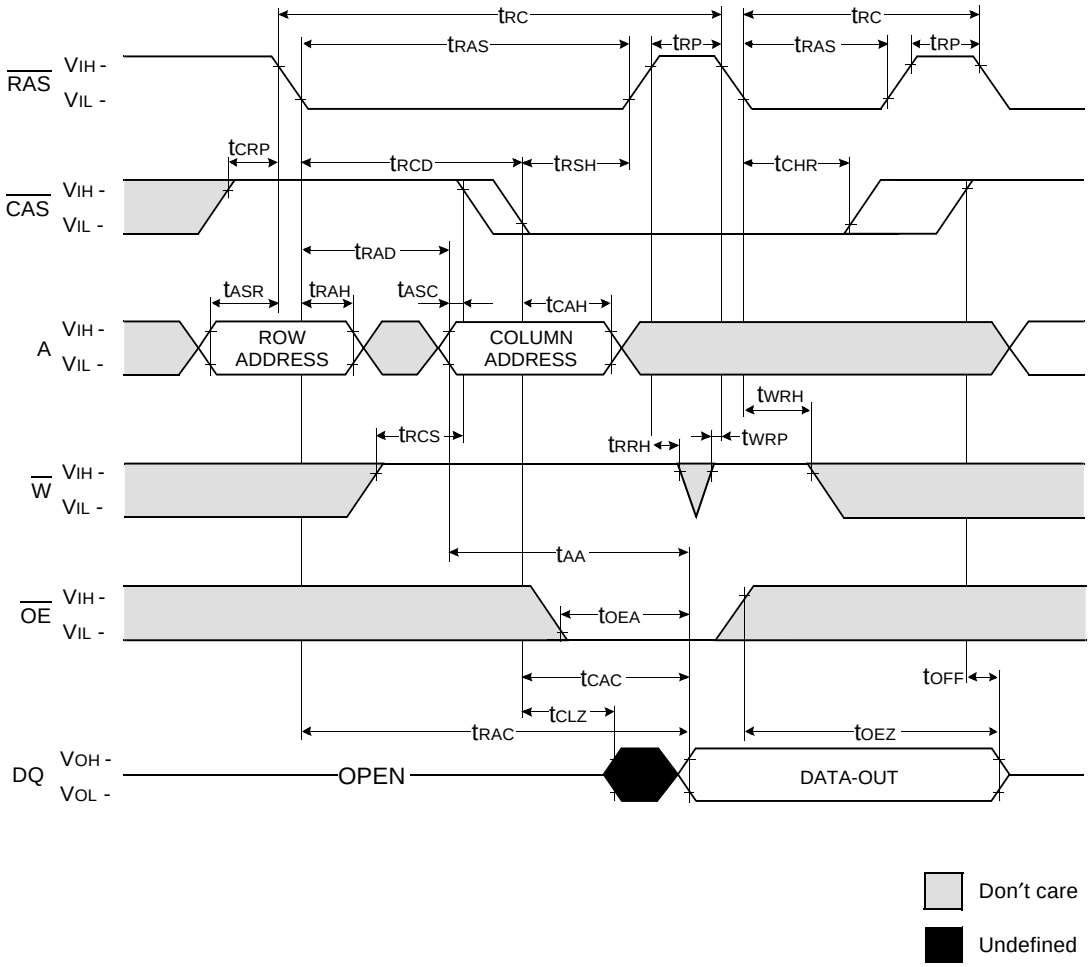



## $\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care

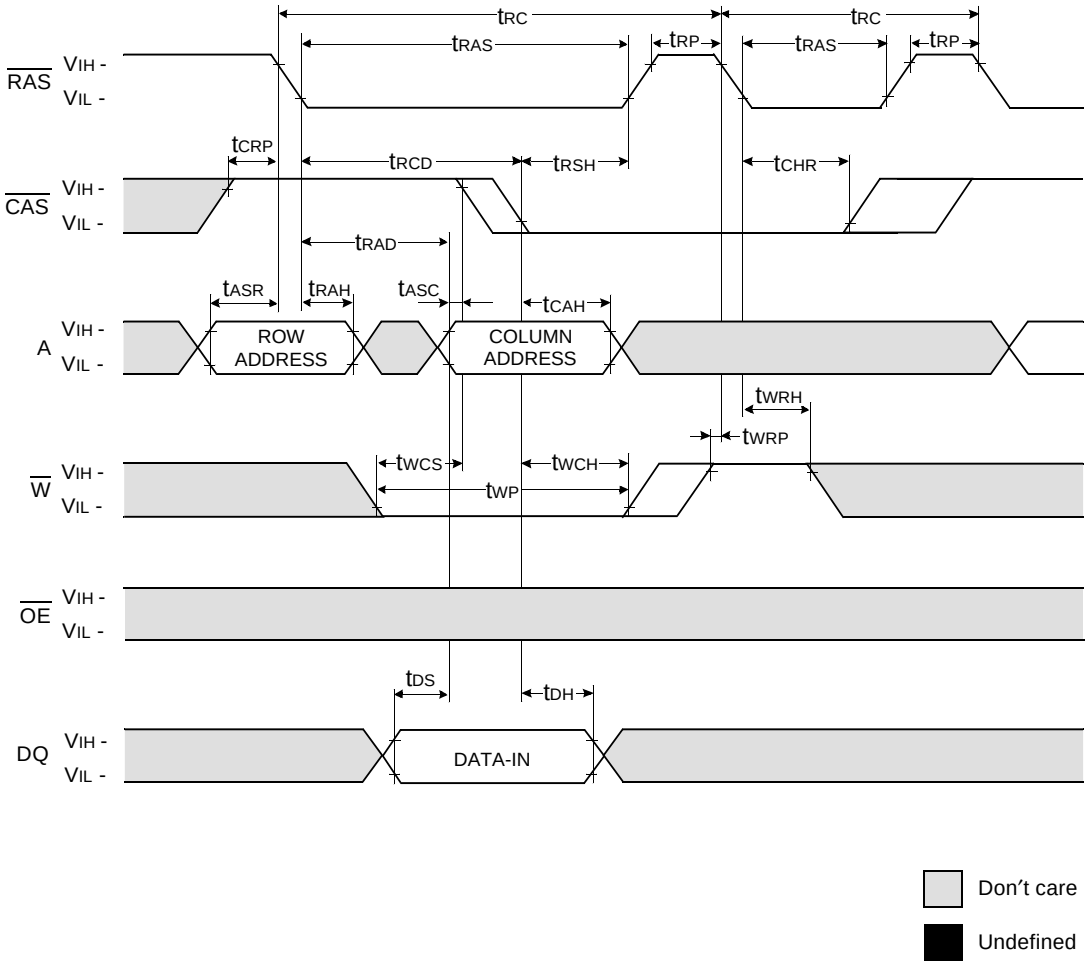


### HIDDEN REFRESH CYCLE ( READ )

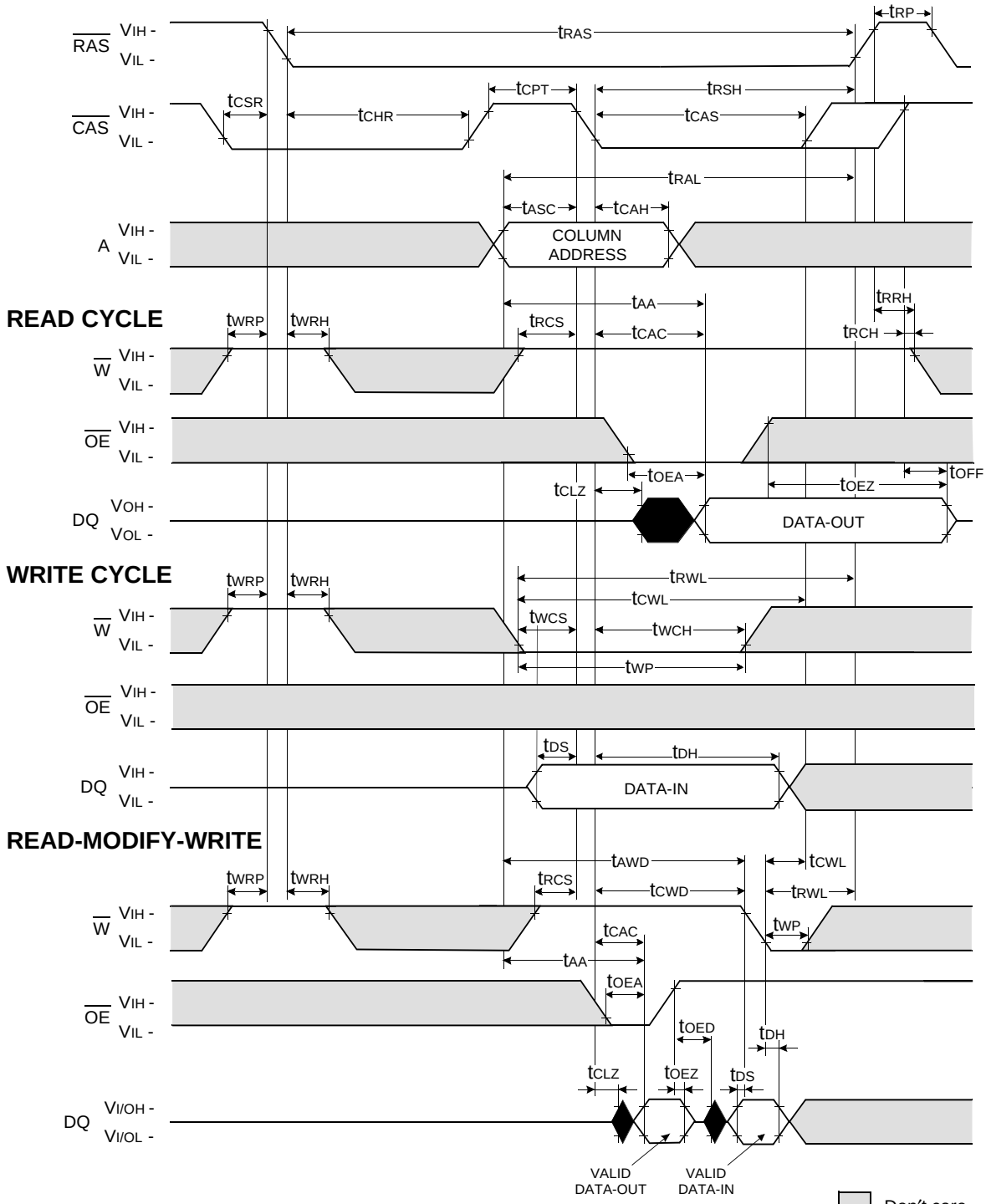


### HIDDEN REFRESH CYCLE ( WRITE )

NOTE : DOUT = OPEN



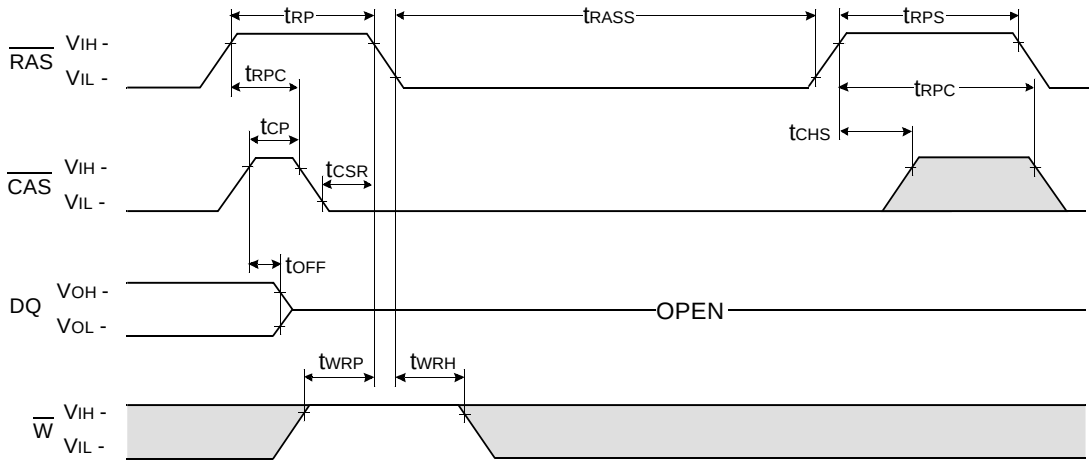
## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE




NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

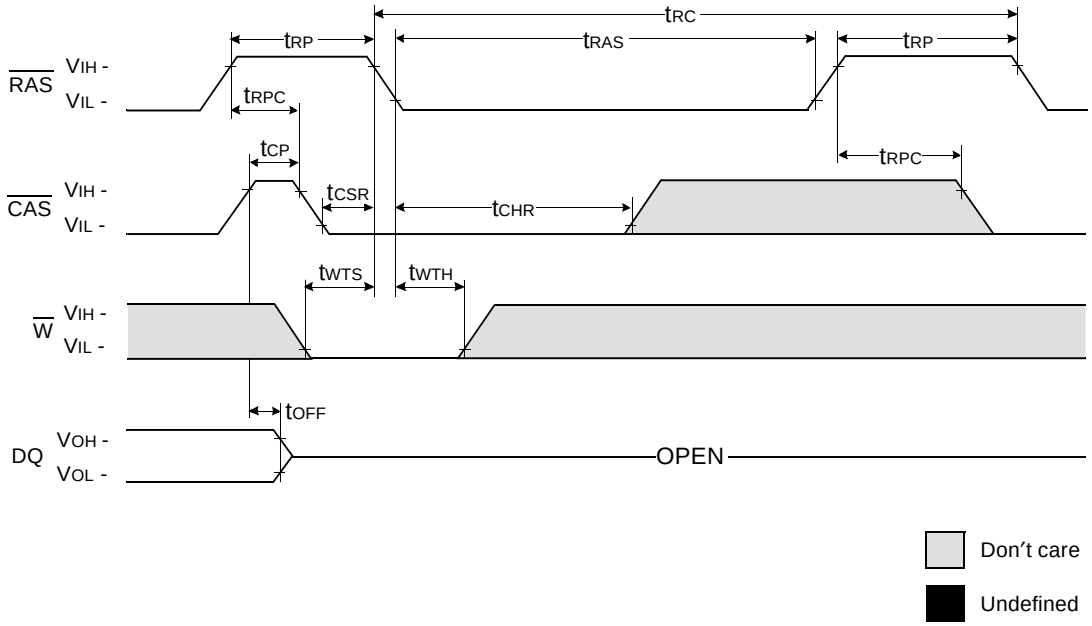
## $\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't care



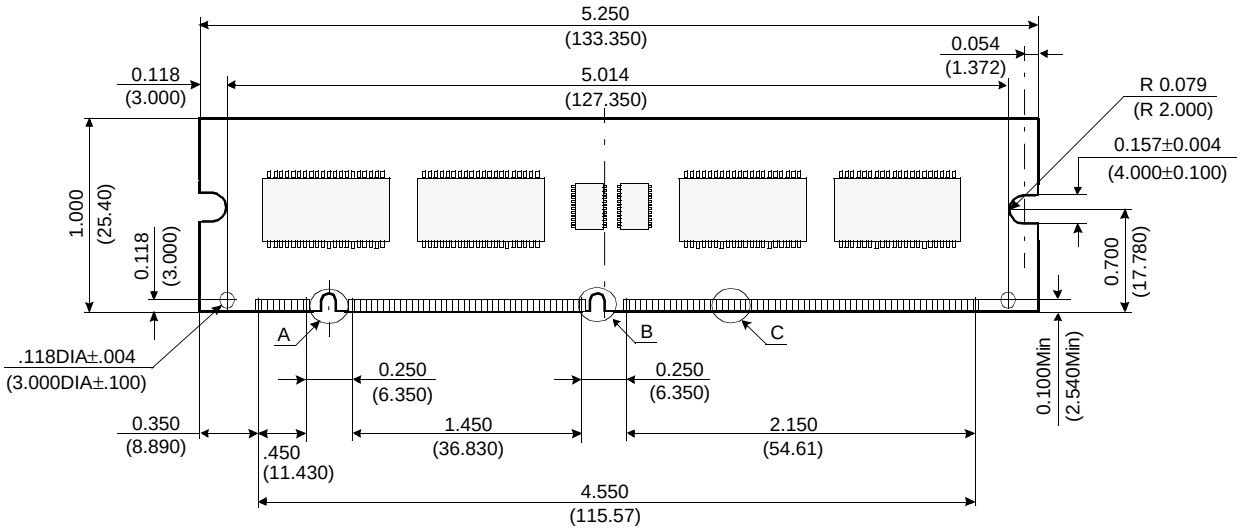

## TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't care

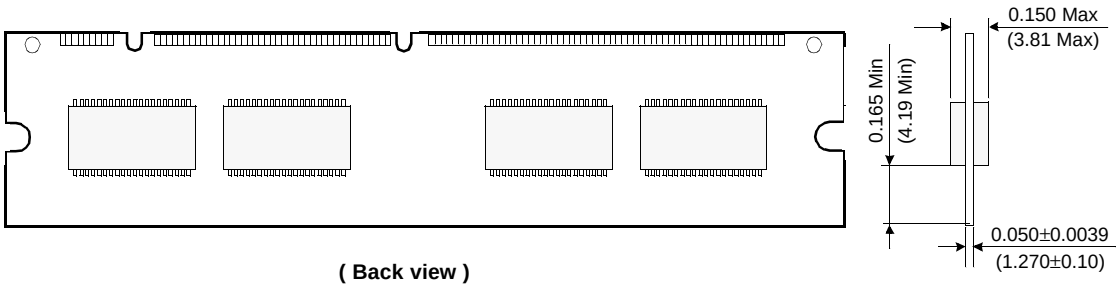


## PACKAGE DIMENSIONS

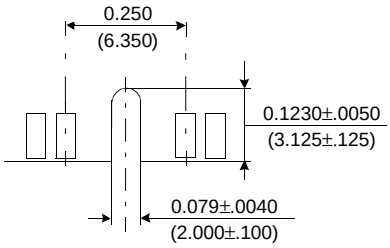
Units : Inches (millimeters)



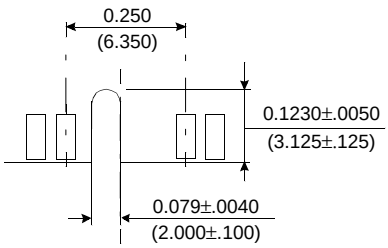

**( Front view )**



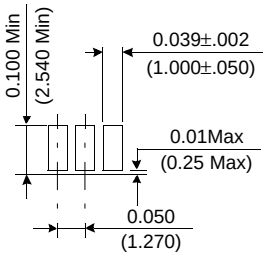

**( Back view )**




**Detail A**




**Detail B**




**Detail C**

Tolerances :±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with Fast page mode, TSOP II.
DRAM Part No. : M364C0804BT0 - K4F641611B
M364C0884BT0 - K4F661611B