

**M366S2953MTS**

**PC133/PC100 Unbuffered DIMM**

**M366S2953MTS SDRAM DIMM**

128Mx64 SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

**GENERAL DESCRIPTION**

The Samsung M366S2953MTS is a 64M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M366S2953MTS consists of sixteen CMOS 64M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM.

The M366S2953MTS is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

**FEATURE**

- Performance range

Part No.	Max Freq. (Speed)
M366S2953MTS-C75	133MHz@CL=3
M366S3953MTS-C1H	100MHz @ CL=2
M366S2953MTS-C1L	100MHz @ CL=3

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs  
Latency (Access from column address)  
Burst length (1, 2, 4, 8 & Full page)  
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,375mil)**, double sided component

**PIN CONFIGURATIONS (Front side/back side)**

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	CS1
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss
5	DQ3	33	A0	61	NC	89	DQ35	117	A1
6	VDD	34	A2	62	*VREF	90	VDD	118	A3
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0
17	DQ13	45	CS2	73	VDD	101	DQ45	129	CS3
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC
23	Vss	51	NC	79	CLK2	107	Vss	135	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6
25	NC	53	*CB3	81	*WP	109	NC	137	*CB7
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49

**PIN NAMES**

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK3	Clock input
CKE0 ~ CKE1	Clock enable input
CS0 ~ CS3	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
*WP	Write protection
DU	Don't use
NC	No connection

\* These pins are not used in this module.  
\*\* These pins should be NC in the system which does not support SPD.

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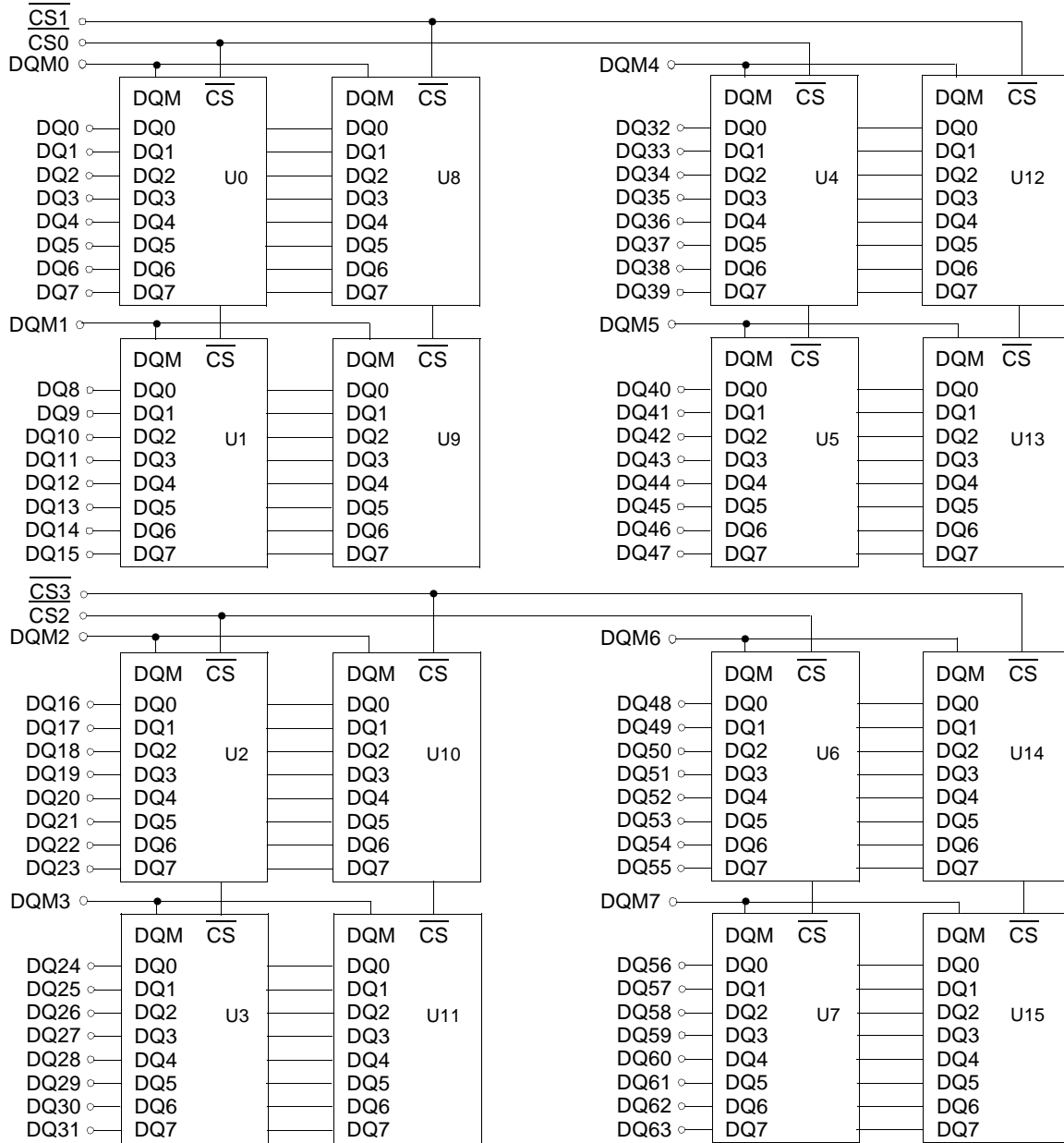
**PIN CONFIGURATION DESCRIPTION**

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM.
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9,CA11
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

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**FUNCTIONAL BLOCK DIAGRAM**



A0 ~ An, BA0 & 1 → SDRAM U0 ~ U15

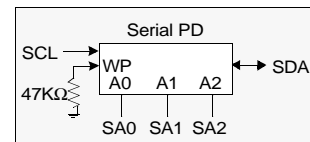
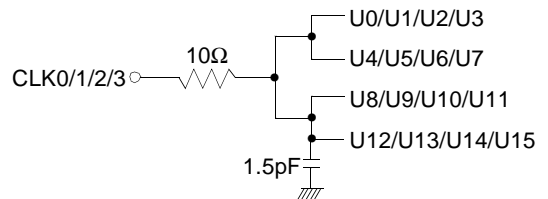
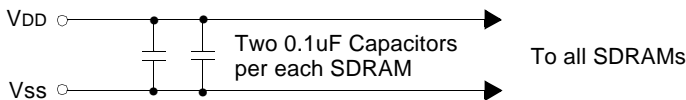
RAS → SDRAM U0 ~ U15

CAS → SDRAM U0 ~ U15

WE → SDRAM U0 ~ U15

CKE0 → SDRAM U0 ~ U7     CKE1 → SDRAM U8 ~ U15

DQn  $\xrightarrow{10\Omega}$  Every DQpin of SDRAM



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### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	16	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

### DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub> , V <sub>DDQ</sub>	3.0	3.3	3.6	V	
Input logic high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input logic low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output logic high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output logic low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current	I <sub>LI</sub>	-10	-	10	uA	3

**Notes :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

### CAPACITANCE (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C <sub>ADD</sub>	80	100	pF
RAS, CAS, WE	C <sub>IN</sub>	80	100	pF
CKE (CKE0 ~ CKE1)	C <sub>CKE</sub>	50	60	pF
Clock (CLK0 ~ CLK3)	C <sub>CLK</sub>	40	45	pF
CS (CS0, CS2)	C <sub>CS</sub>	25	35	pF
DQM (DQM0 ~ DQM7)	C <sub>DQM</sub>	15	20	pF
DQ (DQ0 ~ DQ63)	C <sub>OUT</sub>	10	15	pF

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**DC CHARACTERISTICS**

(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version			Unit	Note
			-75	-1H	-1L		
Operating current (One bank active)	ICC1	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC</sub> (min) I <sub>O</sub> = 0 mA	2000	1840		mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns	95			mA	
	ICC2PS	CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞	80				
Precharge standby current in non power-down mode	ICC2N	CKE ≥ V <sub>IH</sub> (min), $\overline{CS}$ ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	480			mA	
	ICC2NS	CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞ Input signals are stable	160				
Active standby current in power-down mode	ICC3P	CKE ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = 10ns	160			mA	
	ICC3PS	CKE & CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞	130				
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ V <sub>IH</sub> (min), $\overline{CS}$ ≥ V <sub>IH</sub> (min), t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	800			mA	
	ICC3NS	CKE ≥ V <sub>IH</sub> (min), CLK ≤ V <sub>IL</sub> (max), t <sub>CC</sub> = ∞ Input signals are stable	560				
Operating current (Burst mode)	ICC4	I <sub>O</sub> = 0 mA Page burst 4banks Activated. t <sub>CCD</sub> = 2CLKs	2000	1760		mA	1
Refresh current	ICC5	t <sub>RC</sub> ≥ t <sub>RC</sub> (min)	3040	2880		mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	112			mA	
						mA	

**Notes :**

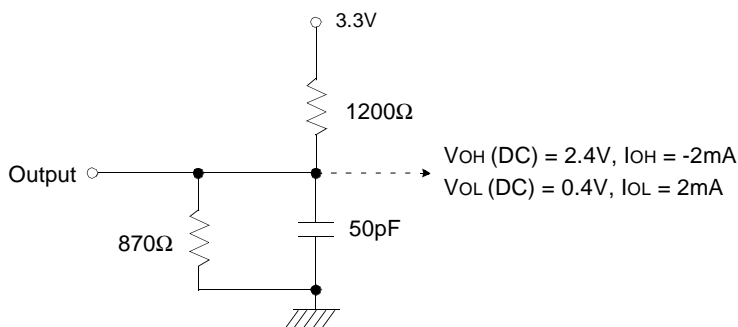
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noticed, input swing level is CMOS(V<sub>IH</sub>/V<sub>IL</sub>=V<sub>DDQ</sub>/V<sub>SSQ</sub>).

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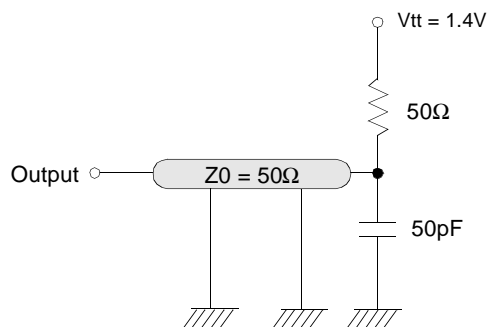
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**AC OPERATING TEST CONDITIONS** ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^{\circ}C$ )

Parameter	Value	Unit
AC input levels ( $V_{ih}/V_{il}$ )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-75	-1H	-1L		
Row active to row active delay	$t_{RRD}(\min)$	15	20	20	ns	1
RAS to CAS delay	$t_{RCD}(\min)$	20	20	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	20	20	ns	1
Row active time	$t_{RAS}(\min)$	45	50	50	ns	1
	$t_{RAS}(\max)$	100			us	
Row cycle time	$t_{RC}(\min)$	65	70	70	ns	1
Last data in to row precharge	$t_{RD}(\min)$	2			CLK	2, 5
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + $t_{RP}$			-	5
Last data in to new col. address delay	$t_{CDL}(\min)$	1			CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1			CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	-	1			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.
  5. In 100MHz and below 100MHz operating conditions,  $t_{RD} = 1CLK$  and  $t_{DAL} = 1CLK + 20ns$  is also supported. SAMSUNG recommends  $t_{RD} = 2CLK$  and  $t_{DAL} = 2CLK + t_{RP}$ .

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**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)

**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		-1H		-1L		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		10		12			
CLK to valid output delay	CAS latency=3	tSAC		5.4		6		6	ns	1,2
	CAS latency=2			-		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		ns	2
	CAS latency=2		-		3		3			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	1.5		2		2		ns	3
Input hold time		tSH	0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		6		6	ns	
	CAS latency=2			-		6		7		

- Notes :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
  - Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2-1]ns$  should be added to the parameter.

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**SIMPLIFIED TRUTH TABLE**

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A12, A11 A9 ~ A0	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3
	Self refresh		Entry									L
		Exit	H	L	H	H	H	X	X			3
	H			X	X	X	3					
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A9,A11)	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A9,A11)	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
Precharge power down mode	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	V	V	V					
DQM		H	X					V	X		7	
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :** 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

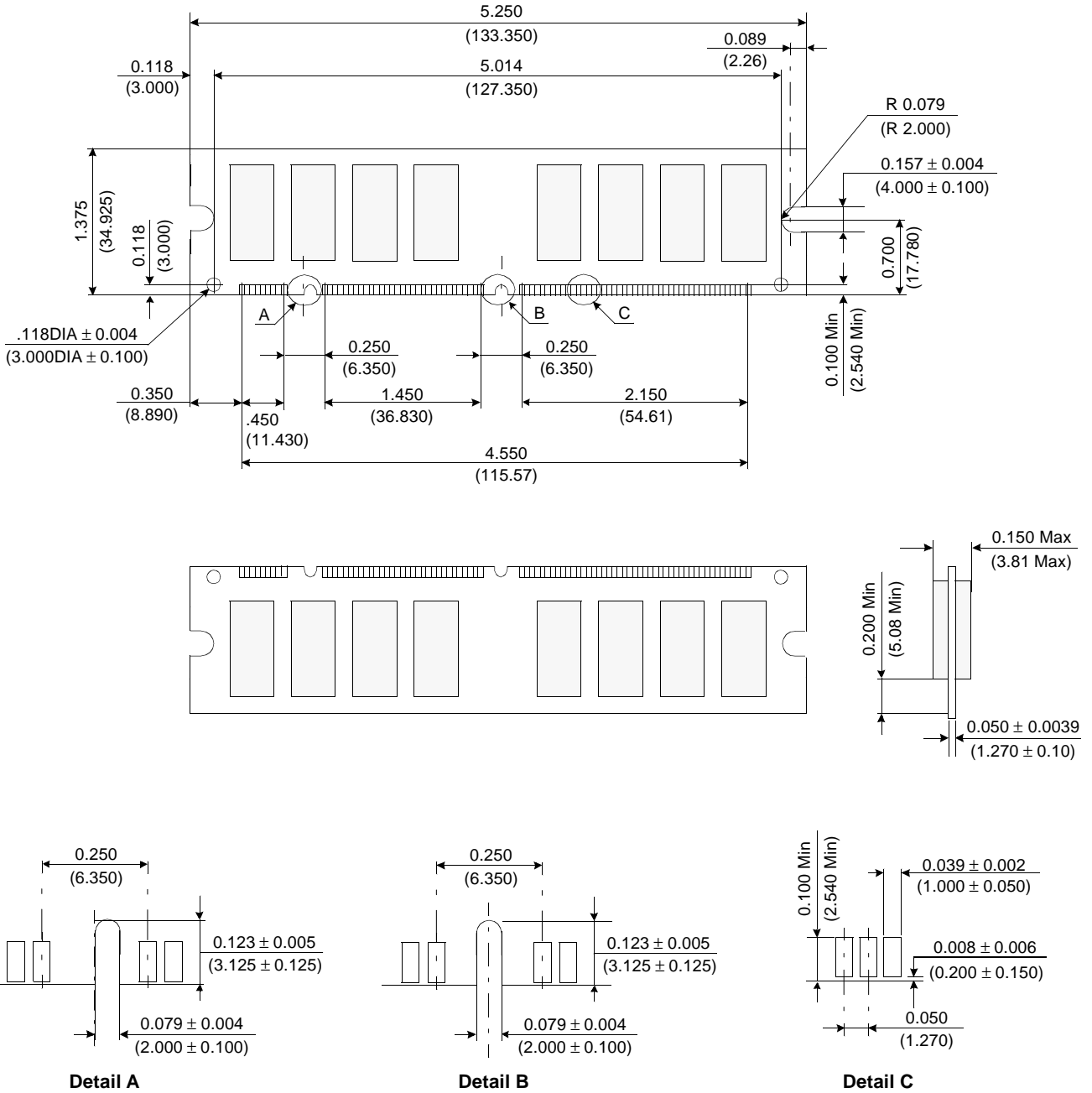


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**PACKAGE DIMENSIONS**

Units : Inches (Millimeters)



Tolerances : ± .005(.13) unless otherwise specified

The used device is 64Mx8 SDRAM, TSOP  
SDRAM Part No. :K4S510832M