

DRAM MODULE

M372F080(8)3DJ(T)0-C

M372F080(8)3DJ(T)0-C EDO Mode

8M x 72 DRAM DIMM with ECC Using 8Mx8, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung M372F080(8)3DJ(T)0-C is a 8Mx72bits Dynamic RAM high density memory module. The Samsung M372F080(8)3DJ(T)0-C consists of nine CMOS 8Mx8bits DRAMs in SOJ/TSOP-II 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M372F080(8)3DJ(T)0-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

| Speed | t _{TRAC} | t _{CAC} | t _{RC} | t _{HPC} |
|-------|-------------------|------------------|-----------------|------------------|
| -C50 | 50ns | 18ns | 84ns | 20ns |
| -C60 | 60ns | 20ns | 104ns | 25ns |

FEATURES

- Part Identification

| Part number | PKG | Ref. | CBR Ref. | ROR Ref. |
|----------------|------|------|----------|----------|
| M372F0803DJ0-C | SOJ | 4K | 4K/64ms | |
| M372F0803DT0-C | TSOP | | | |
| M372F0883DJ0-C | SOJ | 8K | 4K/64ms | 8K/64ms |
| M372F0883DT0-C | TSOP | | | |

- Extended Data Out Mode Operation
- CAS-before-RAS Refresh capability
- RAS-only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except RAS and DQ
- PCB : Height(1250mil), single sided component

PIN CONFIGURATIONS

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|-------|-----|-------|-----|-------|-----|-------|-----|-------|-----|------|
| 1 | Vss | 29 | *CAS2 | 57 | DQ22 | 85 | Vss | 113 | *CAS3 | 141 | DQ58 |
| 2 | DQ0 | 30 | RAS0 | 58 | DQ23 | 86 | DQ36 | 114 | *RAS1 | 142 | DQ59 |
| 3 | DQ1 | 31 | OE0 | 59 | Vcc | 87 | DQ37 | 115 | RFU | 143 | Vcc |
| 4 | DQ2 | 32 | Vss | 60 | DQ24 | 88 | DQ38 | 116 | Vss | 144 | DQ60 |
| 5 | DQ3 | 33 | A0 | 61 | RFU | 89 | DQ39 | 117 | A1 | 145 | RFU |
| 6 | Vcc | 34 | A2 | 62 | RFU | 90 | Vcc | 118 | A3 | 146 | RFU |
| 7 | DQ4 | 35 | A4 | 63 | RFU | 91 | DQ40 | 119 | A5 | 147 | RFU |
| 8 | DQ5 | 36 | A6 | 64 | RFU | 92 | DQ41 | 120 | A7 | 148 | RFU |
| 9 | DQ6 | 37 | A8 | 65 | DQ25 | 93 | DQ42 | 121 | A9 | 149 | DQ61 |
| 10 | DQ7 | 38 | A10 | 66 | DQ26 | 94 | DQ43 | 122 | A11 | 150 | DQ62 |
| 11 | DQ8 | 39 | A12 | 67 | DQ27 | 95 | DQ44 | 123 | *A13 | 151 | DQ63 |
| 12 | Vss | 40 | Vcc | 68 | Vss | 96 | Vss | 124 | Vcc | 152 | Vss |
| 13 | DQ9 | 41 | RFU | 69 | DQ28 | 97 | DQ45 | 125 | RFU | 153 | DQ64 |
| 14 | DQ10 | 42 | RFU | 70 | DQ29 | 98 | DQ46 | 126 | B0 | 154 | DQ65 |
| 15 | DQ11 | 43 | Vss | 71 | DQ30 | 99 | DQ47 | 127 | Vss | 155 | DQ66 |
| 16 | DQ12 | 44 | OE2 | 72 | DQ31 | 100 | DQ48 | 128 | RFU | 156 | DQ67 |
| 17 | DQ13 | 45 | RAS2 | 73 | Vcc | 101 | DQ49 | 129 | *RAS3 | 157 | Vcc |
| 18 | Vcc | 46 | CAS4 | 74 | DQ32 | 102 | Vcc | 130 | *CAS5 | 158 | DQ68 |
| 19 | DQ14 | 47 | *CAS6 | 75 | DQ33 | 103 | DQ50 | 131 | *CAS7 | 159 | DQ69 |
| 20 | DQ15 | 48 | W2 | 76 | DQ34 | 104 | DQ51 | 132 | PDE | 160 | DQ70 |
| 21 | DQ16 | 49 | Vcc | 77 | DQ35 | 105 | DQ52 | 133 | Vcc | 161 | DQ71 |
| 22 | DQ17 | 50 | RSVD | 78 | Vss | 106 | DQ53 | 134 | RSVD | 162 | Vss |
| 23 | Vss | 51 | RSVD | 79 | PD1 | 107 | Vss | 135 | RSVD | 163 | PD2 |
| 24 | RSVD | 52 | DQ18 | 80 | PD3 | 108 | RSVD | 136 | DQ54 | 164 | PD4 |
| 25 | RSVD | 53 | DQ19 | 81 | PD5 | 109 | RSVD | 137 | DQ55 | 165 | PD6 |
| 26 | Vcc | 54 | Vss | 82 | PD7 | 110 | Vcc | 138 | Vss | 166 | PD8 |
| 27 | W0 | 55 | DQ20 | 83 | ID0 | 111 | RFU | 139 | DQ56 | 167 | ID1 |
| 28 | CAS0 | 56 | DQ21 | 84 | Vcc | 112 | *CAS1 | 140 | DQ57 | 168 | Vcc |

NOTE : A12 is used for only M372F0883DJ0/DT0-C (8K Ref.)

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher

level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

| Pin Names | Function |
|------------------|-------------------------|
| A0, B0, A1 - A11 | Address Input(4K ref.) |
| A0, B0, A1 - A12 | Address Input(8K ref.) |
| DQ0 - DQ71 | Data In/Out |
| W0, W2 | Read/Write Enable |
| OE0, OE2 | Output Enable |
| RAS0, RAS2 | Row Address Strobe |
| CAS0, CAS4 | Column Address Strobe |
| Vcc | Power(+3.3V) |
| Vss | Ground |
| NC | No Connection |
| PDE | Presence Detect Enable |
| PD1 - 8 | Presence Detect |
| ID0 - 1 | ID bit |
| RSVD | Reserved Use |
| RFU | Reserved for Future Use |

Pins marked '*' are not used in this module.

PD & ID Table

| Pin | 50NS | 60NS |
|-----|------|------|
| PD1 | 1 | 1 |
| PD2 | 0 | 0 |
| PD3 | 1 | 1 |
| PD4 | 1 | 1 |
| PD5 | 1 | 1 |
| PD6 | 0 | 1 |
| PD7 | 0 | 1 |
| PD8 | 0 | 0 |
| ID0 | 0 | 0 |
| ID1 | 0 | 0 |

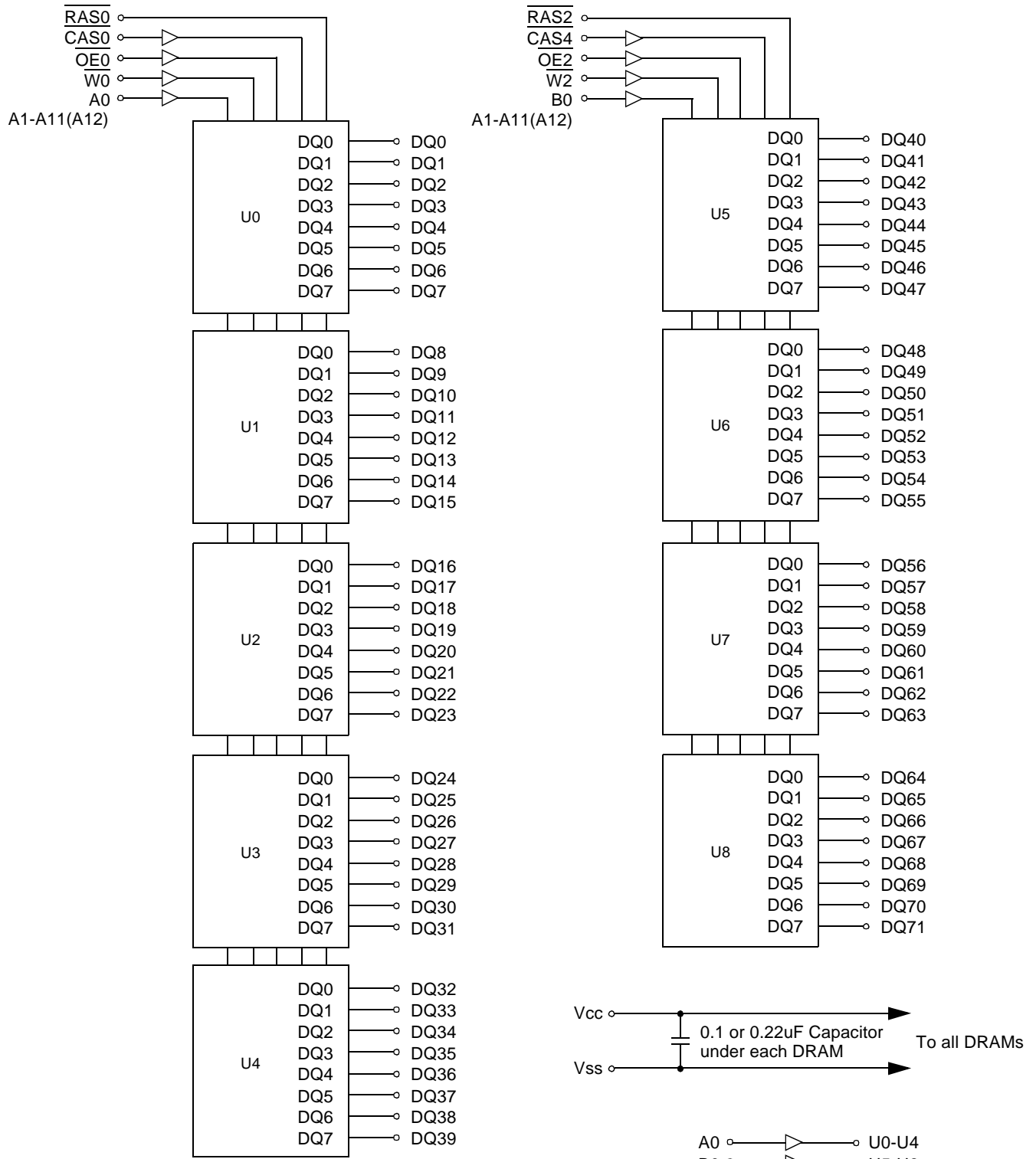
PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

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FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only M372F0883DJ0/DT0 (8K Ref.)

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ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---------------------------------------|------------------------------------|--------------|------|
| Voltage on any pin relative Vss | V _{IN} , V _{OUT} | -0.5 to +4.6 | V |
| Voltage on Vcc supply relative to Vss | V _{CC} | -0.5 to +4.6 | V |
| Storage Temperature | T _{stg} | -55 to +125 | °C |
| Power Dissipation | P _D | 9 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to VSS, TA = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------|-----|------------------------------------|------|
| Supply Voltage | V _{CC} | 3.0 | 3.3 | 3.6 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.0 | - | V _{CC} +0.3 ^{*1} | V |
| Input Low Voltage | V _{IL} | -0.3 ^{*2} | - | 0.8 | V |

*1 : V_{CC}+1.3V at pulse width ≤ 15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width ≤ 15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | M372F0803DJ(T)0 | | M372F0883DJ(T)0 | | Unit |
|-------------------|------------|-----------------|-----|-----------------|-----|------|
| | | Min | Max | Min | Max | |
| I _{CC1} | -50 | - | 990 | - | 720 | mA |
| | -60 | - | 900 | - | 630 | mA |
| I _{CC2} | Don't care | - | 100 | - | 100 | mA |
| I _{CC3} | -50 | - | 990 | - | 720 | mA |
| | -60 | - | 900 | - | 630 | mA |
| I _{CC4} | -50 | - | 810 | - | 810 | mA |
| | -60 | - | 720 | - | 720 | mA |
| I _{CC5} | Don't care | - | 30 | - | 30 | mA |
| I _{CC6} | -50 | - | 990 | - | 990 | mA |
| | -60 | - | 900 | - | 900 | mA |
| I _{I(L)} | Don't care | -10 | 10 | -10 | 10 | uA |
| I _{O(L)} | | -5 | 5 | -5 | 5 | uA |
| V _{OH} | Don't care | 2.4 | - | 2.4 | - | V |
| V _{OL} | | - | 0.4 | - | 0.4 | V |

I_{CC1}* : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

I_{CC4}* : Extended Data Out Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.



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CAPACITANCE (TA = 25°C, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|-------------------------------------|--------|-----|-----|------|
| Input capacitance[A0, B0, A1 - A12] | CIN1 | - | 20 | pF |
| Input capacitance[W0, W2, OE0, OE2] | CIN2 | - | 20 | pF |
| Input capacitance[RAS0, RAS2] | CIN3 | - | 45 | pF |
| Input capacitance[CAS0, CAS4] | CIN4 | - | 20 | pF |
| Input/Output capacitance[DQ0 - 71] | CDQ | - | 17 | pF |

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : VIH/VIL=2.2/0.7V, VOH/VOL=2.0/0.8V, output loading CL=100pF

| Parameter | Symbol | -50 | | -60 | | Unit | Note |
|---------------------------------------|--------|-----|-----|-----|-----|------|----------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 84 | | 104 | | ns | |
| Read-modify-write cycle time | tRWC | 128 | | 153 | | ns | |
| Access time from RAS | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from CAS | tCAC | | 18 | | 20 | ns | 3,4,5,13 |
| Access time from column address | tAA | | 30 | | 35 | ns | 3,10,13 |
| CAS to output in Low-Z | tCLZ | 8 | | 8 | | ns | 3,13 |
| OE to output in Low-Z | tOLZ | 8 | | 8 | | ns | 3,13 |
| Output buffer turn-off delay from CAS | tCEZ | 8 | 18 | 8 | 18 | ns | 6,11,13 |
| Transition time(rise and fall) | tT | 1 | 50 | 1 | 50 | ns | 2 |
| RAS precharge time | tRP | 30 | | 40 | | ns | |
| RAS pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| RAS hold time | tRSH | 13 | | 15 | | ns | 13 |
| CAS hold time | tCSH | 36 | | 38 | | ns | 13 |
| CAS pulse width | tCAS | 8 | 10K | 10 | 10K | ns | |
| RAS to CAS delay time | tRCD | 15 | 32 | 18 | 40 | ns | 4,13 |
| RAS to column address delay time | tRAD | 10 | 20 | 13 | 25 | ns | 10,13 |
| CAS to RAS precharge time | tCRP | 10 | | 10 | | ns | 13 |
| Row address set-up time | tASR | 5 | | 5 | | ns | 13 |
| Row address hold time | tRAH | 5 | | 8 | | ns | 13 |
| Column address set-up time | tASC | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 7 | | 10 | | ns | |
| Column address to RAS lead time | tRAL | 30 | | 35 | | ns | 13 |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referenced to CAS | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to RAS | tRRH | -2 | | -2 | | ns | 8,13 |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| Write command hold time | tWCH | 7 | | 10 | | ns | |
| Write command pulse width | tWP | 7 | | 10 | | ns | |
| Write command to RAS lead time | tRWL | 13 | | 15 | | ns | 13 |
| Write command to CAS lead time | tCWL | 7 | | 10 | | ns | |
| Data set-up time | tDS | -2 | | -2 | | ns | 9,13 |
| Data hold time | tDH | 13 | | 15 | | ns | 9,13 |
| Refresh period(4K & 8K) | tREF | | 64 | | 64 | ms | |
| CAS to W delay time | tCWD | 33 | | 38 | | ns | 7 |
| RAS to W delay time | tRWD | 68 | | 82 | | ns | 7,13 |

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AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 3.3V ± 0.3V. See notes 1,2.)

| Parameter | Symbol | -50 | | -60 | | Unit | Note |
|--|--------|-----|------|-----|------|------|------|
| | | Min | Max | Min | Max | | |
| Column address to \overline{W} delay time | tAWD | 45 | | 53 | | ns | 7 |
| CAS precharge time to \overline{W} delay time | tCPWD | 47 | | 58 | | ns | |
| CAS setup time(CAS-before-RAS refresh) | tCSR | 10 | | 10 | | ns | 13 |
| CAS hold time(CAS-before-RAS refresh) | tCHR | 8 | | 8 | | ns | 13 |
| RAS to CAS precharge time | tRPC | 3 | | 3 | | ns | 13 |
| Access time from CAS precharge | tCPA | | 33 | | 40 | ns | 3,13 |
| Hyper page cycle time | tHPC | 20 | | 25 | | ns | 12 |
| Hyper page read-modify-write cycle time | tHPRWC | 70 | | 77 | | ns | 12 |
| CAS precharge time(Hyper page cycle) | tCP | 7 | | 10 | | ns | |
| RAS pulse width (Hyper page cycle) | tRASP | 50 | 200K | 60 | 200K | ns | |
| RAS hold time from CAS precharge | tRHCP | 35 | | 40 | | ns | 13 |
| \overline{W} to RAS precharge time(C-B-R refresh) | tWRP | 15 | | 15 | | ns | 13 |
| \overline{W} to RAS hold time(C-B-R refresh) | tWRH | 8 | | 8 | | ns | 13 |
| \overline{OE} access time | tOEA | | 18 | | 20 | ns | 13 |
| \overline{OE} to data delay | tOED | 15 | | 18 | | ns | 13 |
| Output buffer turn off delay time from \overline{OE} | tOEZ | 8 | 18 | 8 | 18 | ns | 13 |
| \overline{OE} command hold time | tOEH | 5 | | 5 | | ns | |
| Output data hold time(C-B-R refresh) | tDOH | 10 | | 10 | | ns | 13 |
| Output buffer turn off delay time from RAS | tREZ | 3 | 13 | 3 | 13 | ns | 6,11 |
| Output buffer turn off delay time from \overline{W} | tWEZ | 8 | 18 | 8 | 18 | ns | 6,13 |
| \overline{W} to data delay | tWED | 20 | | 20 | | ns | 13 |
| \overline{OE} to CAS hold time | tOCH | 5 | | 5 | | ns | |
| CAS hold time to \overline{OE} | tCHO | 5 | | 5 | | ns | |
| \overline{OE} precharge time | tOEP | 5 | | 5 | | ns | |
| \overline{W} pulse width (Hyper page cycle) | tWPE | 5 | | 5 | | ns | |
| Present Detect Read Cycle | | | | | | | |
| \overline{PDE} to Valid PD bit | tPD | | 10 | | 10 | ns | |
| \overline{PDE} to PD bit Inactive | tPDOFF | 2 | 7 | 2 | 7 | ns | |

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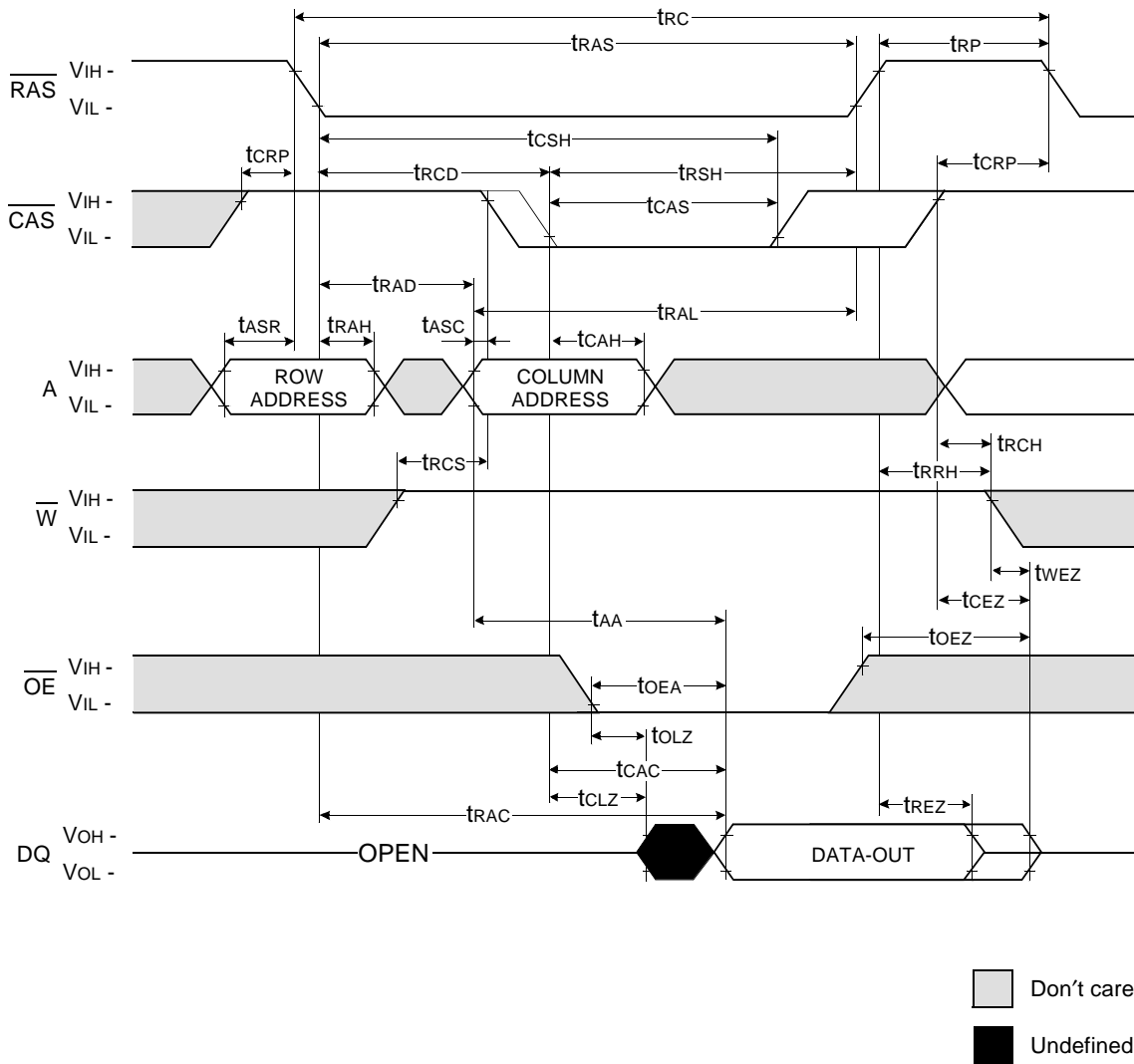
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or $\overline{\text{CAS}}$ -before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$. The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ going.
12. $t_{\text{ASC}} \geq 6\text{ns}$.
13. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

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READ CYCLE

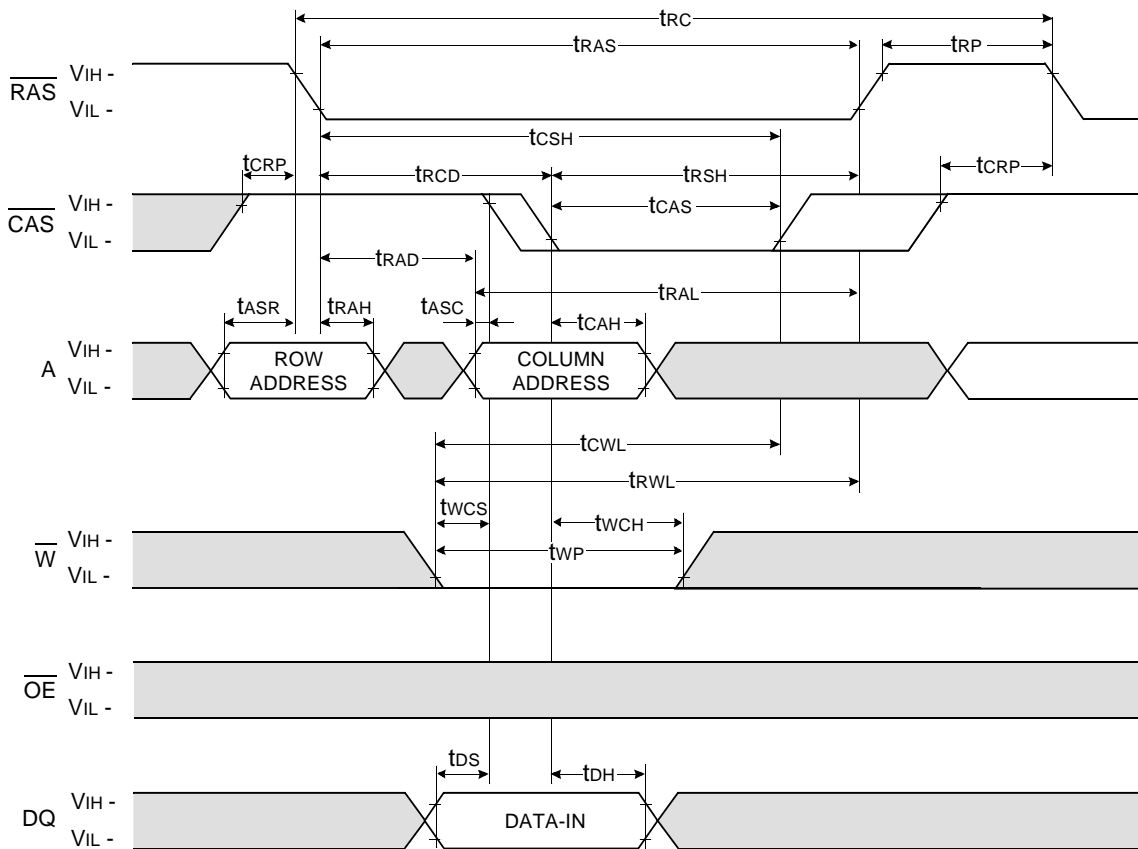


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WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



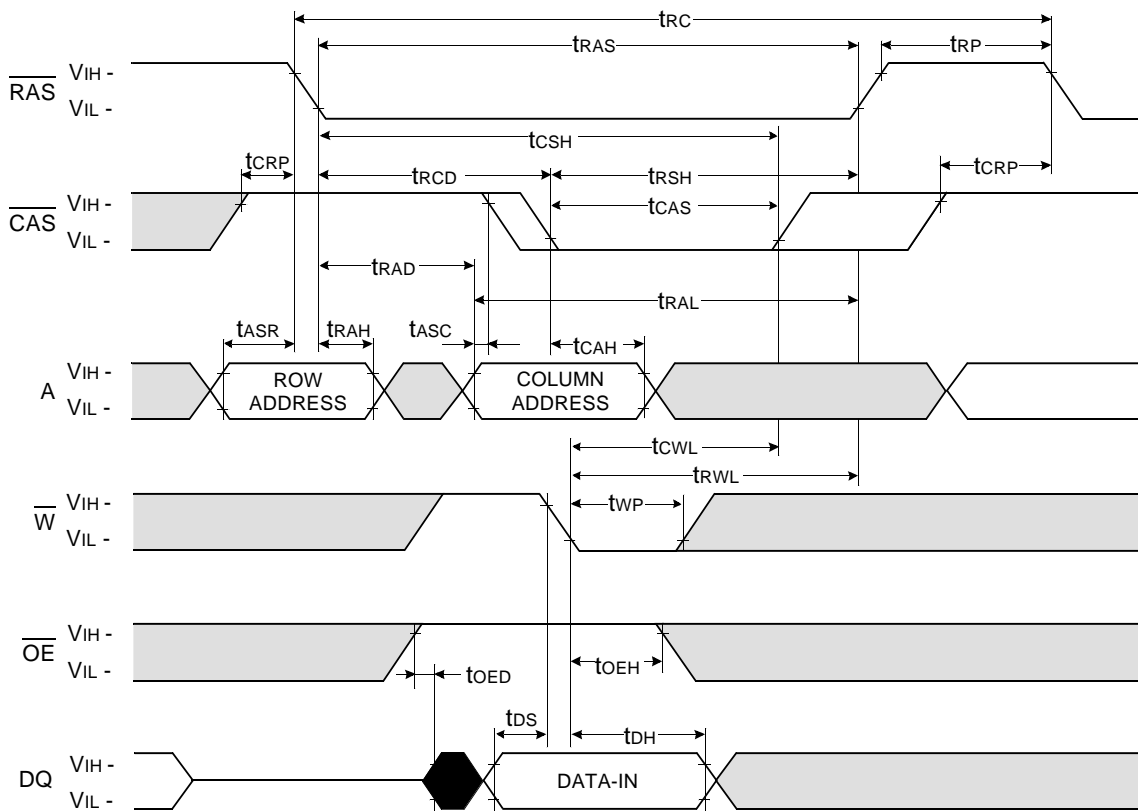
□ Don't care
■ Undefined

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WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN

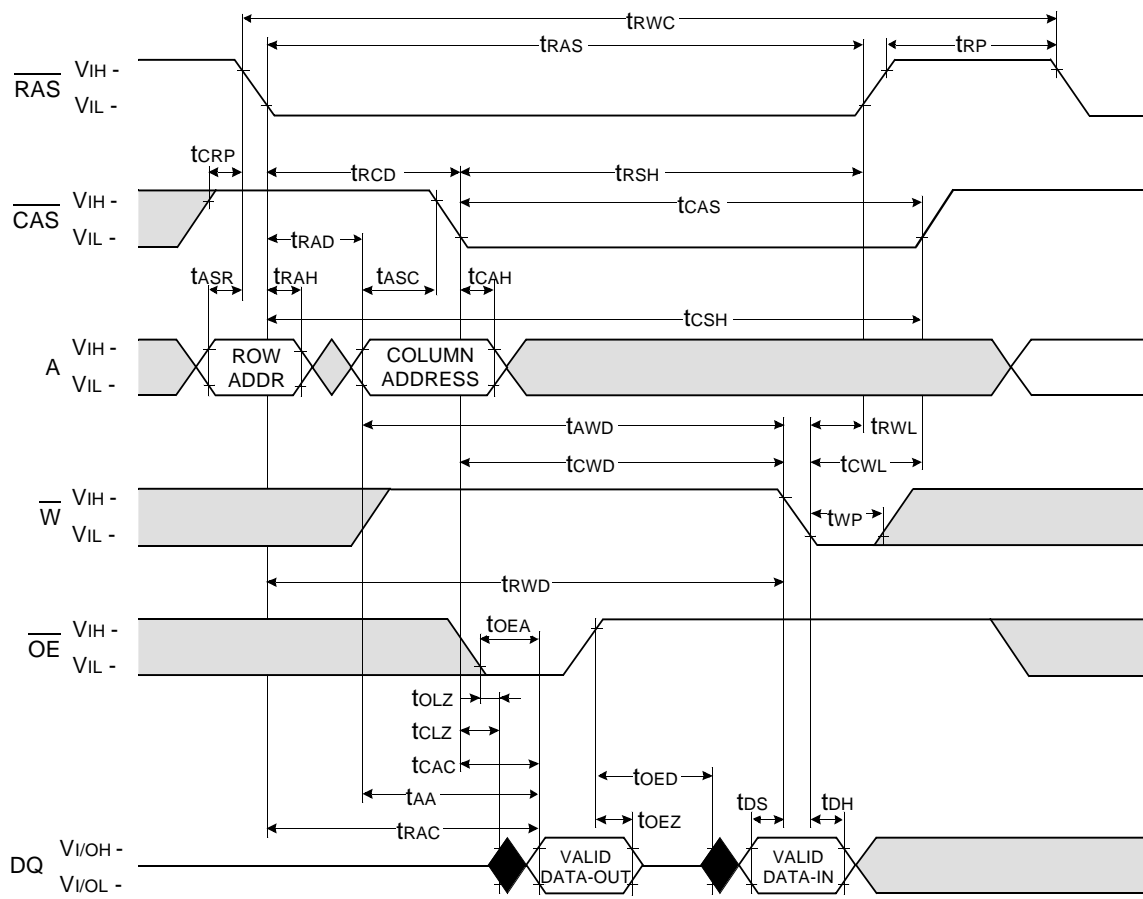


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READ - MODIFY - WRITE CYCLE

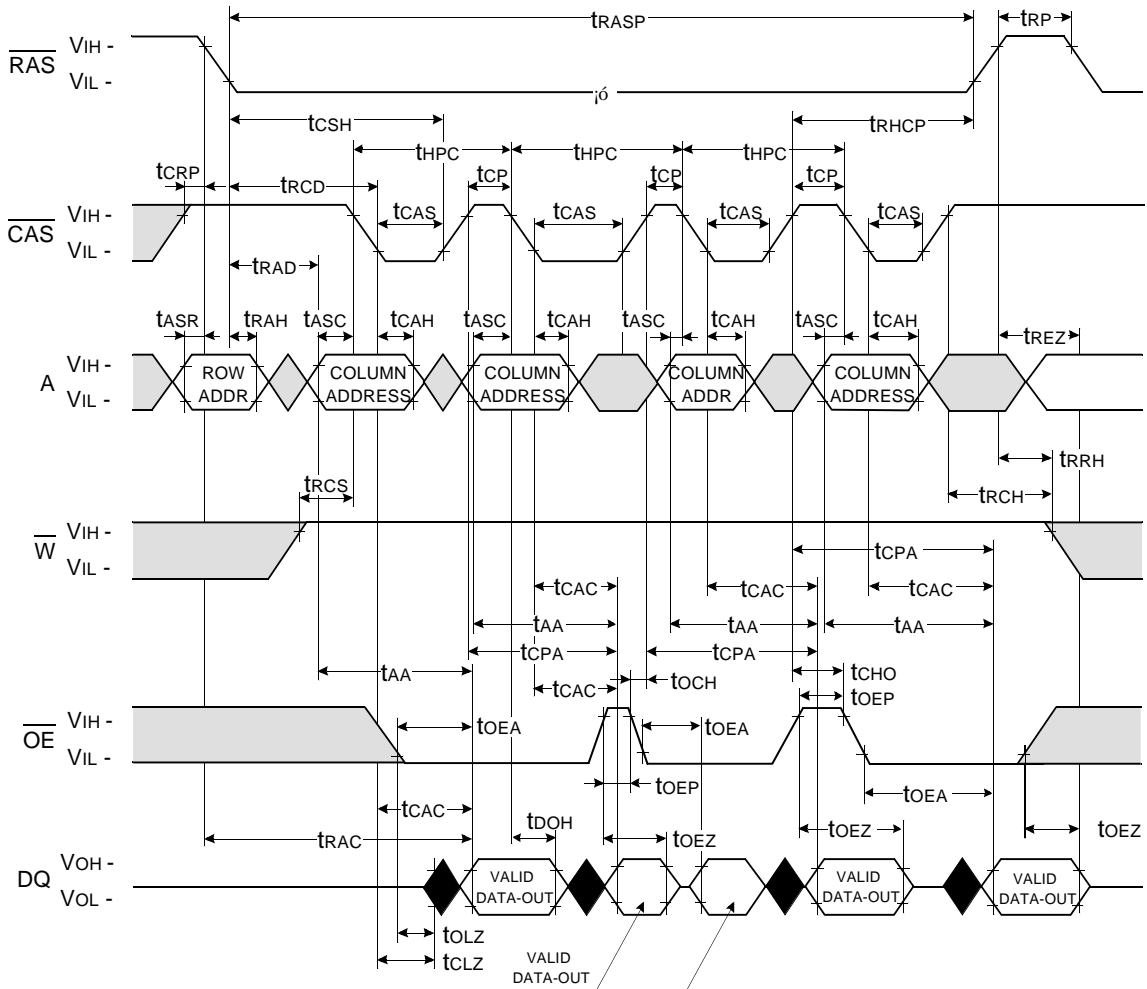


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DRAM MODULE

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HYPER PAGE READ CYCLE



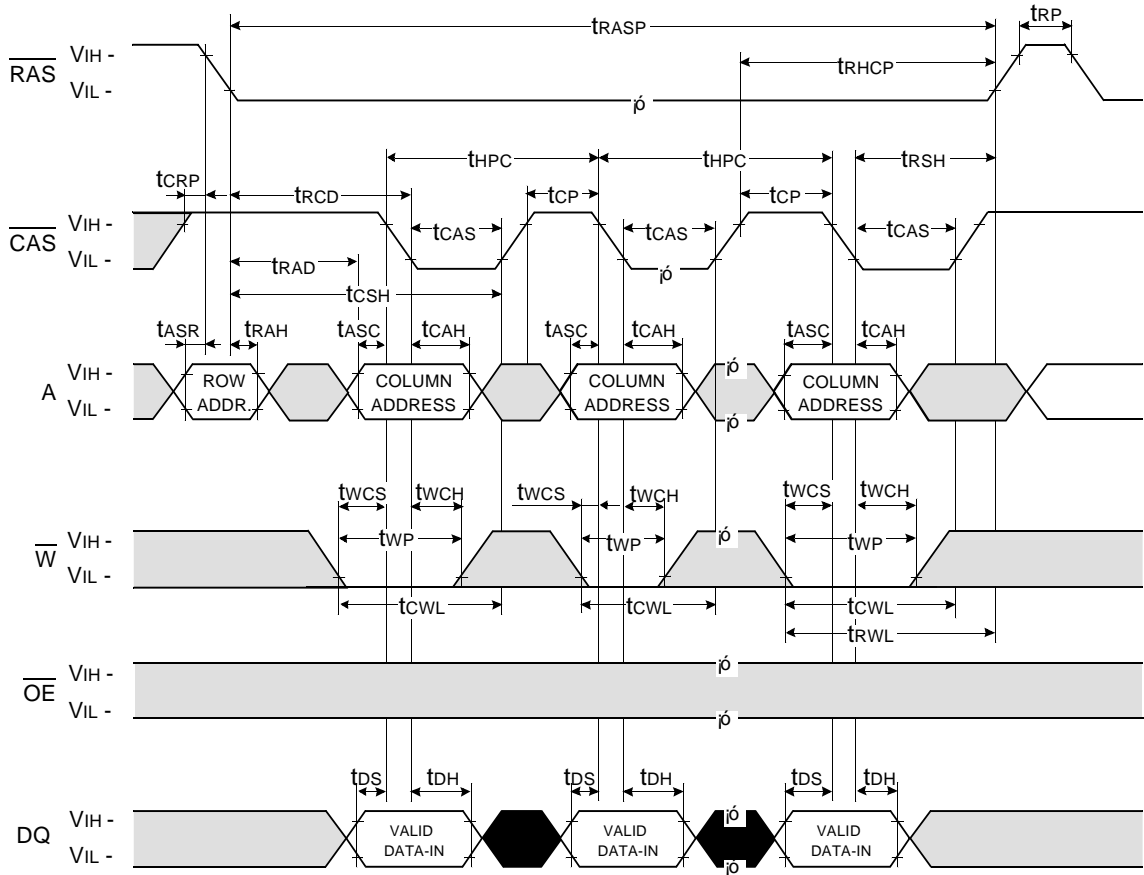
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DRAM MODULE

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HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

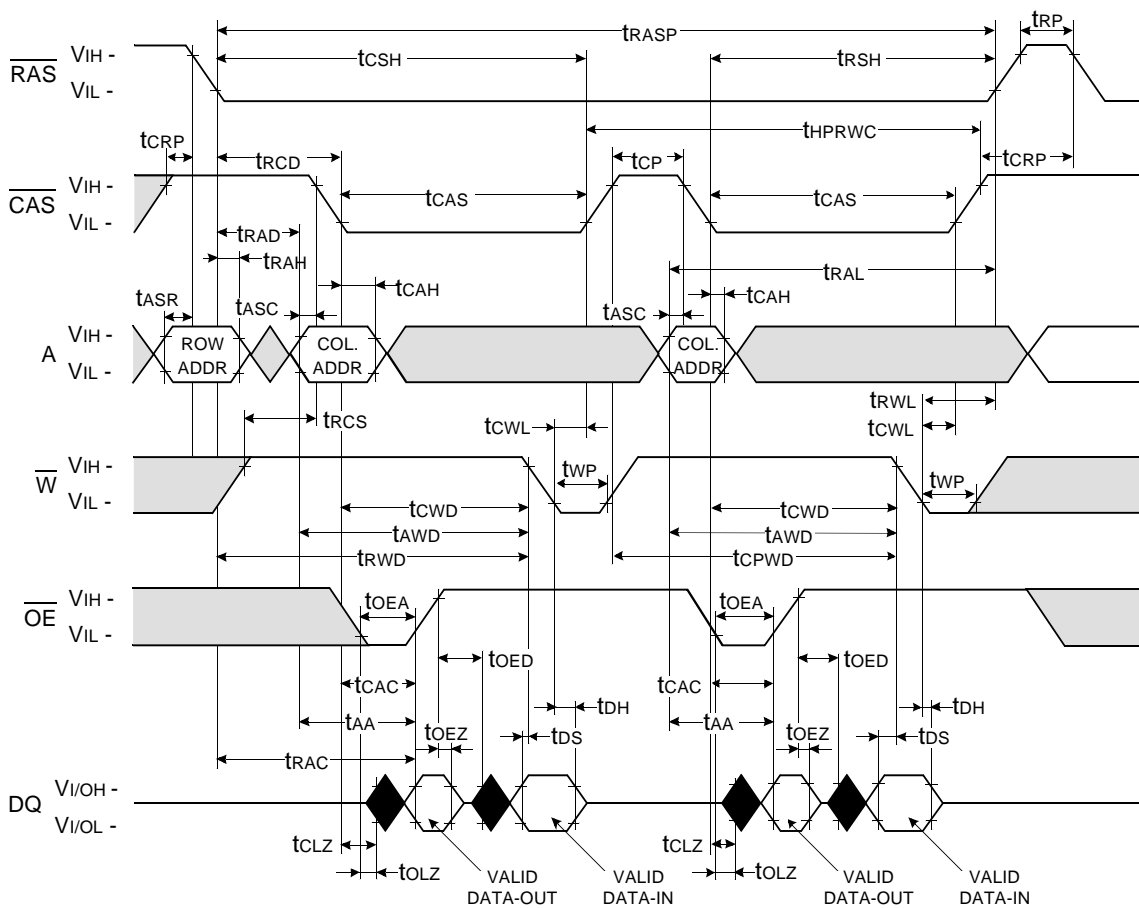


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HYPER PAGE READ-MODIFY-WRITE CYCLE

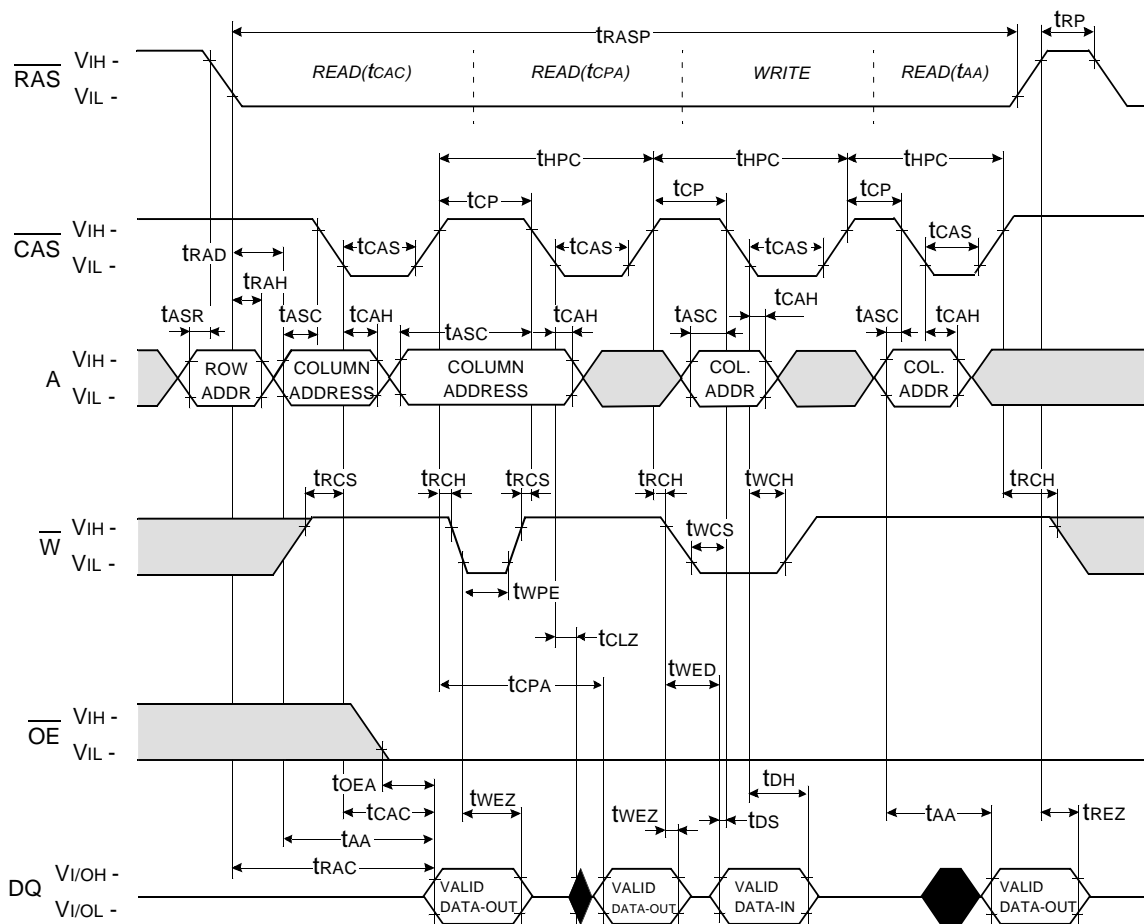


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DRAM MODULE

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HYPER PAGE READ AND WRITE MIXED CYCLE



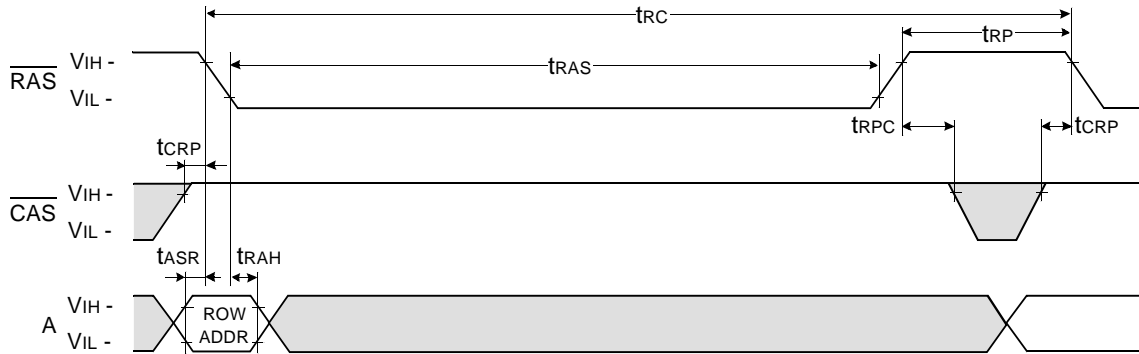
DRAM MODULE

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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

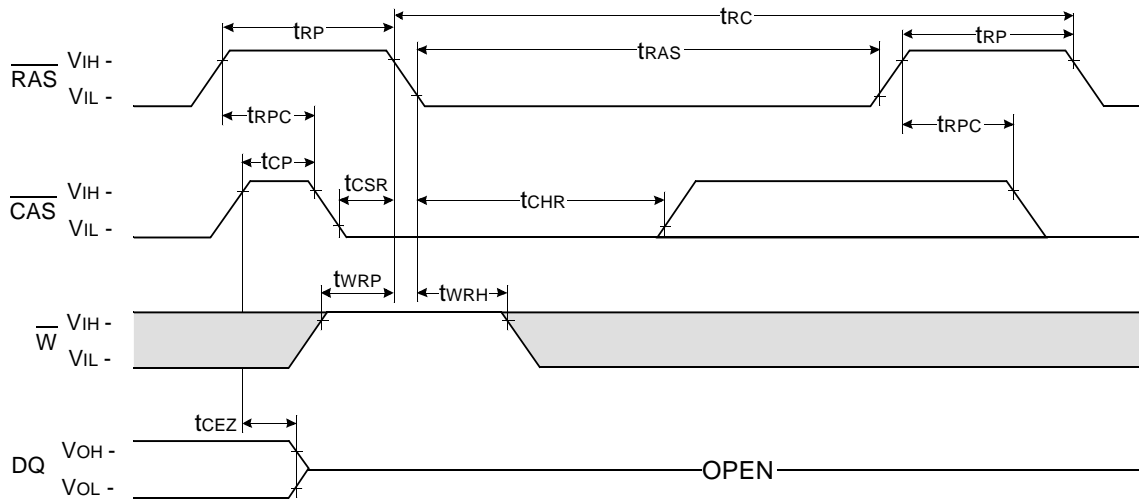
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



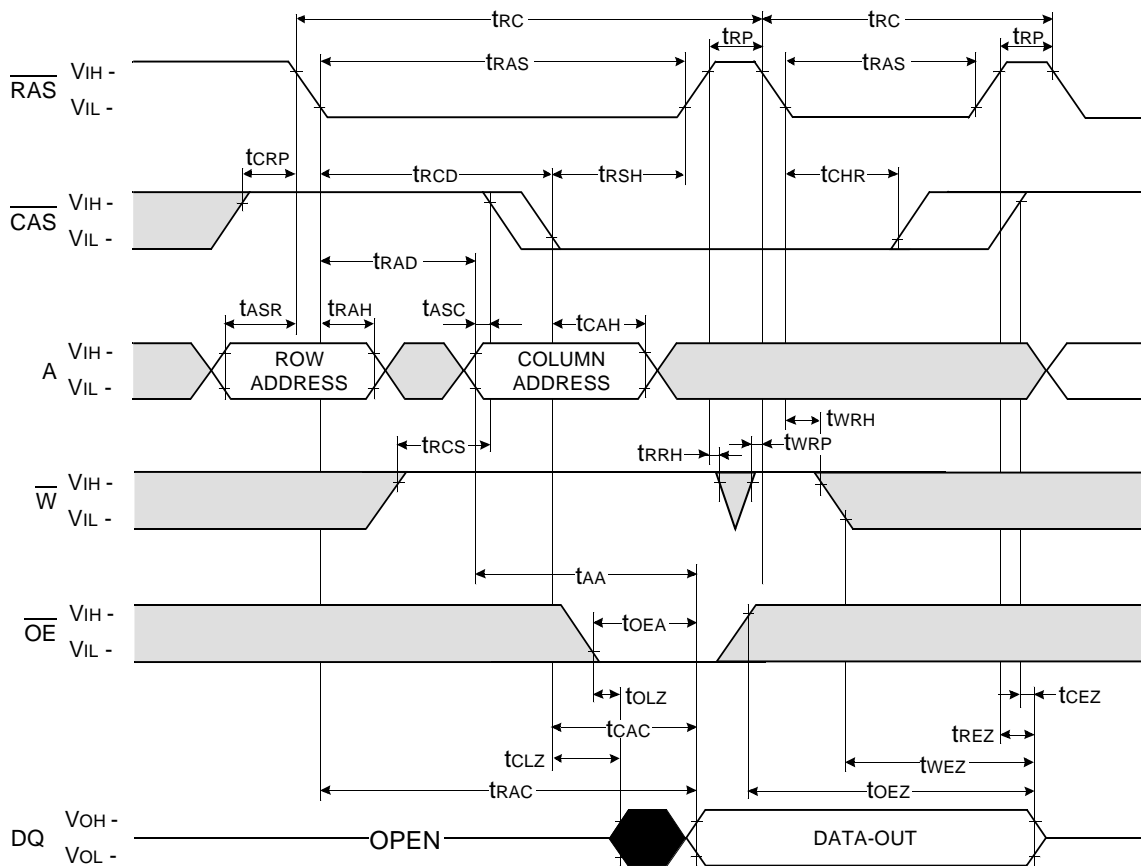
□ Don't care
 ■ Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

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HIDDEN REFRESH CYCLE (READ)



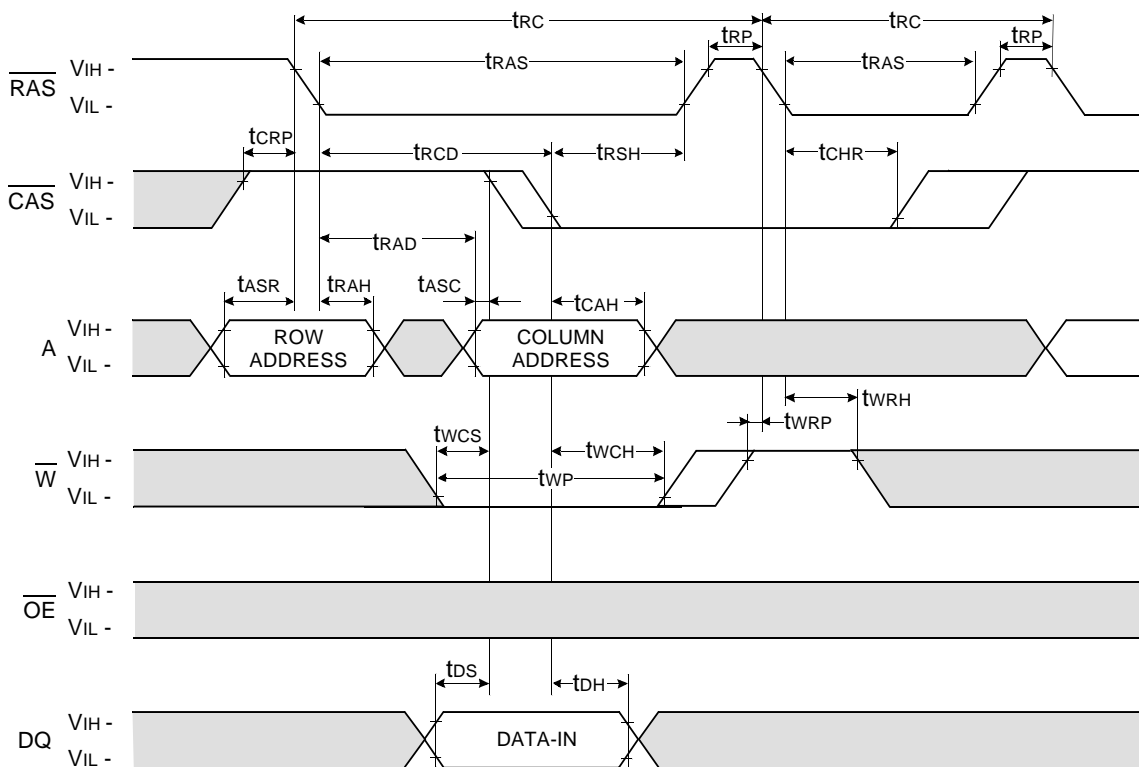
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HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

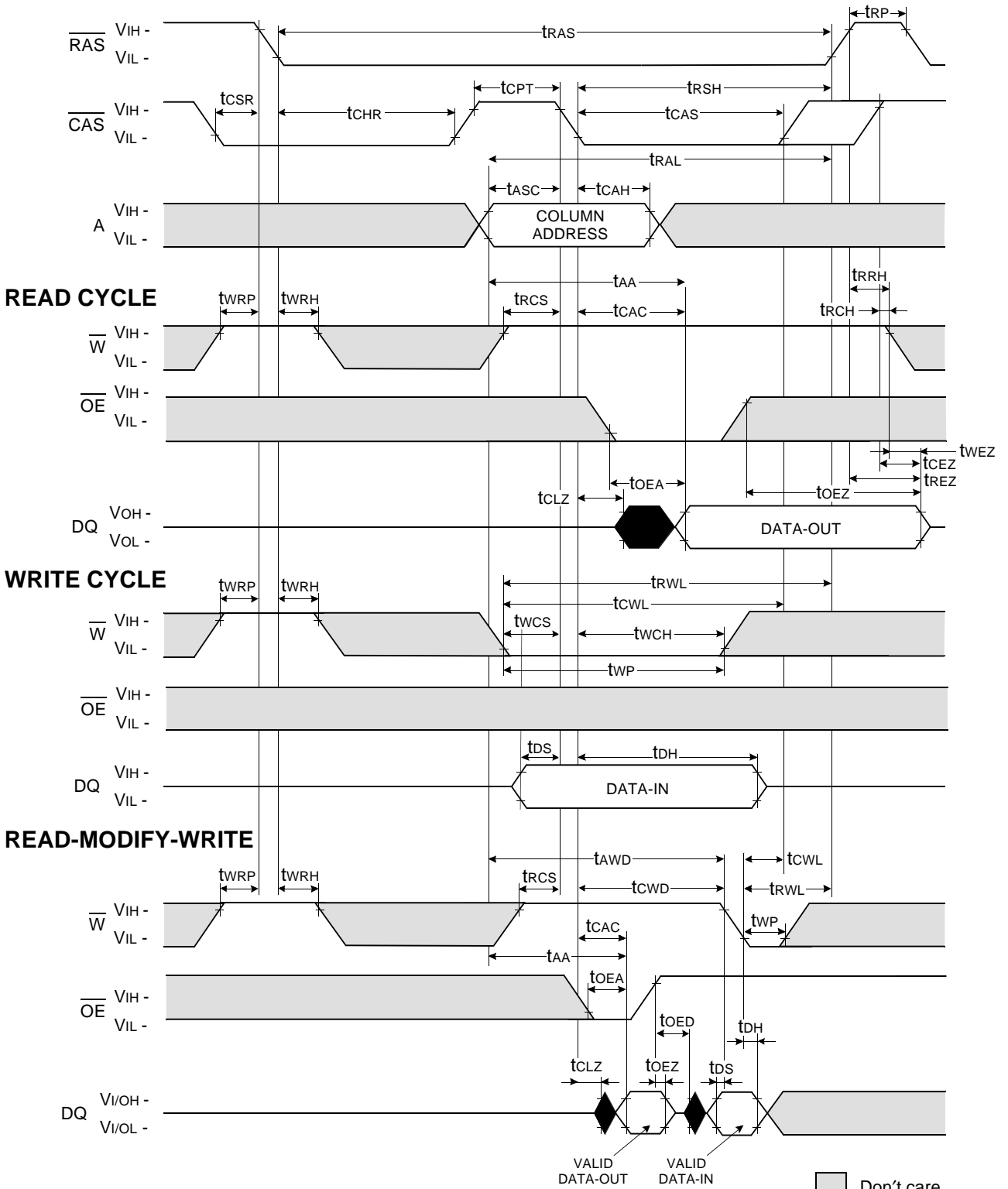


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M372F080(8)3DJ(T)0-C

CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



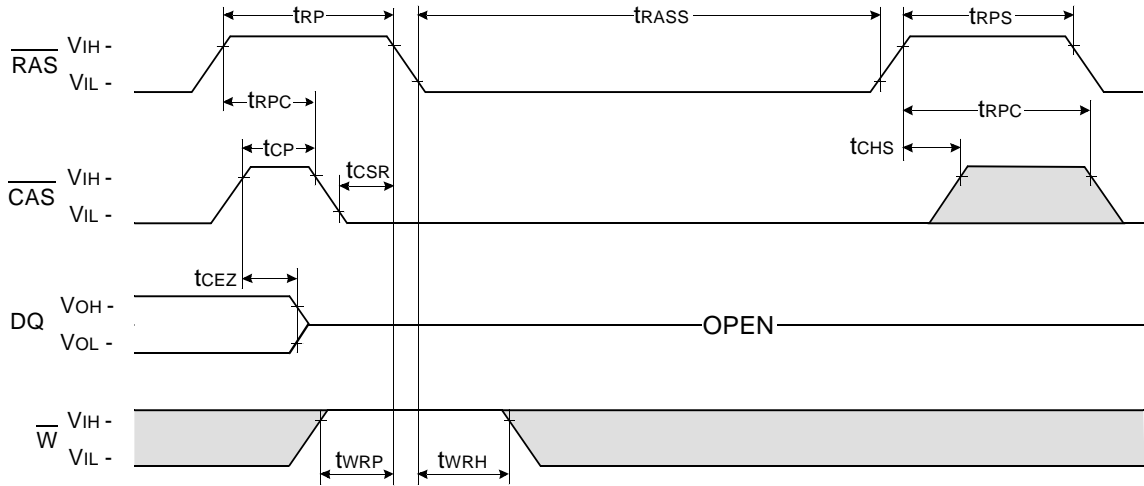
NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

DRAM MODULE

M372F080(8)3DJ(T)0-C

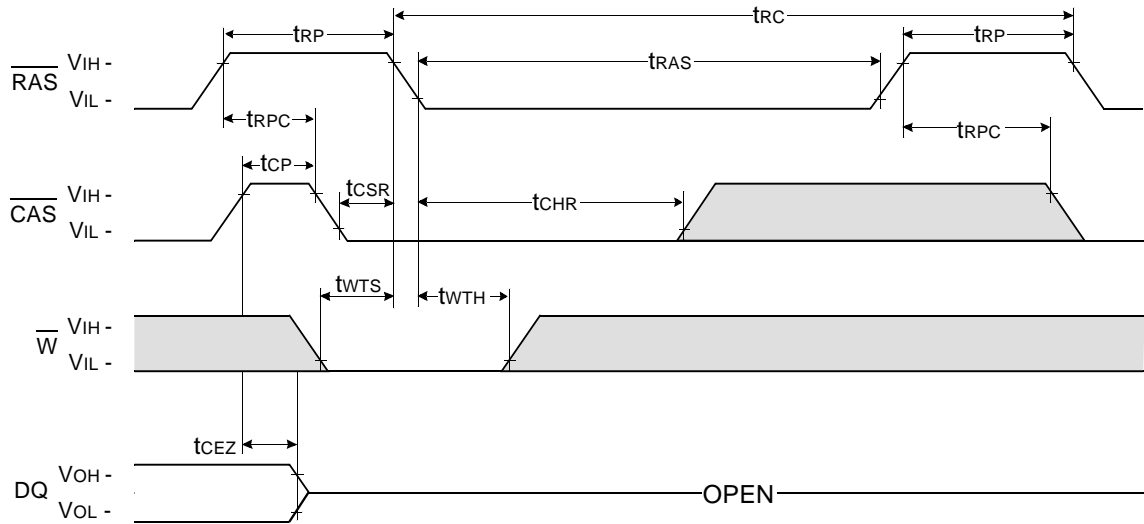
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



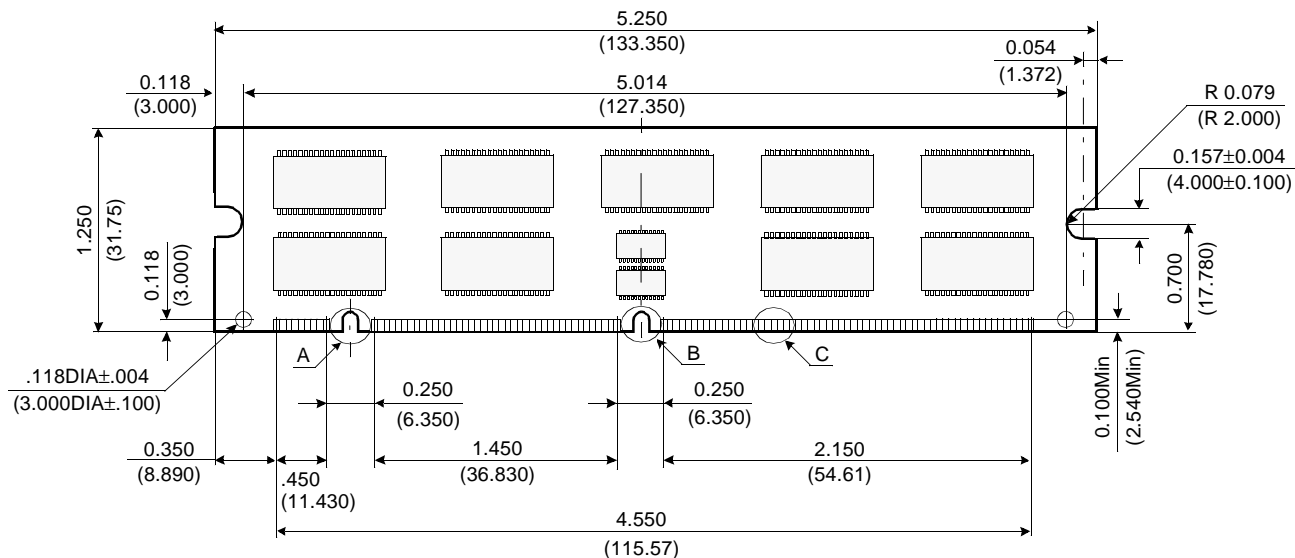
Don't care
 Undefined

DRAM MODULE

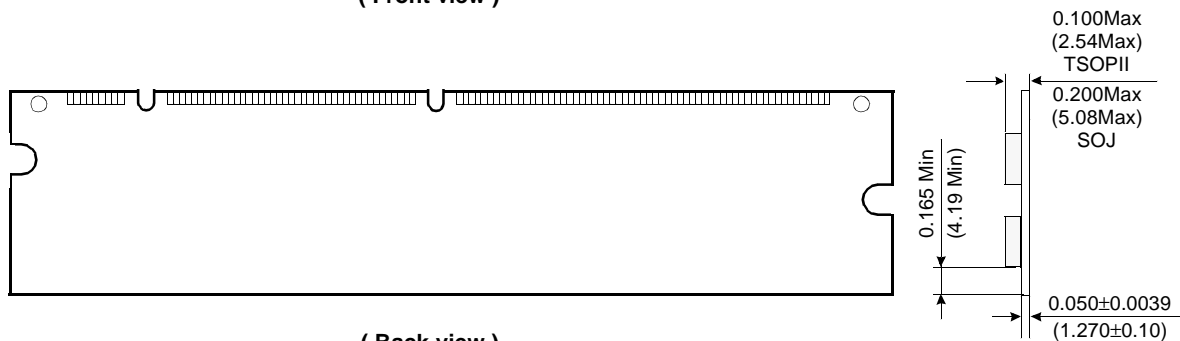
M372F080(8)3DJ(T)0-C

PACKAGE DIMENSIONS

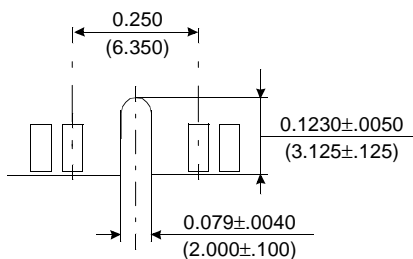
Units : Inches (millimeters)



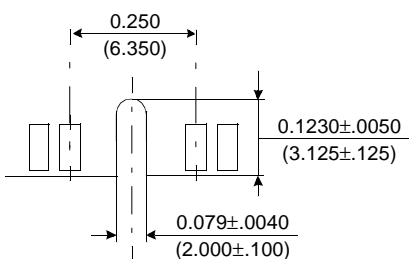
(Front view)



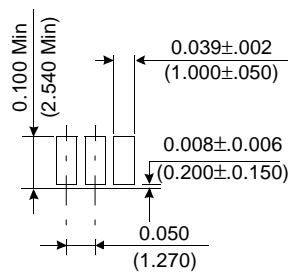
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 8Mx8 DRAM with EDO mode, SOJ or TSOPII.
 DRAM Part No. : M372F0803DJ(T)0 - K4E640812D-J, K4E640812D-T
 M372F0883DJ(T)0 - K4E660812D-J, K4E660812D-T