

M381L1713CTL

184pin Unbuffered DDR SDRAM MODULE

128MB DDR SDRAM MODULE

(16Mx72 based on 16Mx8 DDR SDRAM)

Unbuffered 184pin DIMM
72-bit ECC/Parity

Revision 0.3

May. 2002

M381L1713CTL

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Revision History

Revision 0.0 (Oct. 2001)

1. First release

Revision 0.1 (Nov. 2001)

1. Added DDR333 function
2. Updated DDR333 test specification
3. Deleted typical current in IDD spec. table
4. Included address and control input setup/hold time(tIS/tIH) at slow slew rate in DDR200/266 AC specification
5. Deleted Exit self refresh to write command(tXSW) in DDR200/266 AC specification
6. Changed unit of tMRD from tCK to ns at DDR333
7. Rename tXSA(exit self refresh to bank active command) to tXSNR(exit self refresh to non read command) at DDR200/266
8. Rename tXSR(exit self refresh to read command) to tXSRD at DDR200/266
9. Rename tWPREH(DQS in hold time) to tWPRE at DDR200/266
10. Rename tREF(Refresh interval time) to tREFI at DDR200/266
11. Rename tCDLR(Last write data to Read command) to tWTR

Revision 0.2 (Jan. 2002)

1. Added tRAP(Active to Read with auto precharge command)

Revision 0.3 (May. 2002)

1. Change pin location of A13 from pin 103 to pin 167

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M381L1713CTL DDR SDRAM 184pin DIMM

16Mx72 DDR SDRAM 184pin DIMM based on 16Mx8

GENERAL DESCRIPTION

The Samsung M381L1713CTL is 16M bit x 72 Double Data Rate SDRAM high density memory modules. The Samsung M381L1713CTL consists of eight CMOS 16M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The M381L1713CTL is Dual In-line Memory Modules and inten-ded for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq.	Interface
M381L1713CTL-C(L)B3	166MHz(6ns@CL=2.5)	SSTL_2
M381L1713CTL-C(L)A2	133MHz(7.5ns@CL=2)	
M381L1713CTL-C(L)B0	133MHz(7.5ns@CL=2.5)	

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and \overline{CK})
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 15.6us refresh interval(4K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1250 mil, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin Front	Pin Front	Pin Front	Pin Back	Pin Back	Pin Back
1	VREF	32	A5	62	VDDQ
2	DQ0	33	DQ24	63	/WE
3	VSS	34	VSS	64	DQ41
4	DQ1	35	DQ25	65	/CAS
5	DQS0	36	DQS3	66	VSS
6	DQ2	37	A4	67	DQS5
7	VDD	38	VDD	68	DQ42
8	DQ3	39	DQ26	69	DQ43
9	NC	40	DQ27	70	VDD
10	NC	41	A2	71	*/CS2
11	VSS	42	VSS	72	DQ48
12	DQ8	43	A1	73	DQ49
13	DQ9	44	*CB0	74	VSS
14	DQS1	45	*CB1	75	/CK2
15	VDDQ	46	VDD	76	CK2
16	CK1	47	*DQS8	77	VDDQ
17	/CK1	48	A0	78	DQS6
18	VSS	49	*CB2	79	DQ50
19	DQ10	50	VSS	80	DQ51
20	DQ11	51	*CB3	81	VSS
21	CKE0	52	BA1	82	VDDID
22	VDDQ		KEY	83	DQ56
23	DQ16	53	DQ32	84	DQ57
24	DQ17	54	VDDQ	85	VDD
25	DQS2	55	DQ33	86	DQS7
26	VSS	56	DQS4	87	DQ58
27	A9	57	DQ34	88	DQ59
28	DQ18	58	VSS	89	VSS
29	A7	59	BA0	90	NC
30	VDDQ	60	DQ35	91	SDA
31	DQ19	61	DQ40	92	SCL
				93	VSS
				94	DQ4
				95	DQ5
				96	VDDQ
				97	DM0
				98	DQ6
				99	DQ7
				100	VSS
				101	NC
				102	NC
				103	NC
				104	VDDQ
				105	DQ12
				106	DQ13
				107	DM1
				108	VDD
				109	DQ14
				110	DQ15
				111	*CKE1
				112	VDDQ
				113	*BA2
				114	DQ20
				115	*A12
				116	VSS
				117	DQ21
				118	A11
				119	DM2
				120	VDD
				121	DQ22
				122	A8
				123	DQ23
				124	VSS
				125	A6
				126	DQ28
				127	DQ29
				128	VDDQ
				129	DM3
				130	A3
				131	DQ30
				132	VSS
				133	DQ31
				134	*CB4
				135	*CB5
				136	VDDQ
				137	CK0
				138	/CK0
				139	VSS
				140	*DM8
				141	A10
				142	*CB6
				143	VDDQ
				144	*CB7
				145	VSS
				146	DQ36
				147	DQ37
				148	VDD
				149	DM4
				150	DQ38
				151	DQ39
				152	VSS
				153	DQ44
				154	/RAS
				155	DQ45
				156	VDDQ
				157	/CS0
				158	*/CS1
				159	DM5
				160	VSS
				161	DQ46
				162	DQ47
				163	*/CS3
				164	VDDQ
				165	DQ52
				166	DQ53
				167	*A13
				168	VDD
				169	DM6
				170	DQ54
				171	DQ55
				172	VDDQ
				173	NC
				174	DQ60
				175	DQ61
				176	VSS
				177	DM7
				178	DQ62
				179	DQ63
				180	VDDQ
				181	SA0
				182	SA1
				183	SA2
				184	VDDSPD

PIN DESCRIPTION

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0,CK0~ CK2,CK2	Clock input
CKE0	Clock enable input
/CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DM0 ~ DM7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

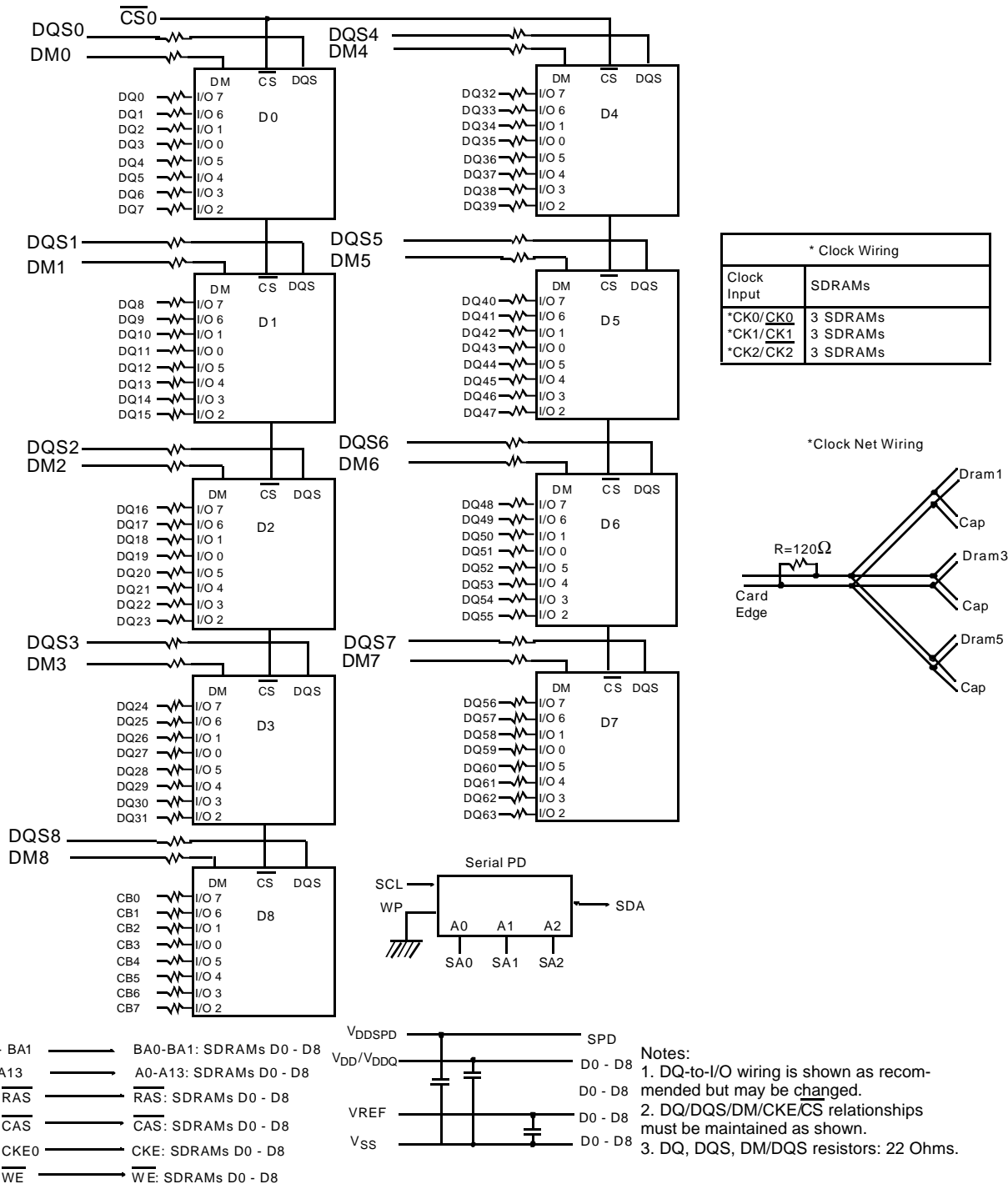
* These pins are not used in this module.

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Functional Block Diagram



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-1.0 ~ 3.6	V
Voltage on V _{DDQ} supply relative to Vss	V _{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	13.5	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V _{DD} of 2.5V)	V _{DD}	2.3	2.7		
I/O Supply voltage	V _{DDQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	V _{DDQ} /2-50mV	V _{DDQ} /2+50mV	V	1
I/O Termination voltage(system)	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{DDQ} +0.3	V	4
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	4
Input Voltage Level, CK and \overline{CK} inputs	V _{IN} (DC)	-0.3	V _{DDQ} +0.3	V	
Input Differential Voltage, CK and \overline{CK} inputs	V _{ID} (DC)	0.3	V _{DDQ} +0.6	V	3
Input crossing point voltage, CK and \overline{CK} inputs	V _{IX} (DC)	1.15	1.35	V	5
Input leakage current	I _I	-2	2	uA	
Output leakage current	I _{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ;V _{OUT} = V _{TT} + 0.84V	I _{OH}	-16.8		mA	
Output High Current(Normal strength driver) ;V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8		mA	
Output High Current(Half strength driver) ;V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9		mA	
Output High Current(Half strength driver) ;V _{OUT} = V _{TT} - 0.45V	I _{OL}	9		mA	

Notes 1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2.V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.

5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

6. These characteristics obey the SSTL-2 class II standards.

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DDR SDRAM IDD spec table

(V_{dd} = 2.7V, T = 10' C)

Symbol	B3(DDR333@CL=2.5)	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0	990	855	855	mA	
IDD1	1260	1125	1125	mA	
IDD2P	36	36	36	mA	
IDD2F	288	225	225	mA	
IDD2Q	180	135	135	mA	
IDD3P	360	270	270	mA	
IDD3N	495	495	495	mA	
IDD4R	1440	1440	1440	mA	
IDD4W	1440	1440	1440	mA	
IDD5	1890	1890	1890	mA	
IDD6	Normal	18	18	mA	
	Low power	9	9	mA	Optional
IDD7A	3600	3150	3150	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

AC OPERATING CONDITIONS

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

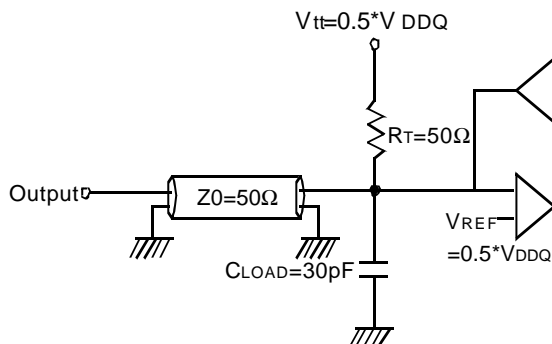
- Note
1. VID is the magnitude of the difference between the input level on CK and the input on \overline{CK} .
 2. The value of V_{I_X} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relative to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	V _{tt}	V	
Output load condition	See Load Circuit		

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Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE (VDD=2.5V, VDDQ=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A0 ~ A11, BA0 ~ BA1, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	CIN1	49	57	pF
Input capacitance(CKE0)	CIN2	42	50	pF
Input capacitance($\overline{\text{CS}}$ 0)	CIN3	42	50	pF
Input capacitance(CLK0, CLK1, CLK2)	CIN4	22	25	pF
Data & DQS input/output capacitance(DQ0~DQ63)	COU5	6	8	pF
Input capacitance(DM0~DM8)	CIN5	6	8	pF

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AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)

Parameter	Symbol	-TCB3 (DDR333)		-TCA2 (DDR266A)		-TCB0 (DDR266B)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	60		65		65		ns		
Refresh row cycle time	tRFC	72		75		75		ns		
Row active time	tRAS	42	70K	45	120K	45	120K	ns		
RAS to CAS delay	tRCD	18		20		20		ns		
Row precharge time	tRP	18		20		20		ns		
Row active to Row active delay	tRRD	12		15		15		ns		
Write recovery time	tWR	15		15		15		ns		
Last data in to Read command	tWTR	1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	7.5	12	10	12	ns	5
		CL=2.5	6	12	7.5	12	7.5	12	ns	5
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSCK	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns		
Output data access time from CK/CK	tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Data strobe edge to output data edge	tDQSQ	-	0.45	-	0.5	-	0.5	ns	5	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		ns	2	
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time(fast)	tIS	0.75		0.9		0.9		ns	6	
Address and Control Input hold time(fast)	tIH	0.75		0.9		0.9		ns	6	
Address and Control Input setup time(slow)	tIS	0.8		1.0		1.0		ns	6	
Address and Control Input hold time(slow)	tIH	0.8		1.0		1.0		ns	6	
Data-out high impedance time from CK/CK	tHZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Data-out low impedance time from CK/CK	tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns		
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		0.5		V/ns	6	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ns	7	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5			

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Parameter	Symbol	-TCB3 (DDR333)		-TCA2 (DDR266A)		-TCB0 (DDR266B)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		2.2		2.2		ns	
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		ns	
Power down exit time	tPDEX	6		7.5		7.5		ns	
Exit self refresh to non-Read command	tXSNR	75		75		75		ns	4
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	tREFI	15.6		15.6		15.6		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.55		0.75		0.75	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Active to Read with Auto precharge command	tRAP	20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

- Maximum burst refresh cycle : 8
- The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with tRCD satisfied after this command.
- For registered DIMMs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
- Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

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8. I/O Setup/Hold Plateau Derating

I/O Input Level	Δt_{DS}	Δt_{DH}
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below $V_{REF} \pm 310mV$ for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	Δt_{DS}	Δt_{DH}
(ns/V)	(ps)	(ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as $1/SlewRate1-1/SlewRate2$. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Reference>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	$\Delta t_{IH}/t_{IS}$ (ps)	$\Delta t_{DSS}/t_{DSH}$ (ps)	$\Delta t_{AC}/t_{DQSCK}$ (ps)	$\Delta t_{LZ}(\min)$ (ps)	$\Delta t_{HZ}(\max)$ (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

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Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA _{0,1}	A _{10/AP}	A ₁₁ A _{9 ~ A₀}	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L					X		3	
		Exit	L	H	L	H	H	H	X		3	
					H	X	X	X			3	
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	Column Address (A ₀ ~A ₉)	4	
	Auto Precharge Enable								H		4	
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	Column Address (A ₀ ~A ₉)	4	
	Auto Precharge Enable								H		4, 6	
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry	H	L	H	X	X	X	X				
				L	V	V	V					
	Exit	L	H	X	X	X	X					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X				
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	V	V	V					
DM		H	X					X			8	
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9	
				L	H	H	H		9			

Note : 1. OP Code : Operand Code. A₀ ~ A₁₁ & BA₀ ~ BA₁ : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.

If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.

If BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank B is selected.

If BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank C is selected.

If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.

5. If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

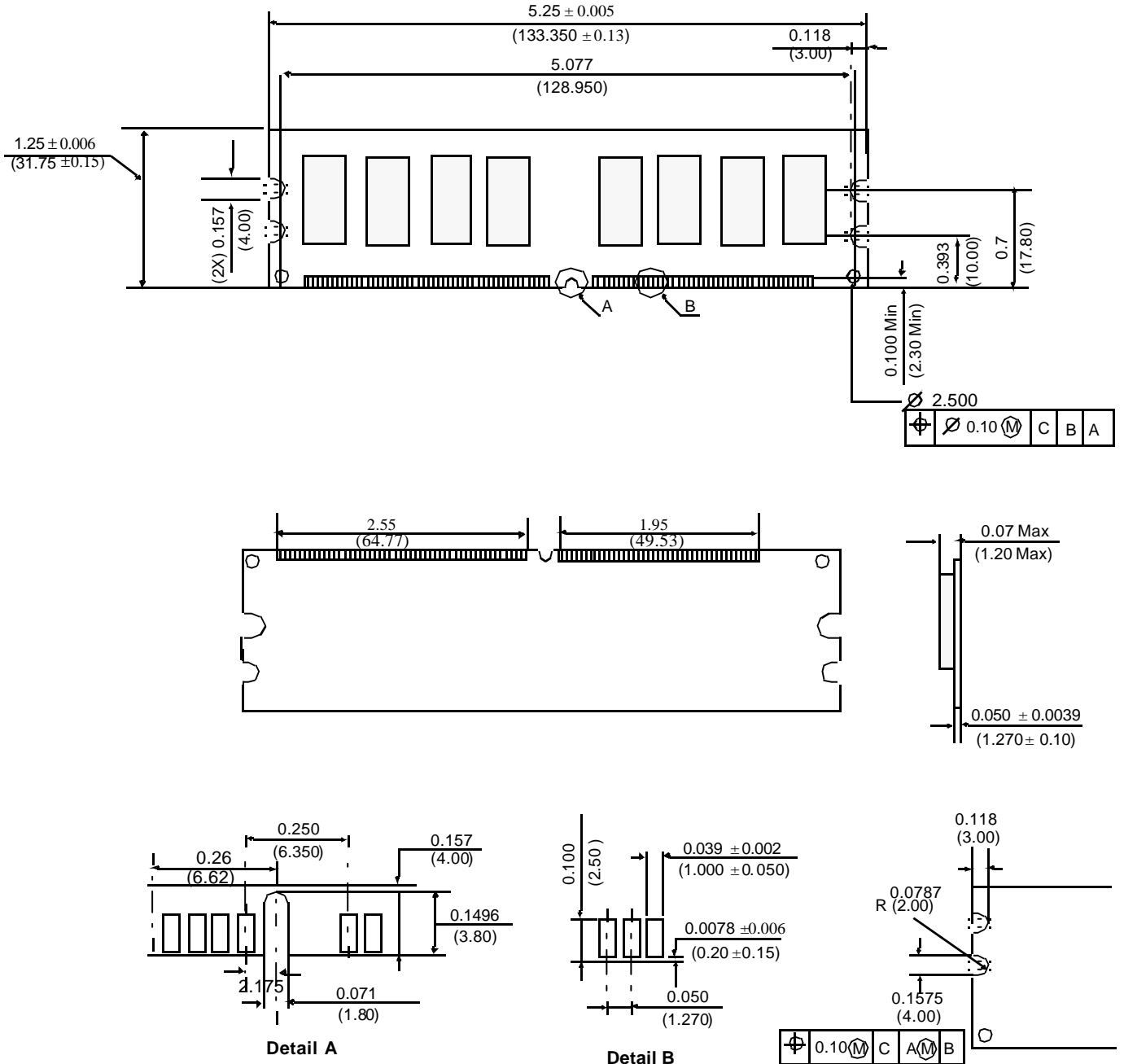
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

M381L1713CTL

184pin Unbuffered DDR SDRAM MODULE

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : $\pm 0.005(.13)$ unless otherwise specified.
 The used device is 16Mx8 DDR SDRAM, TSOP.
 SDRAM Part NO : K4H280838C.