

M383L6420CT1

184pin Registered DDR SDRAM MODULE

512MB DDR SDRAM MODULE

(64Mx72 based on 64Mx4 DDR SDRAM)

Registered 184pin DIMM
72-bit ECC/Parity

Revision 0.3

May. 2002

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Revision History

Revision 0 (Aug 2001)

1. First release for internal usage

Revision 0.1 (Dec. 2001)

- Add derating values for the specifications if the single-ended clock skew rate is less than 1.0V/ns in page 47.
- Revised "Absolute maximum rating" table in page 38.
 - . Changed "Voltage on VDDQ supply relative to VSS" value from -0.5~3.6V to -1~3.6V
 - . Changed "power dissipation" value from 1.0W to 1.5W.
- Revised AC parameter table

	From						To					
	DDR266A		DDR266B		DDR200		DDR266A		DDR266B		DDR200	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
tHZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tLZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tWPST (tCK)	0.25		0.25		0.25		0.4	0.6	0.4	0.6	0.4	0.6
tPDEX	10ns		10ns		10ns		7.5ns		7.5ns		10ns	

- Deleted typical current in IDD spec. table
- Included address and control input setup/hold time(tIS/tIH) at slow slew rate in DDR200/266 AC specification
- Deleted Exit self refresh to write command(tXSW) in DDR200/266 AC specification
- Rename tXSA(exit self refresh to bank active command) to tXSNR(exit self refresh to non read command) at DDR200/266
- Rename tXSR(exit self refresh to read command) to tXSRD at DDR200/266
- Rename tWPREH(DQS in hold time) to tWPRE at DDR200/266
- Rename tREF(Refresh interval time) to tREFI at DDR200/266
- Changed tWR value from 2tCK to 15ns.
- Rename tCDLR(Write data out to Read command) to tWTR
- Added tDAL(tWR+tRP)

Revision 0.2 (Dec. 2001)

1. Added tRAP(Active to Read with auto precharge delay).

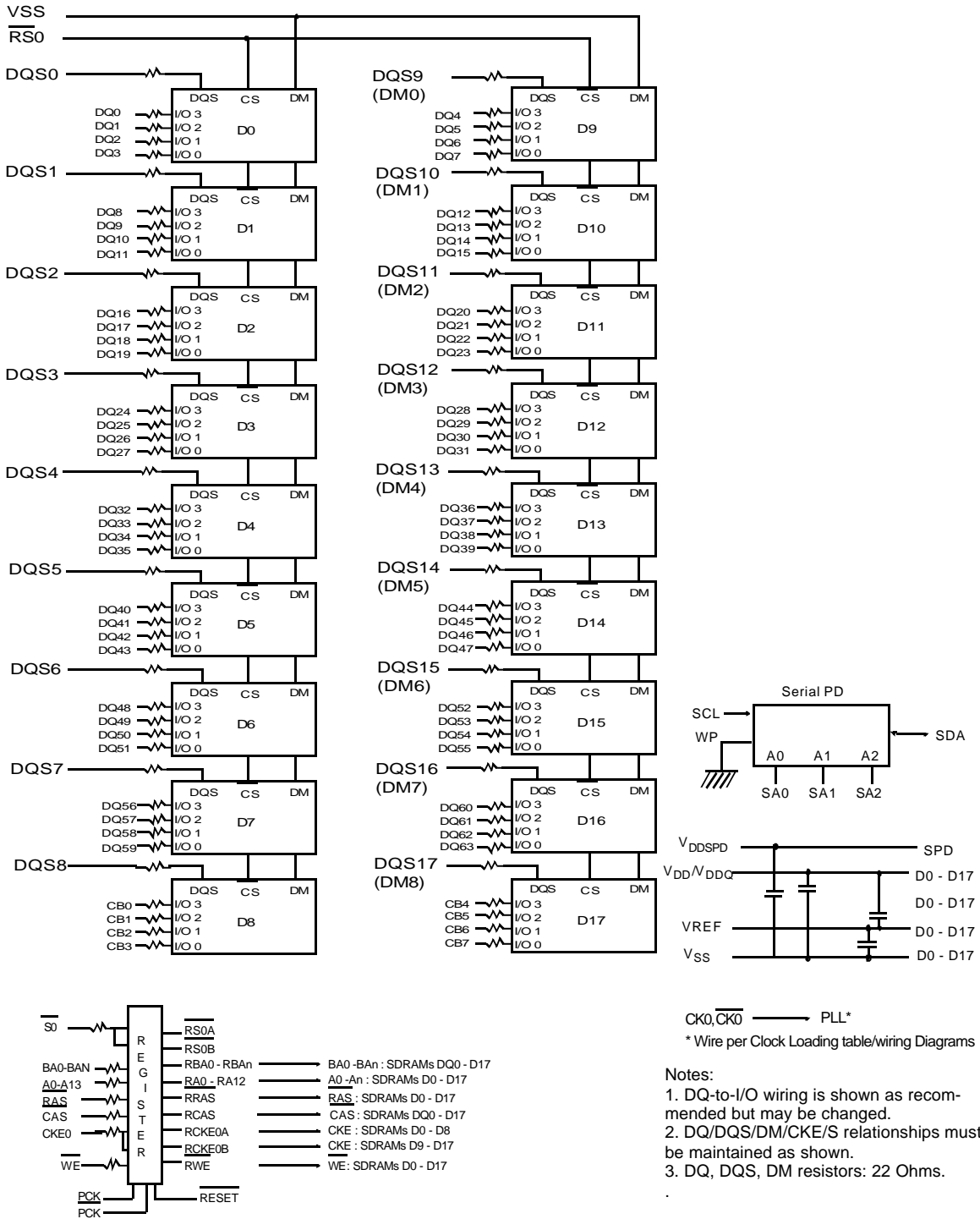
Revision 0.3 (May. 2002)

1. Change pin location of A13 from pin 103 to pin 167

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Functional Block Diagram



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Absolute Maximum Rate

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	27	W
Short circuit current	I_{OS}	50	mA

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to $V_{SS}=0V$, $T_A=0$ to $70^{\circ}C$)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	$V_{DDQ}/2-50mV$	$V_{DDQ}/2+50mV$	V	1
I/O Termination voltage(system)	V_{TT}	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	4
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	4
Input Voltage Level, CK and \overline{CK} inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and \overline{CK} inputs	$V_{ID}(DC)$	0.3	$V_{DDQ}+0.6$	V	3
Input crossing point voltage, CK and \overline{CK} inputs	$V_{IX}(DC)$	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	I_{OH}	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	I_{OL}	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	I_{OH}	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	I_{OL}	9		mA	

Notes 1. Includes $\pm 25mV$ margin for DC offset on V_{REF} , and a combined total of $\pm 50mV$ margin for all AC noise and DC offset on V_{REF} , bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF} , both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of $\leq 3nH$.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF}

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHz.

5. The value of V_{IX} is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the dc level of the same.

6. These characteristics obey the SSTL-2 class II standards.

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DDR SDRAM IDD spec table

Symbol	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	A0(DDR200@CL=2)	Unit	Notes
IDD0	2690	2690	2530	mA	
IDD1	3300	3300	2930	mA	
IDD2P	1140	1140	1140	mA	
IDD2F	1400	1400	1360	mA	
IDD2Q	1540	1540	1460	mA	
IDD3P	1660	1660	1580	mA	
IDD3N	1980	1980	1840	mA	
IDD4R	3300	3300	2970	mA	
IDD4W	3580	3580	3080	mA	
IDD5	4130	4130	3880	mA	
IDD6	1160	1160	1160	mA	
IDD6	Low Power	1130	1130	mA	Optional
IDD7A	5880	5880	5180	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

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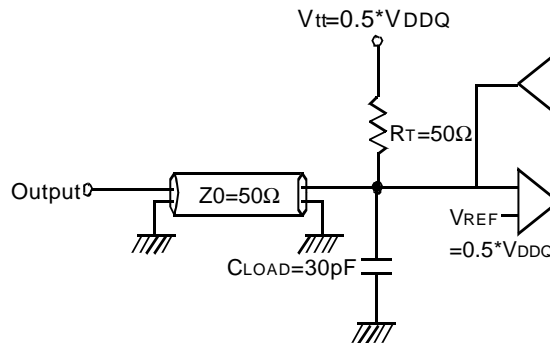
AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V _{IH} (AC)	V _{REF} + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V _{IL} (AC)		V _{REF} - 0.31	V	3
Input Differential Voltage, CK and CK inputs	V _{ID} (AC)	0.7	V _{DDQ} +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V _{IX} (AC)	0.5*V _{DDQ} -0.2	0.5*V _{DDQ} +0.2	V	2

- Note 1. V_{ID} is the magnitude of the difference between the input level on CK and the input on \overline{CK} .
 2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relative to a V_{ref} envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V _{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input Levels(V _{IH} /V _{IL})	V _{REF} +0.31/V _{REF} -0.31	V	
Input timing measurement reference level	V _{REF}	V	
Output timing measurement reference level	V _{tt}	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE (V_{DD}=2.5, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A ₀ ~ A ₁₂ , BA ₀ ~ BA ₁ , \overline{RAS} , \overline{CAS} , \overline{WE})	C _{IN1}	-	12	pF
Input capacitance(CKE ₀)	C _{IN2}	-	12	pF
Input capacitance(\overline{CS} ₀)	C _{IN3}	-	11	pF
Input capacitance(CLK ₀ , /CLK ₀)	C _{IN4}	-	12	pF
Input capacitance(DM ₀ ~DM ₈)	C _{IN5}	-	16	pF
Data & DQS input/output capacitance(DQ ₀ ~DQ ₆₃)	C _{OUT1}	-	16	pF
Data input/output capacitance(CB ₀ ~CB ₇)	C _{OUT2}	-	16	pF

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AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)

Parameter	Symbol	-TCA2 (DDR266A)		-TCB0 (DDR266B)		-TCA0 (DDR200)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	65		65		70		ns		
Refresh row cycle time	tRFC	75		75		80		ns		
Row active time	tRAS	45	120K	45	120K	48	120K	ns		
RAS to CAS delay	tRCD	20		20		20		ns		
Row precharge time	tRP	20		20		20		ns		
Row active to Row active delay	tRRD	15		15		15		ns		
Write recovery time	tWR	15		15		15		ns		
Last data in to Read command	tWTR	1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	10	12	10	12	ns	5
		CL=2.5	7.5	12	7.5	12			ns	5
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Output data access time from CK/CK	tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data strobe edge to output data edge	tDQSQ	-	0.5	-	0.5	-	0.6	ns	5	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		ns	2	
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time(fast)	tIS	0.9		0.9		1.1		ns	6	
Address and Control Input hold time(fast)	tIH	0.9		0.9		1.1		ns	6	
Address and Control Input setup time(slow)	tIS	1.0		1.0		1.1		ns	6	
Address and Control Input hold time(slow)	tIH	1.0		1.0		1.1		ns	6	
Data-out high impedance time from CK/CK	tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data-out low impedance time from CK/CK	tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		0.5		V/ns	6	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ns	7	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5			

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Parameter	Symbol	-TCA2 (DDR266A)		-TCB0 (DDR266B)		-TCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		0.5		0.6		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		2.2		2.5		ns	
DQ & DM input pulse width	tDIPW	1.75		1.75		2		ns	
Power down exit time	tPDEX	7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		80		ns	4
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	tREFI	7.8		7.8		7.8		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Active to Read with Auto precharge command	tRAP	20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

- Maximum burst refresh cycle : 8
- The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with tRCD satisfied after this command.
- For registered DIMMs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
- Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

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8. I/O Setup/Hold Plateau Derating

I/O Input Level	Δt_{DS}	Δt_{DH}
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below $V_{REF} \pm 310mV$ for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	Δt_{DS}	Δt_{DH}
(ns/V)	(ps)	(ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as $1/SlewRate1-1/SlewRate2$. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Reference>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	$\Delta t_{IH}/t_{IS}$ (ps)	$\Delta t_{DSS}/t_{DSH}$ (ps)	$\Delta t_{AC}/t_{DQSCK}$ (ps)	$\Delta t_{LZ}(\min)$ (ps)	$\Delta t_{HZ}(\max)$ (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

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Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA _{0,1}	A _{10/AP}	A _{11, A12} A _{9 ~ A0}	Note			
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2			
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2			
Refresh	Auto Refresh		H	H	L	L	L	H	X		3			
	Self Refresh	Entry		L										3
		Exit	L	H	L	H	H	H	X		3			
	H		X	X	X			3						
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address					
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	L	Column Address A _{0~A9, A11}	4			
	Auto Precharge Enable								H		4			
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	L	Column Address A _{0~A9, A11}	4			
	Auto Precharge Enable								H		4, 6			
Burst Stop		H	X	L	H	H	L	X			7			
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X			
	All Banks								X	H		5		
Active Power Down		Entry	H	L	H	X	X	X	X					
					L	V	V	V						
					L	H	X	X			X	X		
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X					
					L	H	H	H						
					Exit	L	H	H			X	X	X	
								L			V	V	V	
DM		H	X					X			8			
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9			
				L	H	H	H			9				

Note : 1. OP Code : Operand Code. A_{0 ~ A12} & BA_{0 ~ BA1} : Program keys. (@EMRS/MRS)

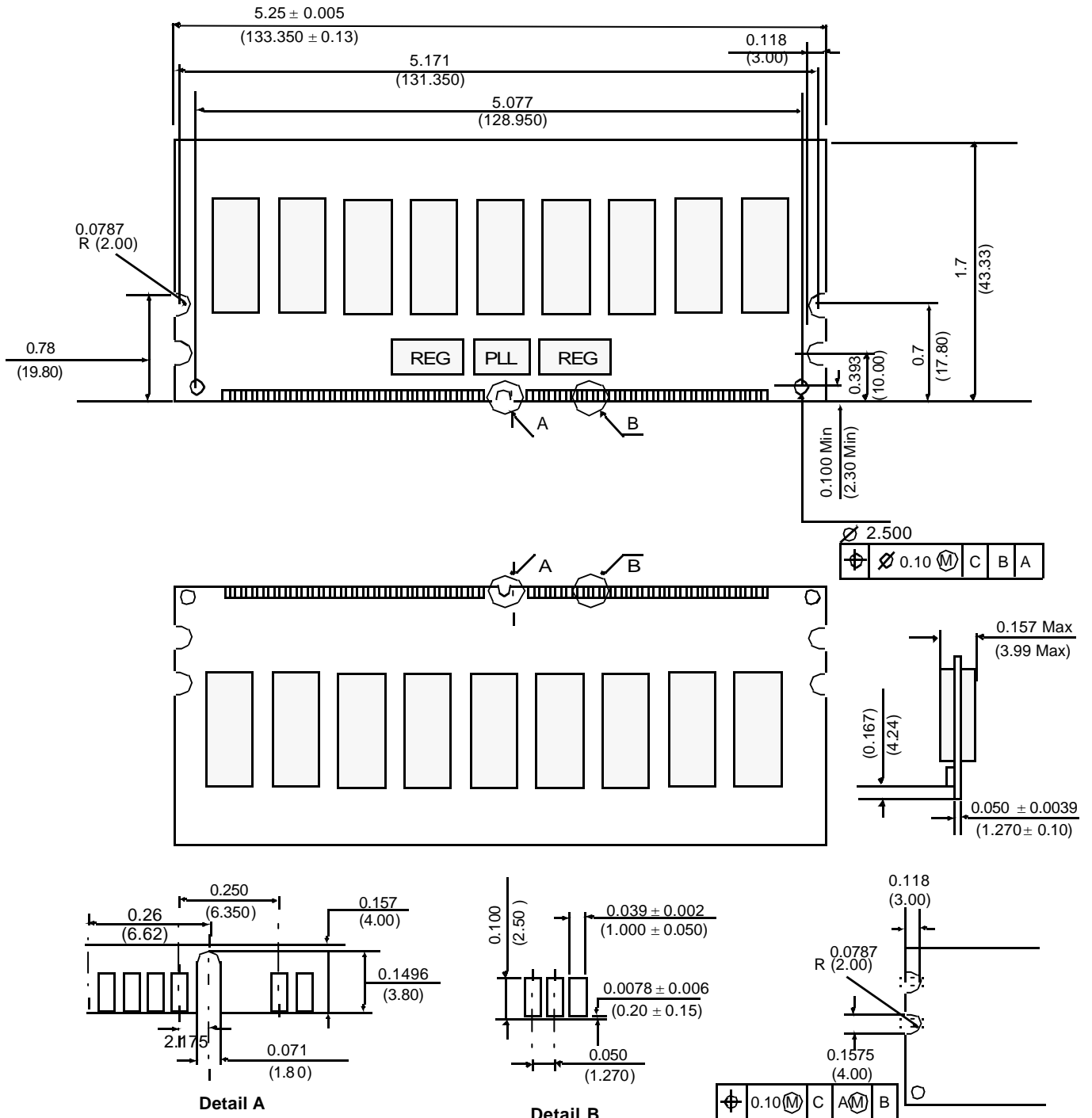
- EMRS/ MRS can be issued only at all banks precharge state.
A new command can be issued 2 clock cycles after EMRS or MRS.
- Auto refresh functions are same as the CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
- BA_{0 ~ BA1} : Bank select addresses.
If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.
If BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank B is selected.
If BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank C is selected.
If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.
- If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ are ignored and all banks are selected.
- During burst write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
- Burst stop command is valid at every burst length.
- DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
- This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

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PACKAGE DIMENSIONS

Units : Inches (Millimeters)

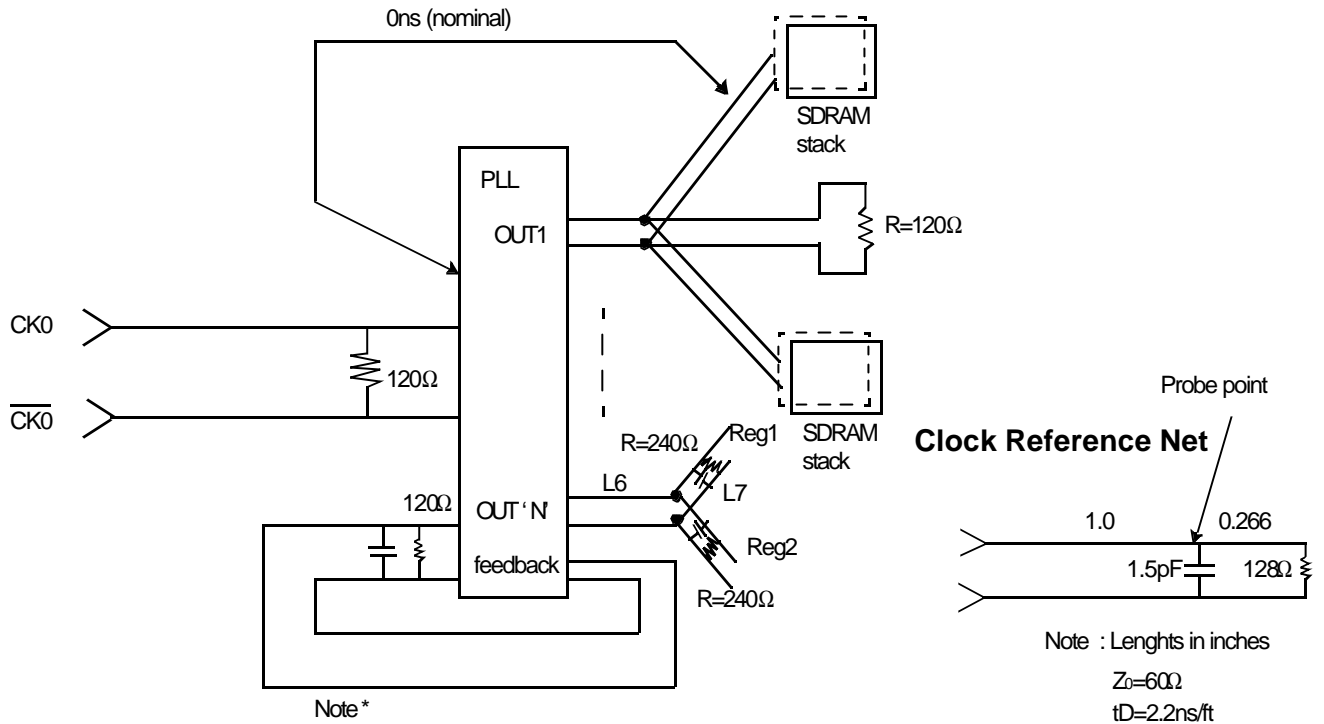


Tolerances : $\pm 0.005(.13)$ unless otherwise specified
 The used device is 64Mx4 SDRAM, TSOP
 SDRAM Part NO : K4H560438B-TC

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184 Pin DDR Registered DIMM Clock Topolgy



Notes* :

1. The Clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns(nominal).
2. Input,output, and feedback clock lines are terminated from line to leine as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar maner.
4. termination resistors for the PLL feedback path clocks are loacted after the pins of the PLL.