M390S3253CTU SDRAM DIMM

32Mx72 SDRAM DIMM with PLL & Register based on 32Mx8, 4Banks 8K Ref., 3.3V Synchronous DRAMs with SPD

GENERAL DESCRIPTION

The Samsung M390S3253CTU is a 32M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S3253CTU consists of nine CMOS 32Mx8 bit Synchronous DRAMs in TSOP-II 400mil packages, two 18-bits Drive ICs for input control signal and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S3253CTU is a Dual In-line Memory Module and is intented for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S3253CTU-C7C	133MHz (7.5ns @ CL=2)
M390S3253CTU-C7A	133MHz (7.5ns @ CL=3)
M390S3253CTU-C1H	100MHz (10ns @ CL=2)
M390S3253CTU-C1L	100MHz (10ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs
  Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,200mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	VSS	106	CB5	134	NC	162	VSS
23	VSS	51	NC	79	*CLK2	107	VSS	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

PIN NAMES

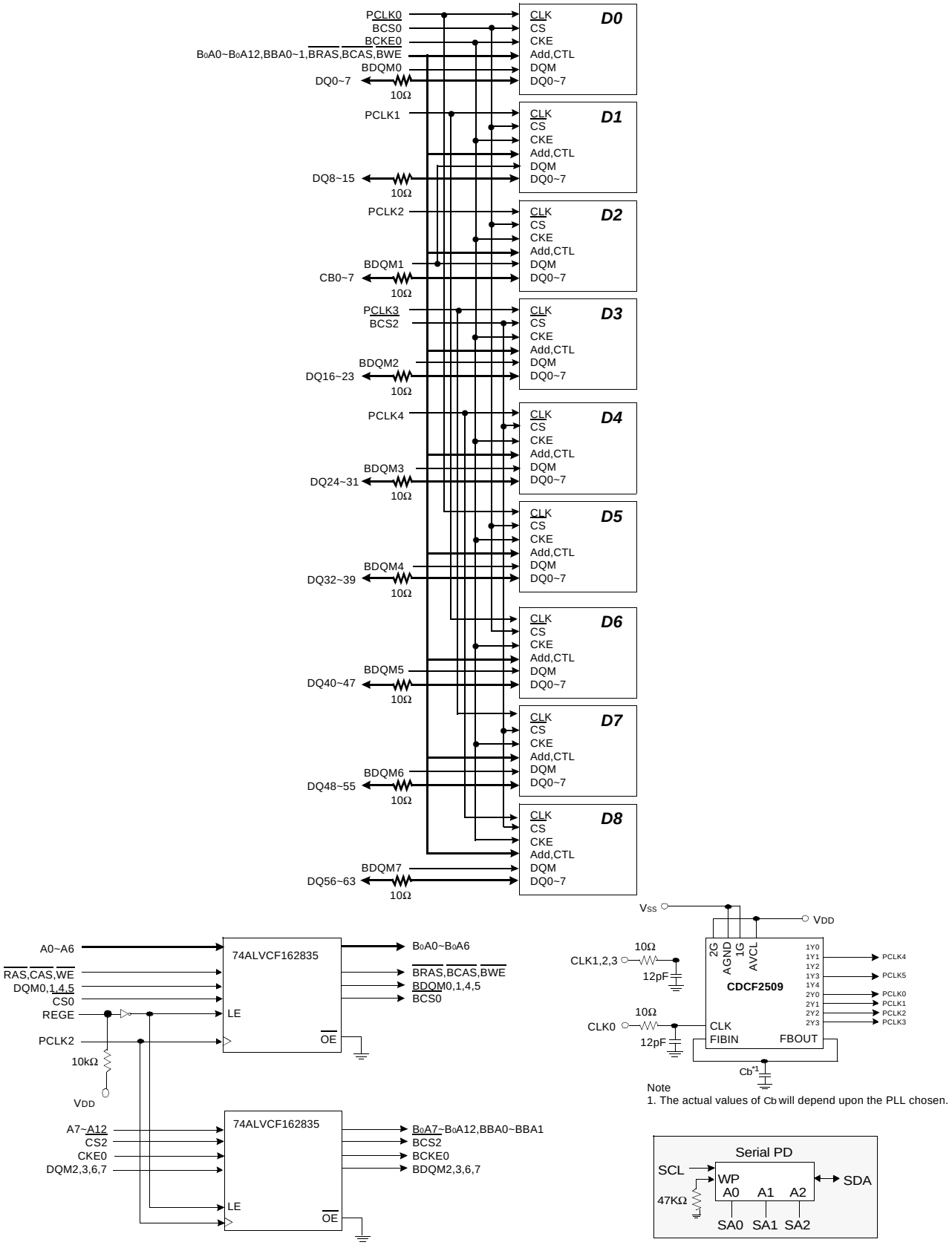
Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
$\overline{CS0}$, $\overline{CS2}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Colume address strobe
$\overline{WE}$	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
VSS	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

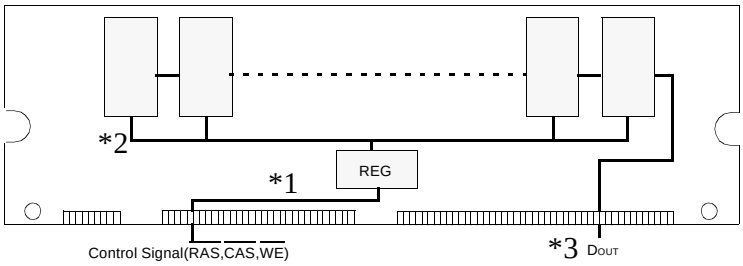
PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA9
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

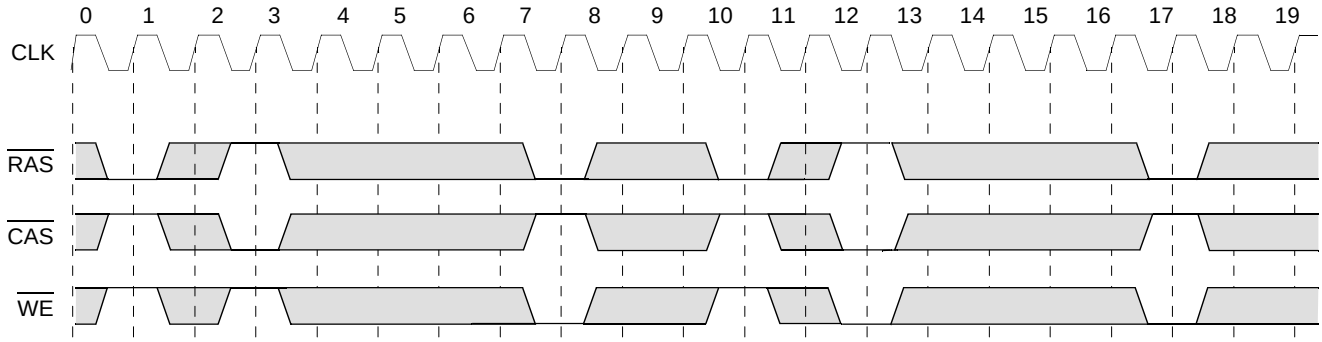
FUNCTIONAL BLOCK DIAGRAM



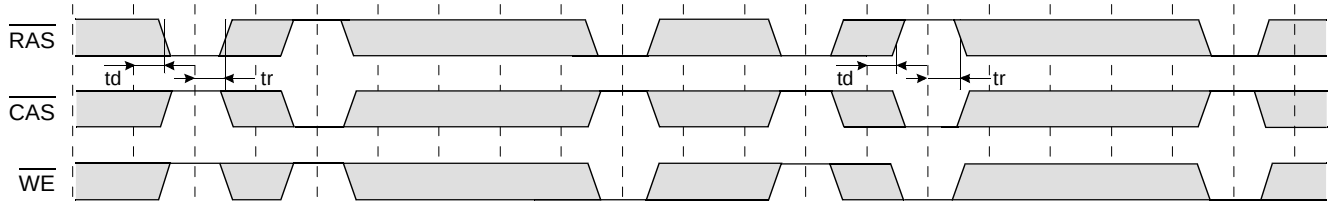
STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



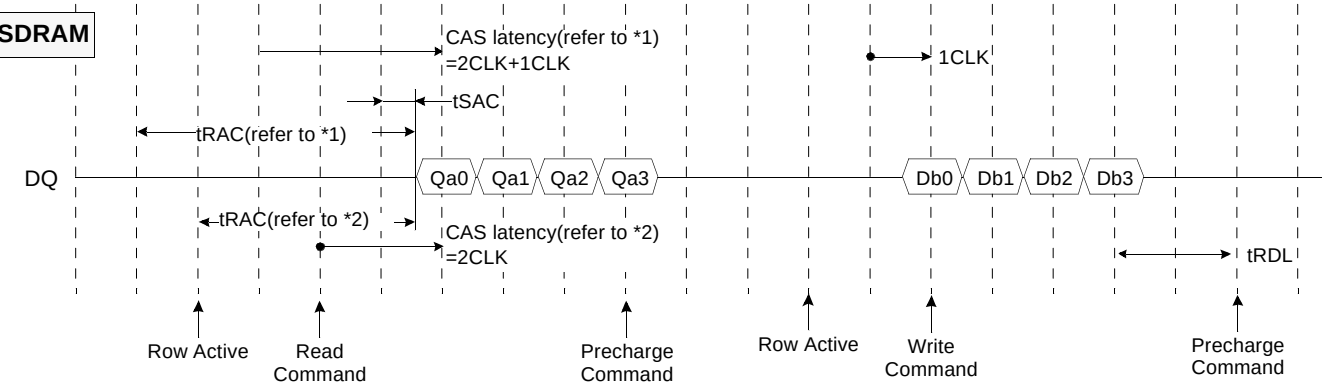
***1. Register Input**



***2. Register Output**



***3. SDRAM**



td, tr = Delay of register

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register . Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. DIN is to be issued 1clock after write command in external timing because DIN is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	9	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended Operating Conditions (Voltage Referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A_0 ~ A_{12})	C_{IN1}	-	15	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	-	15	pF
Input capacitance (CKE0)	C_{IN3}	-	15	pF
Input capacitance (CLK0)	C_{IN4}	-	23	pF
Input capacitance ($\overline{CS0}$, $\overline{CS2}$)	C_{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	-	15	pF
Input capacitance (BA0 ~ BA1)	C_{IN7}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	-	16	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}	-	16	pF

DC CHARACTERISTICS

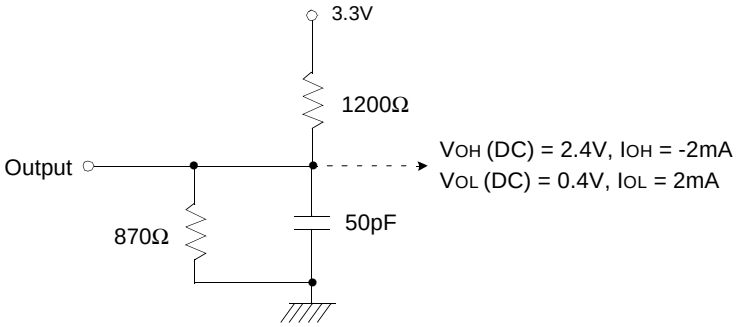
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version				Unit	Note
			- 7C	-7A	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	1400	1310	1310	1310	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	368				mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	20					
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	530				mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	92					
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	404				mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	56					
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	620				mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	227				mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1490	1490	1400	1400	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	2480	2300	2210	2210	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	377				mA	

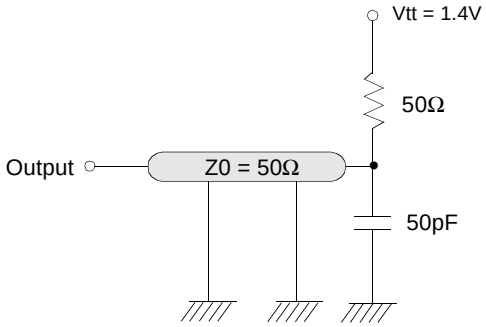
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version				Unit	Note
			- 7C	- 7A	- 1H	-1L		
Row active to row active delay		tRRD(min)	15	15	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	15	20	20	20	ns	1
Row precharge time		tRP(min)	15	20	20	20	ns	1
Row active time		tRAS(min)	45	45	50	50	ns	1
		tRAS(max)	100				us	
Row cycle time		tRC(min)	60	65	70	70	ns	1
Last data in to row precharge		tRDL(min)	2				CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + tRP				-	5
Last data in to new col. address delay		tCDL(min)	1				CLK	2
Last data in to burst stop		tBDL(min)	1				CLK	2
Col. address to col. address delay		tCCD(min)	1				CLK	3
Number of valid output data	CAS latency=3		2				ea	4
	CAS latency=2		1					

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	- 7C		- 7A		- 1H		- 1L		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		7.5		10		10		12			
CLK to valid output delay	CAS latency=3	tSAC		5.4		5.4		6		6	ns	1,2
	CAS latency=2			5.4		6		6		7		
Output data hold time	CAS latency=3	tOH	3		3		3		3		ns	2
	CAS latency=2		3		3		3		3			
CLK high pulse width		tCH	2.5		2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		2.5		3		3		ns	3
Input setup time		tSS	1.5		1.5		2		2		ns	3
Input hold time		tSH	0.8		0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4		5.4		6		6	ns	
	CAS latency=2			5.4		6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

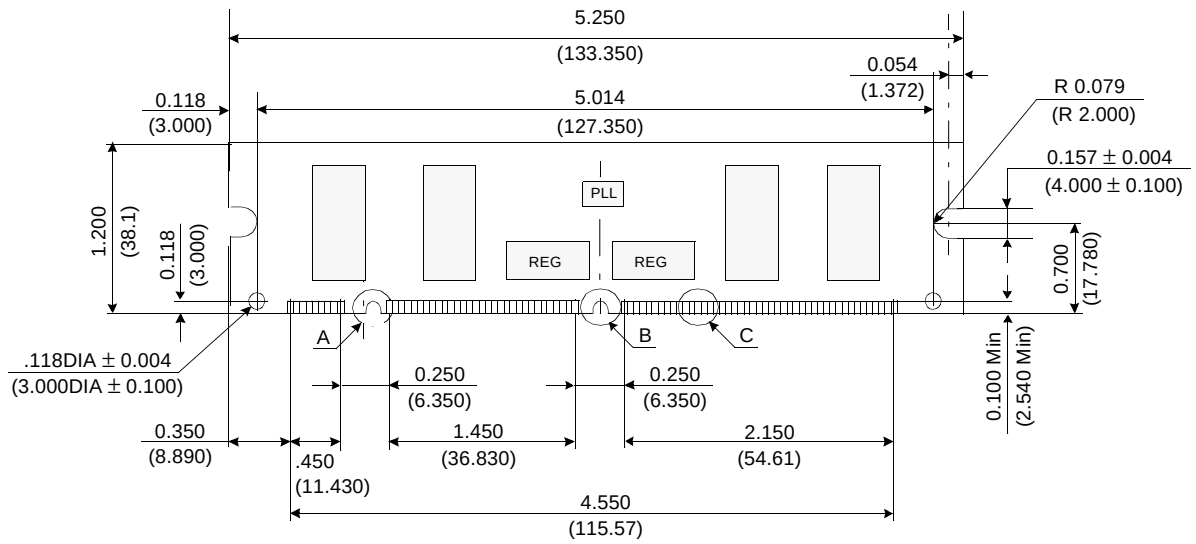
Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11},A_{12} $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_9$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

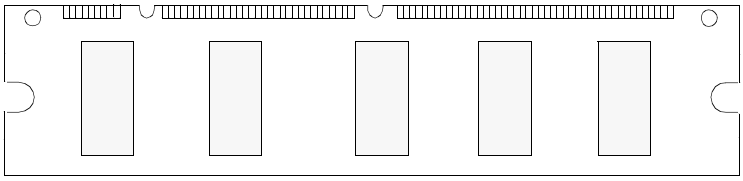
(V=Valid, X=Don't care, H=Logic high, L=Logic low)

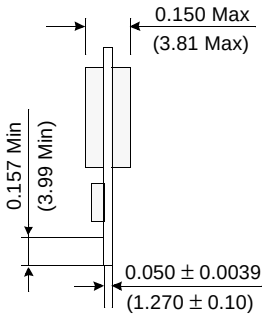
Notes :
1. OP Code : Operand code
   $A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

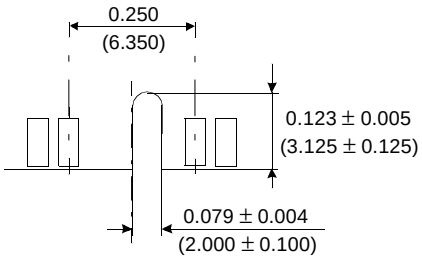
PACKAGE DIMENSIONS

Units : Inches (Millimeters)

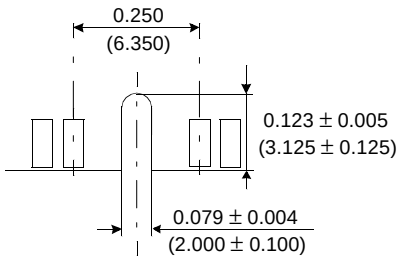




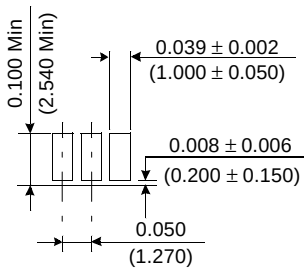




Detail A



Detail B



Detail C

Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOP
SDRAM Part No. : K4S560832C

M390S3253CTU-C7C/C7A/C1H/C1L

•Organization : 32MX72
•Composition : 32MX8 * 9ea
•Used component part # : K4S560832C
•# of rows in module : 1 Row
•# of rows in component : 4 banks
•Feature : 1,200 mil height & double sided
•Refresh : 8K/64ms
•**Contents** :

Byte #	Function described	Function Supported				Hex value				Note
		-7C	-7A	-1H	-1L	-7C	-7A	-1H	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes				80h				
1	Total # of bytes of SPD memory device	256bytes (2K-bit)				08h				
2	Fundamental memory type	SDRAM				04h				
3	# of row address on this assembly	13				0Dh				1
4	# of column address on this assembly	10				0Ah				1
5	# of module Rows on this assembly	1 row				01h				
6	Data width of this assembly	72 bits				48h				
7	..... Data width of this assembly	-				00h				
8	Voltage interface standard of this assembly	LVTTL				01h				
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	10ns	10ns	10ns	75h	75h	A0h	A0h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	6ns	6ns	6ns	54h	54h	60h	60h	2
11	DIMM configuration type	ECC				02h				
12	Refresh rate & type	7.8us, support self refresh				82h				
13	Primary SDRAM width	x8				08h				
14	Error checking SDRAM width	x8				08h				
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK				01h				
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page				8Fh				
17	SDRAM device attributes : # of banks on SDRAM device	4 banks				04h				
18	SDRAM device attributes : CAS latency	2 & 3				06h				
19	SDRAM device attributes : CS latency	0 CLK				01h				
20	SDRAM device attributes : Write latency	0 CLK				01h				
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-card PLL				1Fh				
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge				0Eh				
23	SDRAM cycle time @CAS latency of 2	7.5ns	10ns	10ns	12ns	75h	A0h	A0h	C0h	2
24	SDRAM access time @CAS latency of 2	5.4ns	6ns	6ns	7ns	54h	60h	60h	70h	2
25	SDRAM cycle time @CAS latency of 1	-				00h				
26	SDRAM access time @CAS latency of 1	-				00h				
27	Minimum row precharge time (=tRP)	15ns	20ns	20ns	20ns	0Fh	14h	14h	14h	
28	Minimum row active to row active delay (tRRD)	15ns	15ns	20ns	20ns	0Fh	0Fh	14h	14h	
29	Minimum RAS to CAS delay (=tRCD)	15ns	20ns	20ns	20ns	0Fh	14h	14h	14h	
30	Minimum activate precharge time (=tRAS)	45ns	45ns	50ns	50ns	2Dh	2Dh	32h	32h	
31	Module Row density	1 Row of 256MB				40h				
32	Command and Address signal input setup time	1.5ns	1.5ns	2ns	2ns	15h	15h	20h	20h	
33	Command and Address signal input hold time	0.8ns	0.8ns	1ns	1ns	08h	08h	10h	10h	
34	Data signal input setup time	1.5ns	1.5ns	2ns	2ns	15h	15h	20h	20h	

Byte #	Function Described	Function Supported				Hex value				Note
		-7C	-7A	-1H	-1L	-7C	-7A	-1H	-1L	
35	Data signal input hold time	0.8ns	0.8ns	1ns	1ns	08h	08h	10h	10h	
36~61	Superset information (maybe used in future)	-				00h				
62	SPD data revision code	Intel Rev 1.2B				12h				
63	Checksum for bytes 0 ~ 62	-				C2h	03h	6Ah	9Ah	
64	Manufacturer JEDEC ID code	Samsung				CEh				
65~71	..... Manufacturer JEDEC ID code	Samsung				00h				
72	Manufacturing location	Onyang Korea				01h				
73	Manufacturer part # (Memory module)	M				4Dh				
74	Manufacturer part # (DIMM Configuration)	3				33h				
75	Manufacturer part # (Data bits)	Blank				20h				
76	..... Manufacturer part # (Data bits)	9				39h				
77	..... Manufacturer part # (Data bits)	0				30h				
78	Manufacturer part # (Mode & operating voltage)	S				53h				
79	Manufacturer part # (Module depth)	3				33h				
80	..... Manufacturer part # (Module depth)	2				32h				
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	5				35h				
82	Manufacturer part # (Composition component)	3				33h				
83	Manufacturer part # (Component revision)	C				43h				
84	Manufacturer part # (Package type)	T				54h				
85	Manufacturer part # (PCB revision & type)	U				55h				
86	Manufacturer part # (Hyphen)	" - "				2Dh				
87	Manufacturer part # (Power)	C				43h				
88	Manufacturer part # (Minimum cycle time)	7	7	1	1	37h	37h	31h	31h	
89	Manufacturer part # (Minimum cycle time)	C	A	H	L	43h	41h	48h	4Ch	
90	Manufacturer part # (TBD)	Blank				20h				
91	Manufacturer revision code (For PCB)	U				55h				
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)				43h				
93	Manufacturing date (Year)	-				-				3
94	Manufacturing date (Week)	-				-				3
95~98	Assembly serial #	-				-				4
99~125	Manufacturer specific data (may be used in future)	Undefined				-				
126	System frequency for 100MHz	100MHz				64h				
127	PC100 specification details	Detailed PC100 Information				8Fh	8Fh	8Fh	8Dh	
128+	Unused storage locations	Undefined				-				

Note : 1. The row select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year with BCD format.
4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung's own purpose.