64MB DDR SDRAM MODULE

(8Mx64 based on 8Mx16 DDR SDRAM)

172pin Micro DIMM
64-bit Non-ECC/Parity

Revision 0.1

Jan. 2002

Revision History

Revision 0.0 (Dec. 2001)

1. First release

Revision 0.1 (Jan, 2002)

1. Added tRAP(Active to Read w/ autoprecharge command)

M463L0914DT0 172pin DDR Micro DIMM

8Mx64 172pin DDR Micro DIMM based on 8Mx16

GENERAL DESCRIPTION

The Samsung M463L0914DT0 is 8M bit x 64 Double Data Rate SDRAM high density memory modules.

The Samsung M463L0914DT0 consists of four CMOS 8M x 16 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 172pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM.

The M463L0914DT0 is Dual In-line Memory Modules and intended for mounting into 172pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

• Performance range

Part No.	Max Freq.	Interface
M463L0914DT0-C(L)B3	166MHz(6ns@CL=2.5)	SSTL_2
M463L0914DT0-C(L)A2	133MHz(7.5ns@CL=2)	
M463L0914DT0-C(L)B0	133MHz(7.5ns@CL=2.5)	
M463L0914DT0-C(L)A0	100MHz(10ns@CL=2)	

• Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
• Double-data-rate architecture; two data transfers per clock cycle
• Bidirectional data strobe(DQS)
• Differential clock inputs(CK and $\overline{CK}$)
• DLL aligns DQ and DQS transition with CK transition
• Programmable Read latency 2, 2.5 (clock)
• Programmable Burst length (2, 4, 8)
• Programmable Burst type (sequential & interleave)
• Edge aligned data output, center aligned data input
• Auto & Self refresh, 15.6us refresh interval(4K/64ms refresh)
• Serial presence detect with EEPROM
• PCB :**Height1200mil**, double sided component

PIN CONFIGURATIONS (Front side/back side)

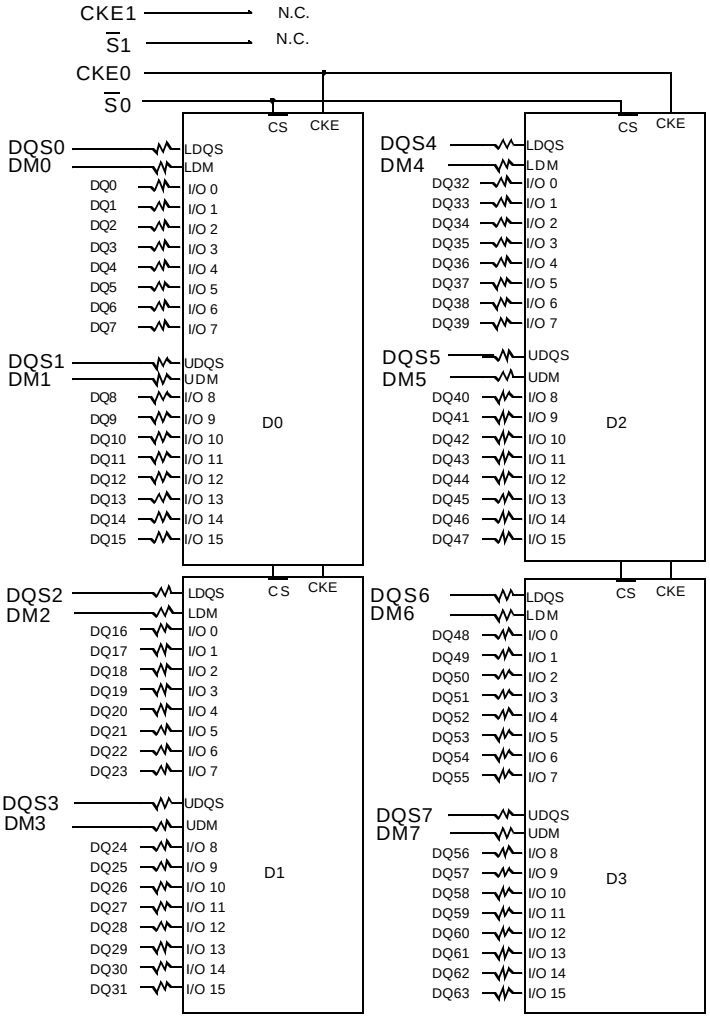
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{REF}	59	DQ25	117	V_{DD}	2	V_{REF}	60	DQ29	118	V_{DD}
3	V_{SS}	61	DQS3	119	DQ41	4	V_{SS}	62	DM3	120	DQ45
5	DQ0	63	V_{SS}	121	DQS5	6	DQ4	64	V_{SS}	122	DM5
7	DQ1	65	DQ26	123	V_{SS}	8	DQ5	66	DQ30	124	V_{SS}
9	V_{DD}	67	DQ27	125	DQ42	10	V_{DD}	68	DQ31	126	DQ46
11	DQS0	69	V_{DD}	127	DQ43	12	DM0	70	V_{DD}	128	DQ47
13	DQ2	71	CKE1	129	V_{DD}	14	DQ6	72	CKE0	130	V_{DD}
15	V_{SS}	73	A12	131	V_{DD}	16	V_{SS}	74	A11	132	$\overline{CK1}$
17	DQ3	75	A9	133	V_{SS}	18	DQ7	76	A8	134	CK1
19	DQ8	77	A7	135	V_{SS}	20	DQ12	78	A6	136	V_{SS}
21	V_{DD}	79	V_{SS}	137	DQ48	22	V_{DD}	80	V_{SS}	138	DQ52
23	DQ9	81	A5	139	DQ49	24	DQ13	82	A4	140	DQ53
25	DQS1	83	A3	141	V_{DD}	26	DM1	84	A2	142	V_{DD}
27	V_{SS}	85	A1	143	DQS6	28	V_{SS}	86	A0	144	DM6
29	DQ10	87	A10/AP	145	DQ50	30	DQ14	88	BA1	146	DQ54
31	DQ11	89	V_{DD}	147	V_{SS}	32	DQ15	90	$\overline{V_{DD}}$	148	V_{SS}
33	V_{DD}	91	$\overline{BA0}$	149	DQ51	34	V_{DD}	92	$\overline{RAS}$	150	DQ55
35	$\overline{CK0}$	93	$\overline{WE}$	151	DQ56	36	V_{DD}	94	$\overline{CAS}$	152	DQ60
37	CK0	95	$\overline{S0}$	153	V_{DD}	38	V_{SS}	96	$\overline{S1}$	154	V_{DD}
39	V_{SS}	97	A13	155	DQ57	40	V_{SS}	98	RFU	156	DQ61
41	DQ16	99	V_{SS}	157	DQS7	42	DQ20	100	V_{SS}	158	DM7
43	DQ17	101	DQ32	159	V_{SS}	44	DQ21	102	DQ36	160	V_{SS}
45	V_{DD}	103	DQ33	161	DQ58	46	V_{DD}	104	DQ37	162	DQ62
47	DQS2	105	V_{DD}	163	DQ59	48	DM2	106	V_{DD}	164	DQ63
49	DQ18	107	DQS4	165	V_{DD}	50	DQ22	108	DM4	166	V_{DD}
51	V_{SS}	109	DQ34	167	SDA	52	V_{SS}	110	DQ38	168	SA0
53	DQ19	111	V_{SS}	169	SCL	54	DQ23	112	V_{SS}	170	SA1
55	DQ24	113	DQ35	171	V_{DD}SPD	56	DQ28	114	DQ39	172	SA2
57	V_{DD}	115	DQ40			58	V_{DD}	116	DQ44		

PIN DESCRIPTION

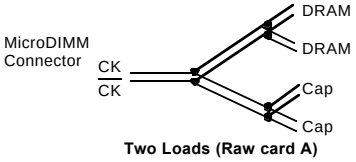
Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
$\overline{CK0}$~ CK1, $\overline{CK0}$~ $\overline{CK1}$	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DM0 ~ DM7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

* These pins are not used in this module.

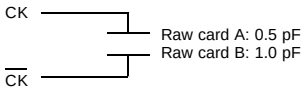
FUNCTIONAL BLOCK DIAGRAM



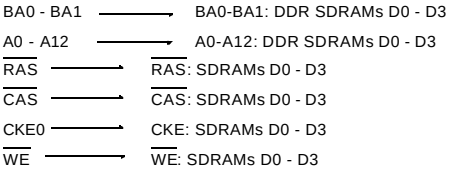
Load matching Capacitors on	X pF	
	Raw card A	Raw card B
A0-AN RAS CAS WE CKE0 S0	10 pF	10 pF

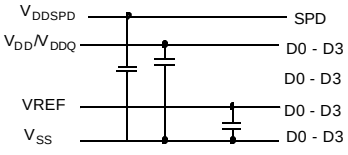


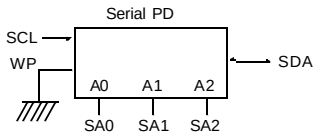
Two Loads (Raw card A)



Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	2 SDRAMs + 2Caps
CK1/CK1	2 SDRAMs + 2Caps







Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.

Absolute Maximum Rate

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	6	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and $\overline{CK}$ inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Notes 1. Includes± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.
6. These characterictics obey the SSTL-2 class II standards.

DDR SDRAM module IDD spec table

Symbol		B3(DDR333@CL=2.5)	A2(DDR266@CL=2) B0(DDR266@CL=2.5)	A0(DDR200@CL=2)	Unit	Notes
IDD0		360	320	300	mA	
IDD1		460	400	380	mA	
IDD2P		12	10	10	mA	
IDD2F		112	96	80	mA	
IDD2Q		72	60	60	mA	
IDD3P		140	140	140	mA	
IDD3N		220	200	200	mA	
IDD4R		660	580	540	mA	
IDD4W		600	500	420	mA	
IDD5		720	580	560	mA	
IDD6	Normal	8	8	8	mA	
	Low power	4	4	4	mA	Optional
IDD7A		1380	1200	1020	mA	

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

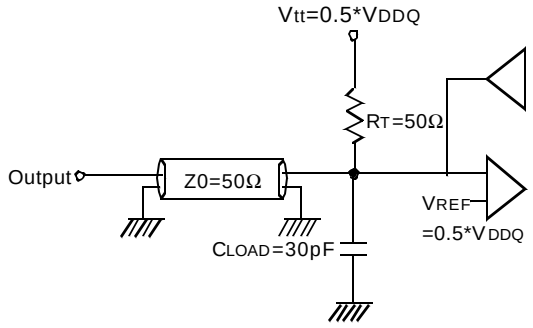
AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note 1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V_{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.31/V_{REF}-0.31	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0 ~ A_{11}, BA_0 ~ BA_1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN1}	29	34	pF
Input capacitance(CKE_0)	C_{IN2}	29	34	pF
Input capacitance($\overline{CS}_0$)	C_{IN3}	26	30	pF
Input capacitance(CLK_0, CLK_1)	C_{IN4}	30	32	pF
Data & DQS input/output capacitance(DQ_0~DQ_{63})	C_{OUT}	8	9	pF
Input capacitance(DM_0~DM_8)	C_{IN5}	8	9	pF

AC Timming Parameters & Specifications

Parameter		Symbol	-TCB3 (DDR333)		-TCA2 (DDR266A)		-TCB0 (DDR266B)		-TCA0 (DDR200)		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	60		65		65		70		ns	
Refresh row cycle time		tRFC	72		75		75		80		ns	
Row active time		tRAS	42	70K	45	120K	45	120K	48	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	18		20		20		20		ns	
Row precharge time		tRP	18		20		20		20		ns	
Row active to Row active delay		tRRD	12		15		15		15		ns	
Write recovery time		tWR	15		15		15		15		ns	
Last data in to Read command		tWTR	1		1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	7.5	12	10	12	10	12	ns	5
	CL=2.5		6	12	7.5	12	7.5	12			ns	5
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.45	-	0.5	-	0.5	-	0.6	ns	5
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		0		ns	2
DQS-in hold time		tWPRE	0.25		0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time(fast)		tIS	0.75		0.9		0.9		1.1		ns	6
Address and Control Input hold time(fast)		tIH	0.75		0.9		0.9		1.1		ns	6
Address and Control Input setup time(slow)		tIS	0.8		1.0		1.0		1.1		ns	6
Address and Control Input hold time(slow)		tIH	0.8		1.0		1.0		1.1		ns	6
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Input Slew Rate(for input only pins)		tSL(I)	0.5		0.5		0.5		0.5		V/ns	6
Input Slew Rate(for I/O pins)		tSL(IO)	0.5		0.5		0.5		0.5		V/ns	7
Output Slew Rate(x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate Matching Ratio(rise to fall)		tSLMR	0.67	1.5	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter	Symbol	-TCB3 (DDR333)		-TCA2 (DDR266A)		-TCB0 (DDR266B)		-TCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	12		15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.45		0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.45		0.5		0.5		0.6		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		2.2		2.2		2.5		ns	
DQ & DM input pulse width	tDIPW	1.75		1.75		1.75		2		ns	
Power down exit time	tPDEX	6		7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		75		80		ns	4
Exit self refresh to read command	tXSRD	200		200		200		200		tCK	
Refresh interval time	tREFI	15.6		15.6		15.6		15.6		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.55		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Active to Read with Auto precharge command	tRAP	18		20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

1. Maximum burst refresh cycle : 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	ΔtDS	ΔtDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.
11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Reference>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	ΔtIH/tIS (ps)	ΔtDSS/tDSH (ps)	ΔtAC/tDQSCK (ps)	ΔtLZ(min) (ps)	ΔtHZ(max) (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

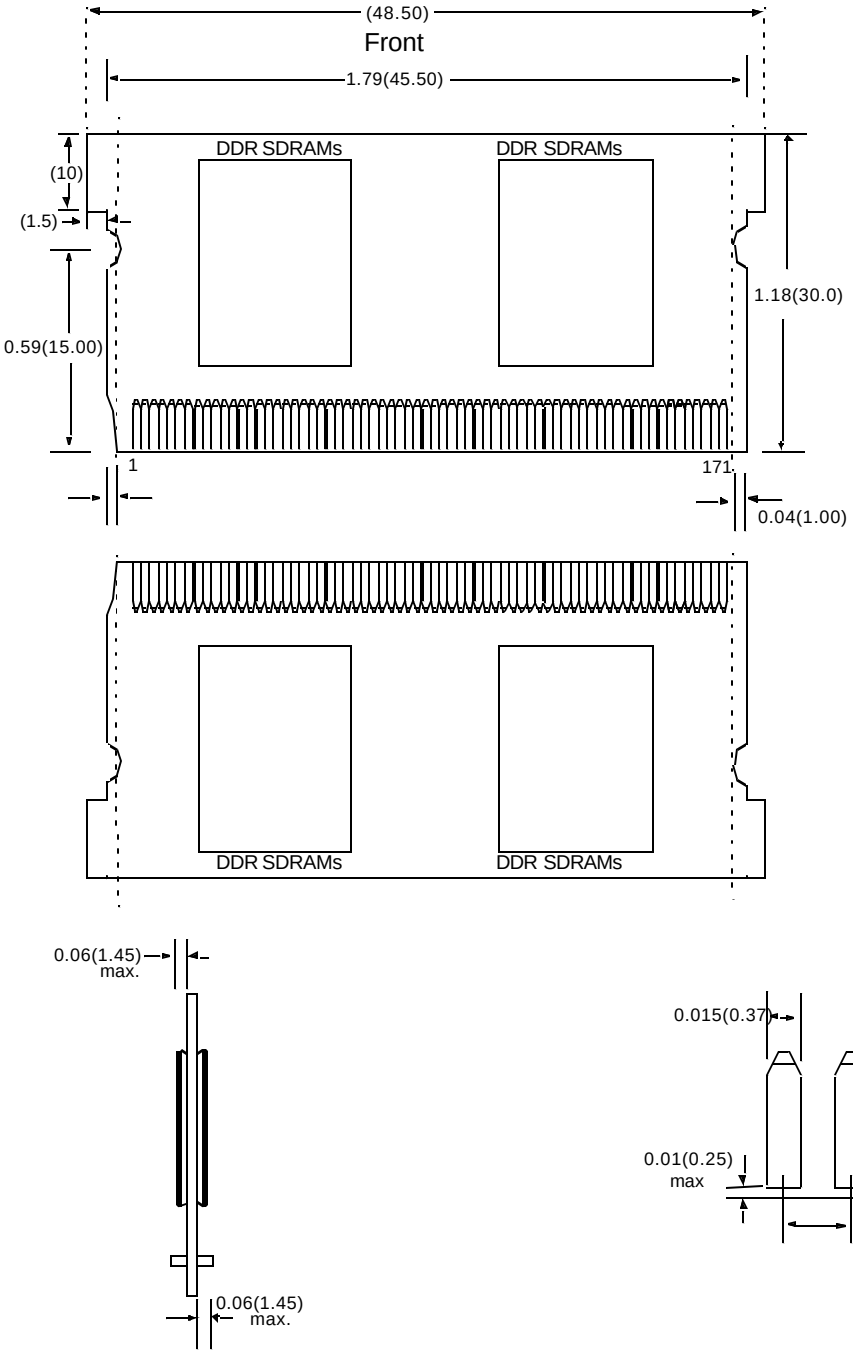
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$BA_{0,1}$	A_{10}/AP	A_{11} $A_9 \sim A_0$	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address ($A_0 \sim A_8$)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note : 1. OP Code : Operand Code. $A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ±.01(.25) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOP
SDRAM Part No. : K4H281638D