

M463L1624BT0

172pin DDR Micro DIMM

128MB DDR SDRAM MODULE

(16Mx64 based on 16Mx16 DDR SDRAM)

172pin Micro DIMM
64-bit Non-ECC/Parity

Revision 0.4

Dec. 2001

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Revision History

Revision 0.0 (Apr. 2001)

1. First release

Revision 0.1 (May. 2001)

Changed the Package Dimension.

Revision 0.2 (June. 2001)

1. Changed module current specification
2. Changed typo size on module PCB in package dimensions. (from 2.6mm to 3mm).
3. Changed AC parameter table.

Revision 0.3 (July. 2001)

1. Changed typo size on module PCB in package dimensions.

Revision 0.4 (Dec. 2001)

- Add derating values for the specifications if the single-ended clock skew rate is less than 1.0V/ns in page 47.
- Revised "Absolute maximum rating" table in page 38.
 - . Changed "Voltage on VDDQ supply relative to VSS" value from -0.5~3.6V to -1~3.6V
 - . Changed "power dissipation" value from 1.0W to 1.5W.
- Revised AC parameter table

	From						To					
	DDR266A		DDR266B		DDR200		DDR266A		DDR266B		DDR200	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
tHZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tLZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tWPST (tCK)	0.25		0.25		0.25		0.4	0.6	0.4	0.6	0.4	0.6
tPDEX	10ns		10ns		10ns		7.5ns		7.5ns		10ns	

- Deleted typical current in IDD spec. table
- Included address and control input setup/hold time(tIS/tIH) at slow slew rate in DDR200/266 AC specification
- Deleted Exit self refresh to write command(tXSW) in DDR200/266 AC specification
- Rename tXSA(exit self refresh to bank active command) to tXSNR(exit self refresh to non read command) at DDR200/266
- Rename tXSR(exit self refresh to read command) to tXSRD at DDR200/266
- Rename tWPREH(DQS in hold time) to tWPRE at DDR200/266
- Rename tREF(Refresh interval time) to tREFI at DDR200/266
- Changed tWR value from 2tCK to 15ns.
- Rename tCDLR(Write data out to Read command) to tWTR
- Added tDAL(tWR+tRP)

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16Mx64 172pin DDR Micro DIMM based on 16Mx16

GENERAL DESCRIPTION

The Samsung M463L1624BT0 is 16M bit x 64 Double Data Rate SDRAM high density memory modules based on first gen of 256Mb DDR SDRAM respectively.

The Samsung M463L1624BT0 consists of four CMOS 16M x 16 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 172pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM.

The M463L1624BT0 is Dual In-line Memory Modules and intended for mounting into 172pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq.	Interface
M463L1624BT0-C(L)A2	133MHz(7.5ns@CL=2)	SSTL_2
M463L1624BT0-C(L)B0	133MHz(7.5ns@CL=2.5)	
M463L1624BT0-C(L)A0	100MHz(10ns@CL=2)	

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and \overline{CK})
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB :Height 1200 (mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V _{REF}	59	DQ25	117	V _{DD}	2	V _{REF}	60	DQ29	118	V _{DD}
3	V _{SS}	61	DQS3	119	DQ41	4	V _{SS}	62	DM3	120	DQ45
5	DQ0	63	V _{SS}	121	DQS5	6	DQ4	64	V _{SS}	122	DM5
7	DQ1	65	DQ26	123	V _{SS}	8	DQ5	66	DQ30	124	V _{SS}
9	V _{DD}	67	DQ27	125	DQ42	10	V _{DD}	68	DQ31	126	DQ46
11	DQS0	69	V _{DD}	127	DQ43	12	DM0	70	V _{DD}	128	DQ47
13	DQ2	71	CKE1	129	V _{DD}	14	DQ6	72	CKE0	130	V _{DD}
15	V _{SS}	73	A12	131	V _{DD}	16	V _{SS}	74	A11	132	CK1
17	DQ3	75	A9	133	V _{SS}	18	DQ7	76	A8	134	CK1
19	DQ8	77	A7	135	V _{SS}	20	DQ12	78	A6	136	V _{SS}
21	V _{DD}	79	V _{SS}	137	DQ48	22	V _{DD}	80	V _{SS}	138	DQ52
23	DQ9	81	A5	139	DQ49	24	DQ13	82	A4	140	DQ53
25	DQS1	83	A3	141	V _{DD}	26	DM1	84	A2	142	V _{DD}
27	V _{SS}	85	A1	143	DQS6	28	V _{SS}	86	A0	144	DM6
29	DQ10	87	A10/AP	145	DQ50	30	DQ14	88	BA1	146	DQ54
31	DQ11	89	V _{DD}	147	V _{SS}	32	DQ15	90	V _{DD}	148	V _{SS}
33	V _{DD}	91	BA0	149	DQ51	34	V _{DD}	92	RAS	150	DQ55
35	CK0	93	WE	151	DQ56	36	V _{DD}	94	CAS	152	DQ60
37	CK0	95	S0	153	V _{DD}	38	V _{SS}	96	S1	154	V _{DD}
39	V _{SS}	97	A13	155	DQ57	40	V _{SS}	98	RFU	156	DQ61
41	DQ16	99	V _{SS}	157	DQS7	42	DQ20	100	V _{SS}	158	DM7
43	DQ17	101	DQ32	159	V _{SS}	44	DQ21	102	DQ36	160	V _{SS}
45	V _{DD}	103	DQ33	161	DQ58	46	V _{DD}	104	DQ37	162	DQ62
47	DQS2	105	V _{DD}	163	DQ59	48	DM2	106	V _{DD}	164	DQ63
49	DQ18	107	DQS4	165	V _{DD}	50	DQ22	108	DM4	166	V _{DD}
51	V _{SS}	109	DQ34	167	SDA	52	V _{SS}	110	DQ38	168	SA0
53	DQ19	111	V _{SS}	169	SCL	54	DQ23	112	V _{SS}	170	SA1
55	DQ24	113	DQ35	171	V _{DD} SPD	56	DQ28	114	DQ39	172	SA2
57	V _{DD}	115	DQ40			58	V _{DD}	116	DQ44		

PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0~ CK1, CK0~ CK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DM0 ~ DM7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

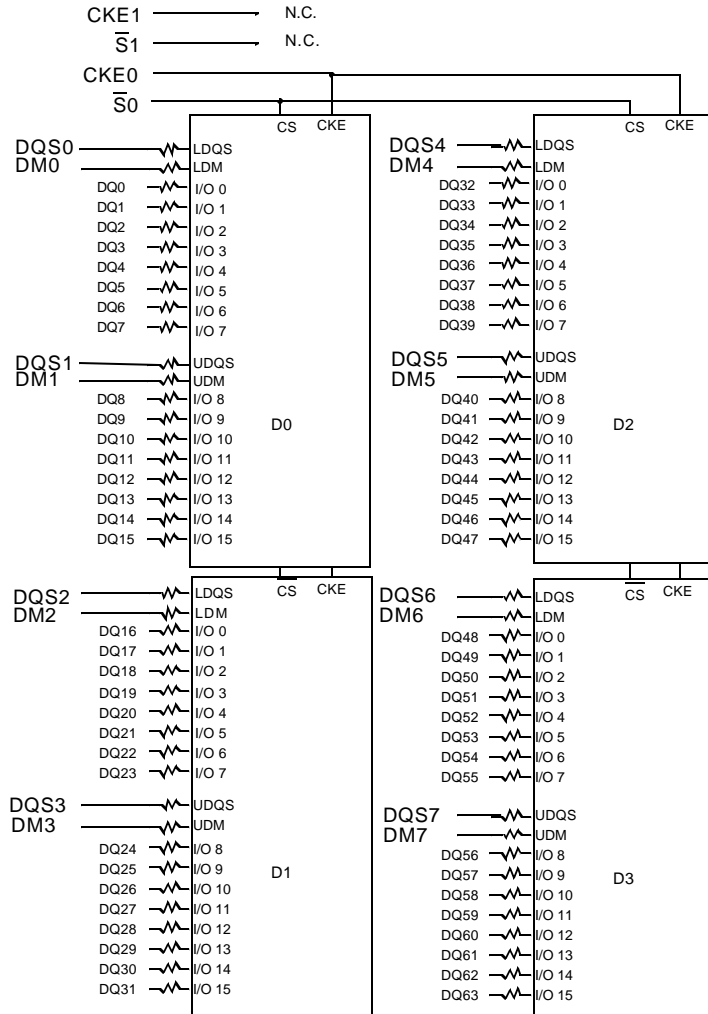
* These pins are not used in this module.

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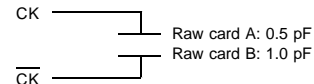
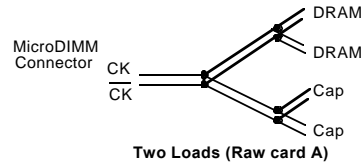
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FUNCTIONAL BLOCK DIAGRAM

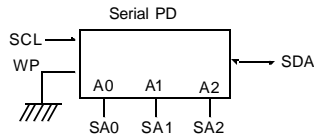
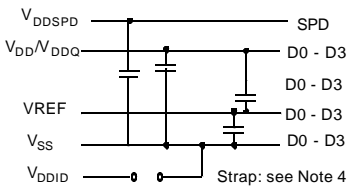


Load matching Capacitors on	$\frac{1}{s} \times \text{pF}$	
	Raw card A	Raw card B
A0-AN RAS CAS WE CKE0 S0	10 pF	10 pF



Clock Wiring	
Clock Input	SDRAMs
CK0, CK0-bar	2 SDRAMs + 2Caps
CK1, CK1-bar	2 SDRAMs + 2Caps

BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D3
 A0 - A12 → A0-A12: DDR SDRAMs D0 - D3
 RAS → RAS: SDRAMs D0 - D3
 CAS → CAS: SDRAMs D0 - D3
 CKE0 → CKE: SDRAMs D0 - D3
 WE → WE: SDRAMs D0 - D3



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. VDDID strap connections (for memory device VDD, VDDQ):
 STRAP OUT (OPEN): VDD = VDDQ
 STRAP IN (VSS): VDD ≠ VDDQ.

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Absolute Maximum Rate

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	6	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to $V_{SS}=0V$, $T_A=0$ to $70^{\circ}C$)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	$V_{DDQ}/2-50mV$	$V_{DDQ}/2+50mV$	V	1
I/O Termination voltage(system)	V_{TT}	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	4
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	4
Input Voltage Level, CK and \overline{CK} inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and \overline{CK} inputs	$V_{ID}(DC)$	0.3	$V_{DDQ}+0.6$	V	3
Input crossing point voltage, CK and \overline{CK} inputs	$V_{IX}(DC)$	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	I_{OH}	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	I_{OL}	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	I_{OH}	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	I_{OL}	9		mA	

- Notes**
- Includes $\pm 25mV$ margin for DC offset on V_{REF} , and a combined total of $\pm 50mV$ margin for all AC noise and DC offset on V_{REF} , bandwidth limited to 20MHZ. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF} , both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of $\leq 3nH$.
 - V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} , and must track variations in the DC level of V_{REF}
 - V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK} .
 - These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
 - The value of V_{IX} is expected to equal $0.5 \cdot V_{DDQ}$ of the transmitting device and must track variations in the dc level of the same.
 - These characteristics obey the SSTL-2 class II standards.

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DDR SDRAM SPEC Items and Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	IDD1
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); Vin = Vref for DQ,DQS and DM	IDD2P
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	IDD2F
Precharge Quiet standby current; CS# > = VIH(min); All banks idle; CKE > = VIH(min); Address and other control inputs stable with keeping >= VIH(min) or =<VIL(max); Vin = Vref for DQ ,DQS and DM	IDD2Q
Active power - down standby current ; one bank active; power-down mode; CKE=< VIL (max); Vin = Vref for DQ,DQS and DM	IDD3P
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; 50% of data changing at every burst; Iout = 0 m A	IDD4R
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W
Auto refresh current; tRC = tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz ; distributed refresh	IDD5
Self refresh current; CKE =< 0.2V; External clock should be on; tCK = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B	IDD6
Orerating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7A

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DDR SDRAM I_{DD} spec table

Symbol	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	A0(DDR200@CL=2)	Unit	Notes
IDD0	480	480	440	mA	
IDD1	660	660	600	mA	
IDD2P	128	128	100	mA	
IDD2F	220	220	180	mA	
IDD2Q	180	180	140	mA	
IDD3P	200	200	160	mA	
IDD3N	280	280	220	mA	
IDD4R	1040	1040	880	mA	
IDD4W	1260	1260	1000	mA	
IDD5	900	900	820	mA	
IDD6	Normal	12	12	mA	
	Low power	6	6	mA	Optional
IDD7A	1720	1720	1520	mA	

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

< Detailed test conditions for DDR SDRAM IDD1 & IDD7 >

IDD1 : Operating current: One bank operation

- Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{out} = 0mA
- Timing patterns
 - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
 - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
 - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

IDD7A : Operating current: Four bank operation

- Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. I_{out} = 0mA
- Timing patterns
 - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with autoprerecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst
 - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
Read with autoprerecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst
 - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK, Read with autoprerecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
*100% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

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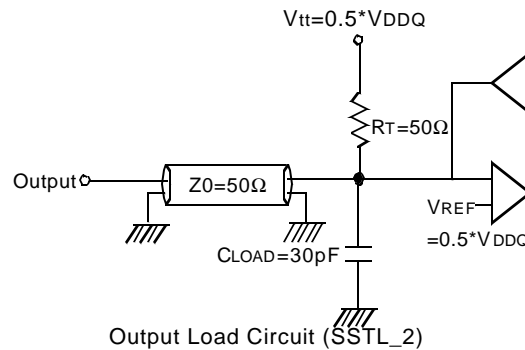
AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V _{IH} (AC)	V _{REF} + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V _{IL} (AC)		V _{REF} - 0.31	V	3
Input Differential Voltage, CK and CK inputs	V _{ID} (AC)	0.7	V _{DDQ} +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V _{IX} (AC)	0.5*V _{DDQ} -0.2	0.5*V _{DDQ} +0.2	V	2

- Note
1. V_{ID} is the magnitude of the difference between the input level on CK and the input on $\overline{\text{CK}}$.
 2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relative to a V_{ref} envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V _{DDQ}	V	
Input signal maximum peak swing	1.5	V	
Input Levels(V _{IH} /V _{IL})	V _{REF} +0.31/V _{REF} -0.31	V	
Input timing measurement reference level	V _{REF}	V	
Output timing measurement reference level	V _{tt}	V	
Output load condition	See Load Circuit		



Input/Output CAPACITANCE (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A ₀ ~ A ₁₁ , BA ₀ ~ BA ₁ , $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C _{IN1}	29	34	pF
Input capacitance(CKE ₀)	C _{IN2}	29	34	pF
Input capacitance($\overline{\text{CS}}$ ₀)	C _{IN3}	26	30	pF
Input capacitance(CLK ₀ , CLK ₁)	C _{IN4}	30	32	pF
Data & DQS input/output capacitance(DQ ₀ ~DQ ₆₃)	C _{OUT}	8	9	pF
Input capacitance(DM ₀ ~DM ₈)	C _{IN5}	8	9	pF

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AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)

Parameter	Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	65		65		70		ns		
Refresh row cycle time	tRFC	75		75		80		ns		
Row active time	tRAS	45	120K	45	120K	48	120K	ns		
RAS to CAS delay	tRCD	20		20		20		ns		
Row precharge time	tRP	20		20		20		ns		
Row active to Row active delay	tRRD	15		15		15		ns		
Write recovery time	tWR	15		15		15		ns		
Last data in to Read command	tWTR	1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	10	12	10	12	ns	5
		CL=2.5	7.5	12	7.5	12			ns	5
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/ $\overline{\text{CK}}$	tDQSK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Output data access time from CK/ $\overline{\text{CK}}$	tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data strobe edge to output data edge	tDQSQ	-	0.5	-	0.5	-	0.6	ns	5	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		ns	2	
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time(fast)	tIS	0.9		0.9		1.1		ns	6	
Address and Control Input hold time(fast)	tIH	0.9		0.9		1.1		ns	6	
Address and Control Input setup time(slow)	tIS	1.0		1.0		1.1		ns	6	
Address and Control Input hold time(slow)	tIH	1.0		1.0		1.1		ns	6	
Data-out high impedance time from CK/ $\overline{\text{CK}}$	tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data-out low impedance time from CK/ $\overline{\text{CK}}$	tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		0.5		V/ns	6	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ns	7	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10	
Output Slew Rate(x16)	tSL(O)	0.7	5	0.7	5	0.7	5	V/ns	10	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5			

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Parameter	Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		0.5		0.6		ns	7,8,9
DQ & DM input pulse width	tDIPW	1.75		1.75		2		ns	
Power down exit time	tPDEX	7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		80		ns	4
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	64Mb, 128Mb	tREFI	15.6		15.6		15.6	us	1
	256Mb		7.8		7.8		7.8	us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

1. Maximum burst refresh of 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DIMMs, tCL and tCH are $\geq 45\%$ of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.

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6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	Δt_{IS} (ps)	Δt_{IH} (ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	Δt_{DS} (ps)	Δt_{DH} (ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level (mV)	Δt_{DS} (ps)	Δt_{DH} (ps)
± 280	+50	+50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below $V_{REF} \pm 310mV$ for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate (ns/V)	Δt_{DS} (ps)	Δt_{DH} (ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as $1/SlewRate1-1/SlewRate2$. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Note>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	$\Delta t_{IH}/t_{IS}$ (ps)	$\Delta t_{DSS}/t_{DSH}$ (ps)	$\Delta t_{AC}/t_{DQSCK}$ (ps)	$\Delta t_{LZ}(\min)$ (ps)	$\Delta t_{HZ}(\max)$ (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

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Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0,1	A10/AP	A12, A11 A9 ~ A0	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L							3	
		Exit	L	H	L	H	H	H	X		3	
	H		X	X							X	3
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable									H		4, 6
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry		H	L	H	X	X	X	X			
	Exit				L	H	X	X			X	X
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X			
	Exit				L	H	X	X			X	X
	Entry		L	H	H	X	X	X				
	Exit				L	H	H	H			H	
DM		H	X					X			8	
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9	
				L	H	H	H			9		

Note : 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

7. Burst stop command is valid at every burst length.

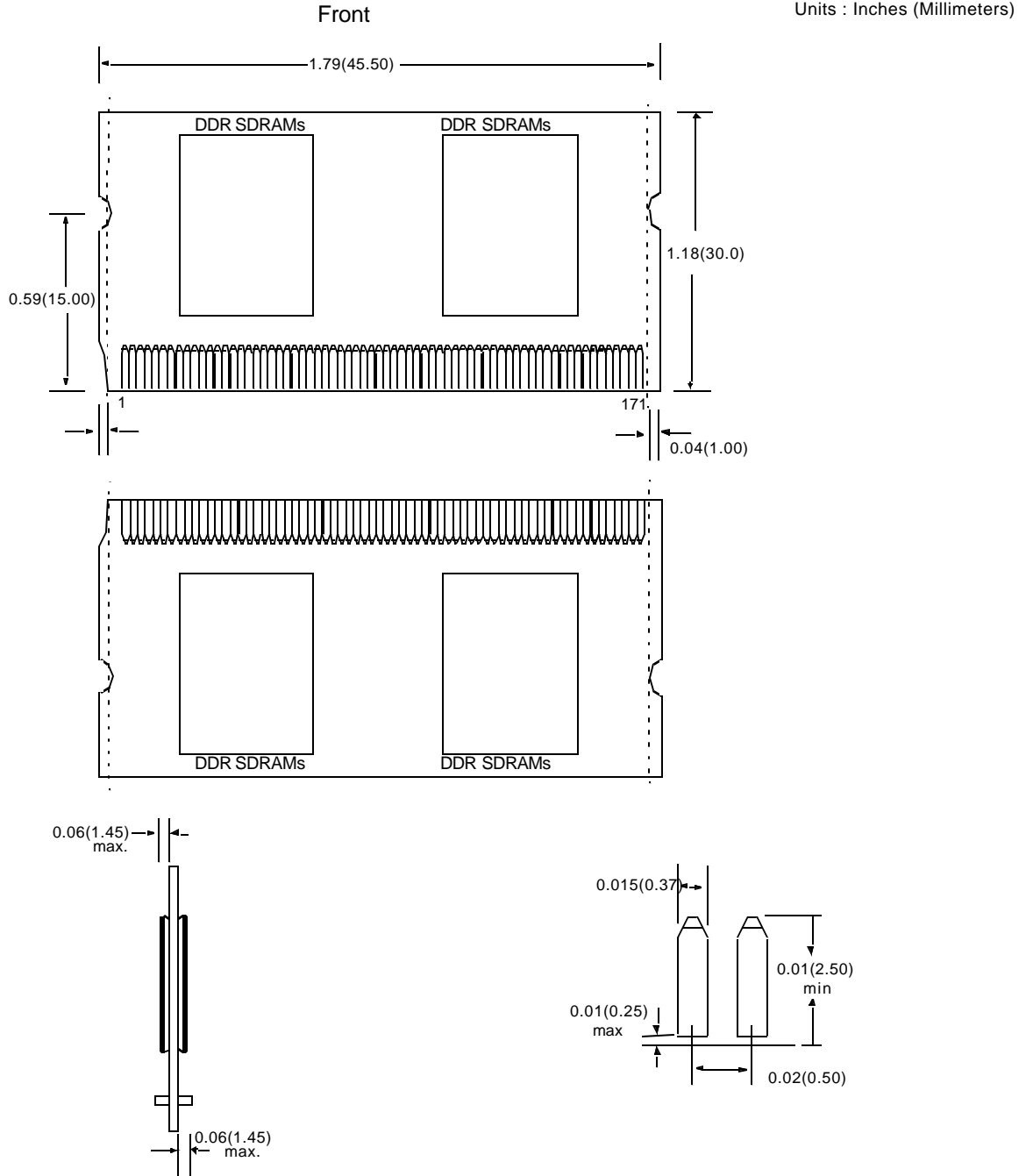
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

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PACKAGE DIMENSIONS



Tolerances : ± 0.01 (.25) unless otherwise specified

The used device is 16Mx16 SDRAM, TSOP
SDRAM Part No. : K4H561638B-TC/L