

**Revision History**

**Revision 0 (Oct. 2000)**

-PC133 First Published.

**M464S1654BT2 SDRAM SODIMM**

16Mx64 SDRAM SODIMM based on 16Mx16,4Banks,8K Refresh 3.3V Synchronous DRAMs with SPD

**GENERAL DESCRIPTION**

The Samsung M464S1654BT2 is a 16M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M464S1654BT2 consists of four CMOS 16M x 16 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M464S1654BT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

**FEATURE**

- Performance range

Part No.	Max Freq. (Speed)
M464S1654BT2-L75 /C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs  
Latency (Access from column address)  
Burst length (1, 2, 4, 8 & Full page)  
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,000mil)** , double sided component

**PIN CONFIGURATIONS (Front side/back side)**

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	<b>Voltage Key</b>				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37	109	A9	110	BA1				
17	DQ6	18	DQ38	61	CLK0	62	CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	VDD	64	VDD	113	VDD	114	VDD
21	Vss	22	Vss	65	RAS	66	CAS	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	WE	68	*CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	CS0	70	A12	119	Vss	120	Vss
27	VDD	28	VDD	71	*CS1	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	*CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	Vss	76	Vss	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	79	NC	80	NC	129	VDD	130	VDD
37	DQ8	38	DQ40	81	VDD	82	VDD	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	VDD	46	VDD	89	DQ19	90	DQ51	139	Vss	140	Vss
47	DQ12	48	DQ44	91	Vss	92	Vss	141	**SDA	142	**SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	VDD	144	VDD

**PIN NAMES**

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address storbe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

\* These pins are not used in this module.  
\*\* These pins should be NC in the system which does not support SPD.

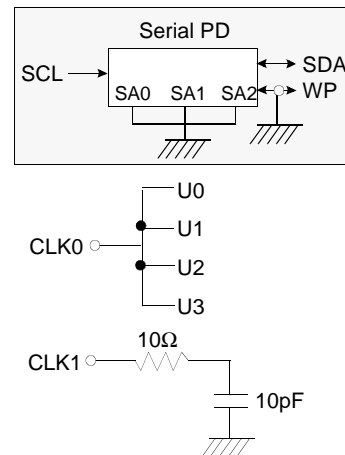
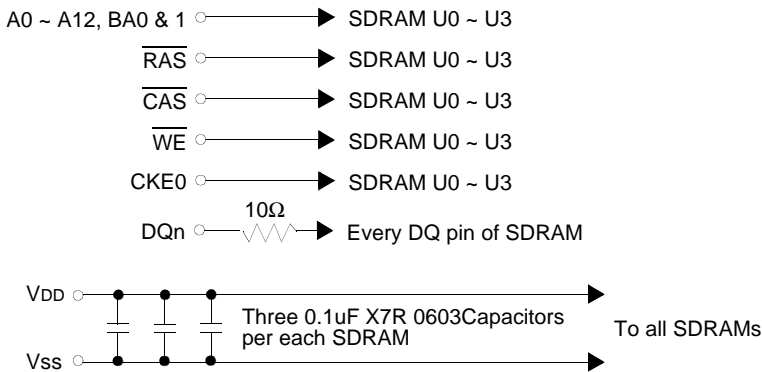
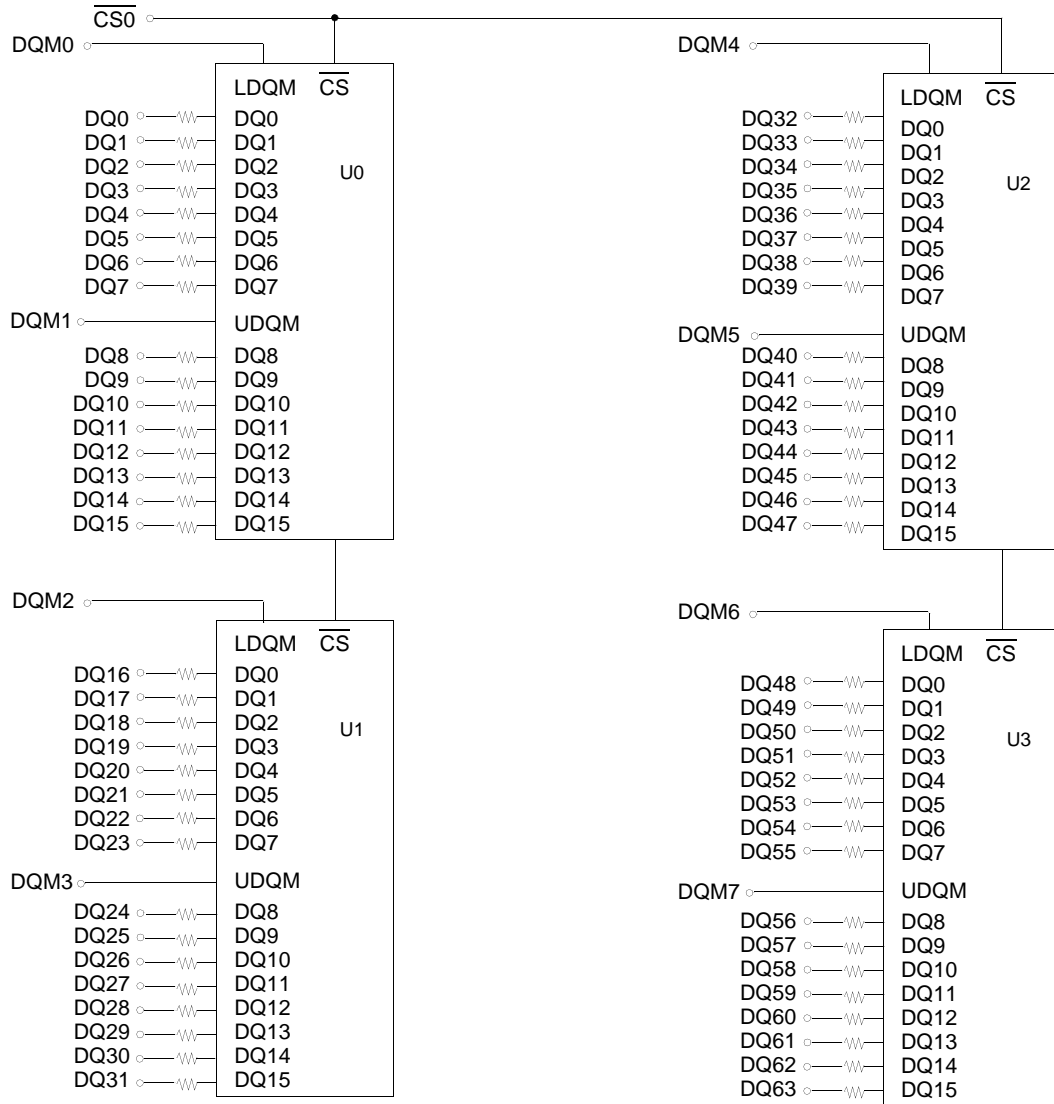
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## PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	4	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

Recommended operating conditions (Voltage referenced to Vss = 0V, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	
Input high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current	I <sub>LI</sub>	-10	-	10	uA	3

**Notes :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

**CAPACITANCE** (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A <sub>0</sub> ~ A <sub>11</sub> , BA <sub>0</sub> ~ BA <sub>1</sub> )	C <sub>IN1</sub>	15	25	pF
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ )	C <sub>IN2</sub>	15	25	pF
Input capacitance (CKE <sub>0</sub> )	C <sub>IN3</sub>	15	25	pF
Input capacitance (CLK <sub>0</sub> )	C <sub>IN4</sub>	15	21	pF
Input capacitance ( $\overline{\text{CS0}}$ )	C <sub>IN5</sub>	15	25	pF
Input capacitance (DQM <sub>0</sub> ~ DQM <sub>7</sub> )	C <sub>IN6</sub>	10	12	pF
Data input/output capacitance (DQ <sub>0</sub> ~ DQ <sub>63</sub> )	C <sub>OUT</sub>	10	12	pF

## DC CHARACTERISTICS

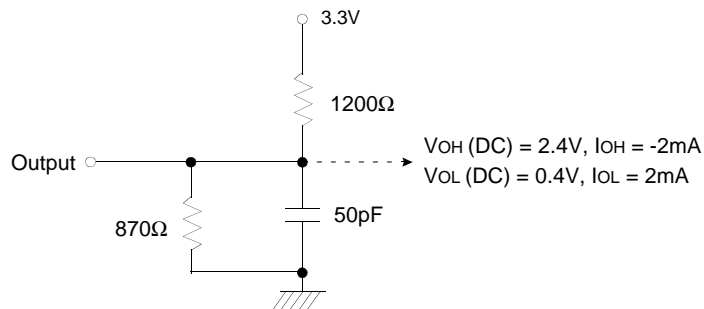
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note	
			-75			
Operating current (One bank active)	ICC1	Burst length = 1 trc ≥ trc(min) IO = 0 mA	600	mA	1	
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tcc = 10ns	8	mA		
	ICC2PS	CKE & CLK ≤ VIL(max), tcc = ∞	8			
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$ , tcc = 10ns Input signals are changed one time during 20ns	64	mA		
	ICC2NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	56			
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tcc = 10ns	24	mA		
	ICC3PS	CKE & CLK ≤ VIL(max), tcc = ∞	24			
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$ , tcc = 10ns Input signals are changed one time during 20ns	140	mA		
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tcc = ∞ Input signals are stable	120	mA		
Operating current (Burst mode)	ICC4	IO = 0 mA Page burst 4Banks activated tCCD = 2CLKs	720	mA	1	
Refresh current	ICC5	trc ≥ trc(min)	880	mA	2	
Self refresh current	ICC6	CKE ≤ 0.2V	C	12	mA	
			L	8	mA	

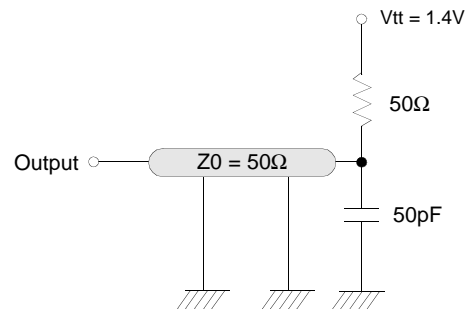
- Notes :**
1. Measured with outputs open.
  2. Refresh period is 64ms.
  3. Unless otherwise noted, input swing level is CMOS(VIH/VIL=VDDQ/VSSQ)

**AC OPERATING TEST CONDITIONS** ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^\circ C$ )

Parameter	Value	Unit
AC input levels ( $V_{ih}/V_{il}$ )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	$t_{RRD}(\min)$	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	$t_{RCD}(\min)$	20	ns	1
Row precharge time	$t_{RP}(\min)$	20	ns	1
Row active time	$t_{RAS}(\min)$	45	ns	1
	$t_{RAS}(\max)$	100	us	
Row cycle time	$t_{RC}(\min)$	65	ns	1
Last data in to row precharge	$t_{RDL}(\min)$	2	CLK	2
Last data in to Active delay	$t_{DAL}(\min)$	2 CLK + 20 ns	-	
Last data in to new col. address delay	$t_{CDL}(\min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(\min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(\min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	-		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.

**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)  
**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
	CAS latency=2		-			
CLK to valid output delay	CAS latency=3	tSAC		5.4	ns	1,2
	CAS latency=2			-		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		-			
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	
	CAS latency=2			-		

- Notes :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns,  $(tr/2-0.5)$ ns should be added to the parameter.
  - Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
 If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered,  
 i.e.,  $[(tr + tf)/2-1]$ ns should be added to the parameter.



SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A11,A12 A9 ~ A0	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self refresh	L	H	L	H	H	H	X	X			3	
				H	X	X	X					3	
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A0 ~ A8)		4
	Auto precharge enable									H			4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A0 ~ A8)		4
	Auto precharge enable									H			4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X				
				L	V	V	V						
Precharge power down mode	Entry	H	L	H	X	X	X	X	X				
				L	H	H	H						
	Exit	L	H	H	X	X	X	X	X				
				L	V	V	V						
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

Notes : 1. OP Code : Operand code

A0 ~ A12 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

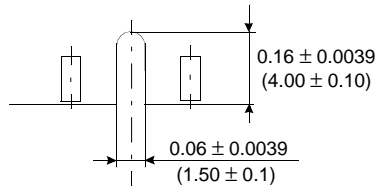
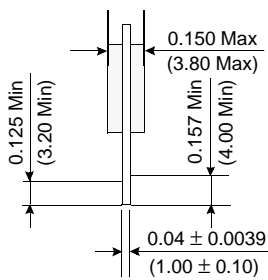
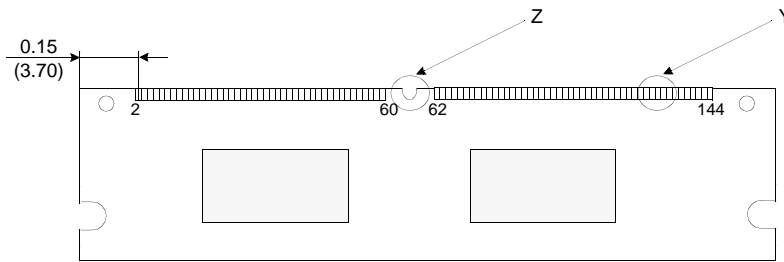
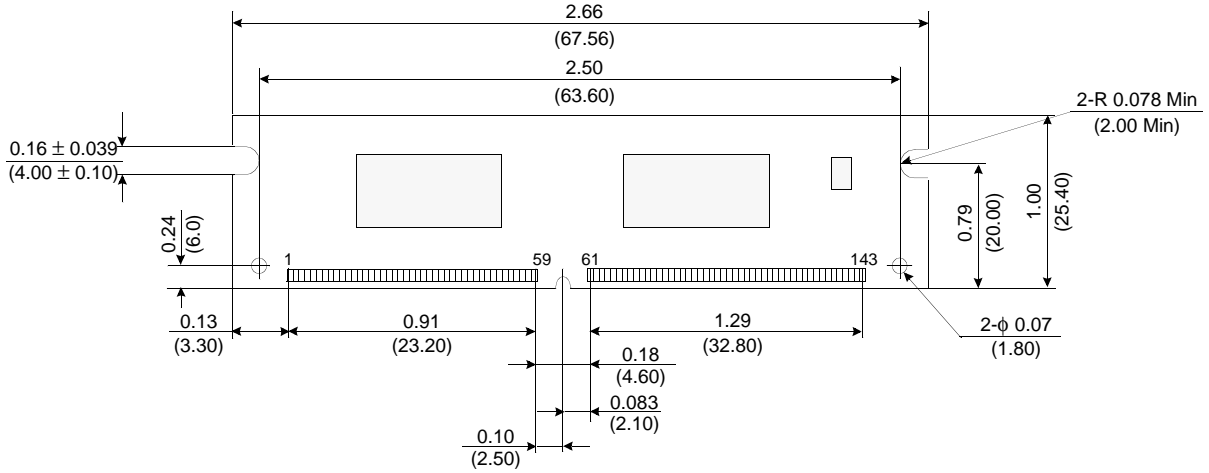
New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

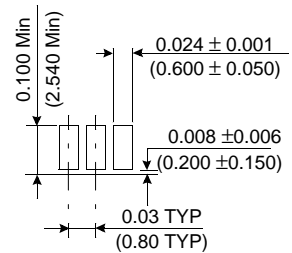
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ± 0.006(.15) unless otherwise specified

The used device is 16Mx16 SDRAM, TSOP  
SDRAM Part No. : K4S561632B

# M464S1654BT2

# PC133 SODIMM

## M464S1654BT2-L75/C75(Intel SPD 1.2B ver. based)

- Organization : 16MX64
- Composition : 16MX16 \*4
- Used component part # : K4S561632B-TL75/TC75
- # of rows in module : 1 row
- # of banks in component : 4 banks
- Feature : 1,000 mil height & double sided
- Refresh : 8K/64ms
- Contents :

Byte #	Function described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	13	0Dh	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTTL	01h	
9	SDRAM cycle time from clock @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	Non parity	00h	
12	Refresh rate & type	7.8us, support self refresh self	82h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered/Non-Registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module Row density	1 Row of 128MB	20h	
32	Command and Address signal input setup time	1.5ns	15h	
33	Command and Address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

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## SERIAL PRESENCE DETECT INFORMATION

Byte #	Function described	Function Supported		Hex value		Note
		-75		-75		
35	Data signal input hold time	0.8ns		08h		
36-61	Superset information (maybe used in future)	-		00h		
62	SPD data revision code	Intel 1.2B		12h		
63	Checksum for bytes 0 ~ 62	-		B7h		
64	Manufacturer JEDEC ID code	Samsung		CEh		
65-71	..... Manufacturer JEDEC ID code	Samsung		00h		
72	Manufacturing location	Onyang Korea		01h		
73	Manufacturer part # (Memory module)	M		4Dh		
74	Manufacturer part # (DIMM Configuration)	4		34h		
75	Manufacturer part # (Data bits)	Blank		20h		
76	..... Manufacturer part # (Data bits)	6		36h		
77	..... Manufacturer part # (Data bits)	4		34h		
78	Manufacturer part # (Mode & operating voltage)	S		53h		
79	Manufacturer part # (Module depth)	1		31h		
80	..... Manufacturer part # (Module depth)	6		36h		
81	Manufacturer part # (Refresh, #of banks in Comp. & Inter-	5		35h		
82	Manufacturer part # (Composition component)	4		34h		
83	Manufacturer part # (Component revision)	B		42h		
84	Manufacturer part # (Package type)	T		54h		
85	Manufacturer part # (PCB revision & type)	2		32h		
86	Manufacturer part # (Hyphen)	" - "		2Dh		
87	Manufacturer part # (Power)	L	C	4Ch	43h	
88	Manufacturer part # (Minimum cycle time)	7		37h		
89	Manufacturer part # (Minimum cycle time)	5		35h		
90	Manufacturer part # (TBD)	Blank		20h		
91	Manufacturer revision code (For PCB)	2		32h		
92	..... Manufacturer revision code (For component)	B-die (3rd Gen.)		42h		
93	Manufacturing date (Week)	-		-		3
94	Manufacturing date (Year)	-		-		3
95-98	Assembly serial #	-		-		4
99-125	Manufacturer specific data (may be used in future)	Undefined		-		5
126	Reserved	-		64h		6
127	Reserved	Detailed PC100 Information		8Dh		6
128+	Unused storage locations	Undefined		-		5

- Note :**
1. The bank select address is excluded in counting the total # of addresses.
  2. This value is based on the component specification.
  3. These bytes are programmed by code of Date Week & Date Year with BCD format.
  4. These bytes are programmed by Samsung's own Assembly Serial # system. All modules may have different unique serial #.
  5. These bytes are Undefined and can be used for Samsung's own purpose.
  6. These values apply to PC100 applications only, per Intel PC66/PC100 SPD standards.