# SDRAM Unbuffered SODIMM

144pin Unbuffered SODIMM based on 128Mb K-die
64-bit Non ECC

## 54 TSOP-II with Lead-Free and Halogen-Free

**(RoHS compliant)**

## Table of Contents

## Revision History

| Revision | Month | Year | History |
|---|---|---|---|
| 1.0 | February | 2007 | - Revision 1.0 spec release. |
| 1.1 | September | 2007 | - Changed the component feature |
| 1.2 | August | 2008 | - Corrected typo on IDD current table |
| 1.21 | February | 2009 | - Corrected typo on ordering information |

## 144Pin Unbuffered SODIMM based on 128Mb K-die (x16)

## 1.0 Ordering Information

| Part Number | Density | Organization | Component Composition | Component Package | Height |
|---|---|---|---|---|---|
| M464S1724KLS-C(L)7A | 128MB | 16M x 64 | 8Mx16( K4S281632K) * 8EA | 54-TSOPII | 1,250mil |

Note:
1. “L” of Part number(11th digit) stands for Lead-Free, Halogen-Free, and RoHS compliant products.

## 2.0 Operating Frequencies

| | 7A | |
|---|---|---|
| | Speed @CL3 | Speed @CL2 |
| Maximum Clock Frequency | 133MHz(7.5ns) | 100MHz(10ns) |
| CL-tRCD-tRP | 3-3-3 | 2-2-2 |

## 3.0 Feature

• Burst mode operation
• Auto & self refresh capability (4096 Cycles/64ms)
• LVTTL compatible inputs and outputs
• Single 3.3V ± 0.3V power supply
• MRS cycle with address key programs Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
• All inputs are sampled at the positive going edge of the system clock
• Serial presence detect with EEPROM
• **54 TSOPII Lead-Free and Halogen-Free Package**
• All of products are Lead-Free and Halogen-Free, and RoHS compliant

## 4.0 Pin Configuration (Front side/back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 2 | $V_{SS}$ | 51 | DQ14 | 52 | DQ46 | 95 | DQ21 | 96 | DQ53 |
| 3 | DQ0 | 4 | DQ32 | 53 | DQ15 | 54 | DQ47 | 97 | DQ22 | 98 | DQ54 |
| 5 | DQ1 | 6 | DQ33 | 55 | $V_{SS}$ | 56 | $V_{SS}$ | 99 | DQ23 | 100 | DQ55 |
| 7 | DQ2 | 8 | DQ34 | 57 | NC | 58 | NC | 101 | $V_{DD}$ | 102 | $V_{DD}$ |
| 9 | DQ3 | 10 | DQ35 | 59 | NC | 60 | NC | 103 | A6 | 104 | A7 |
| 11 | $V_{DD}$ | 12 | $V_{DD}$ | Voltage Key | | | | 105 | A8 | 106 | BA0 |
| 13 | DQ4 | 14 | DQ36 | | | | | 107 | $V_{SS}$ | 108 | $V_{SS}$ |
| 15 | DQ5 | 16 | DQ37 | | | | | 109 | A9 | 110 | BA1 |
| 17 | DQ6 | 18 | DQ38 | 61 | **CLK0 | 62 | **CKE0 | 111 | A10/AP | 112 | A11 |
| 19 | DQ7 | 20 | DQ39 | 63 | $V_{DD}$ | 64 | $V_{DD}$ | 113 | $V_{DD}$ | 114 | $V_{DD}$ |
| 21 | $V_{SS}$ | 22 | $V_{SS}$ | 65 | $\overline{RAS}$ | 66 | $\overline{CAS}$ | 115 | DQM2 | 116 | DQM6 |
| 23 | DQM0 | 24 | DQM4 | 67 | $\overline{WE}$ | 68 | **CKE1 | 117 | DQM3 | 118 | DQM7 |
| 25 | DQM1 | 26 | DQM5 | 69 | **$\overline{CS0}$ | 70 | *A12 | 119 | $V_{SS}$ | 120 | $V_{SS}$ |
| 27 | $V_{DD}$ | 28 | $V_{DD}$ | 71 | **$\overline{CS1}$ | 72 | *A13 | 121 | DQ24 | 122 | DQ56 |
| 29 | A0 | 30 | A3 | 73 | DU | 74 | **CLK1 | 123 | DQ25 | 124 | DQ57 |
| 31 | A1 | 32 | A4 | 75 | $V_{SS}$ | 76 | $V_{SS}$ | 125 | DQ26 | 126 | DQ58 |
| 33 | A2 | 34 | A5 | 77 | NC | 78 | NC | 127 | DQ27 | 128 | DQ59 |
| 35 | $V_{SS}$ | 36 | $V_{SS}$ | 79 | NC | 80 | NC | 129 | $V_{DD}$ | 130 | $V_{DD}$ |
| 37 | DQ8 | 38 | DQ40 | 81 | $V_{DD}$ | 82 | $V_{DD}$ | 131 | DQ28 | 132 | DQ60 |
| 39 | DQ9 | 40 | DQ41 | 83 | DQ16 | 84 | DQ48 | 133 | DQ29 | 134 | DQ61 |
| 41 | DQ10 | 42 | DQ42 | 85 | DQ17 | 86 | DQ49 | 135 | DQ30 | 136 | DQ62 |
| 43 | DQ11 | 44 | DQ43 | 87 | DQ18 | 88 | DQ50 | 137 | DQ31 | 138 | DQ63 |
| 45 | $V_{DD}$ | 46 | $V_{DD}$ | 89 | DQ19 | 90 | DQ51 | 139 | $V_{SS}$ | 140 | $V_{SS}$ |
| 47 | DQ12 | 48 | DQ44 | 91 | $V_{SS}$ | 92 | $V_{SS}$ | 141 | SDA | 142 | SCL |
| 49 | DQ13 | 50 | DQ45 | 93 | DQ20 | 94 | DQ52 | 143 | $V_{DD}$ | 144 | $V_{DD}$ |

**Note :**

1.* These pins are not used in this module.

2.Pins 141,142 should be NC in the system which does not support SPD.

3.** About these pins, Refer to the Block Diagram of each.

## 5.0 Pin Description

| Pin Name | Function | Pin Name | Function |
|---|---|---|---|
| A0 ~ A11 | Address input (Multiplexed) | $\overline{WE}$ | Write enable |
| BA0 ~ BA1 | Select bank | DQM0 ~ 7 | DQM |
| DQ0 ~ DQ63 | Data input/output | $V_{DD}$ | Power supply (3.3V) |
| CLK0 ~ CLK1 | Clock input | $V_{SS}$ | Ground |
| CKE0 ~ CKE1 | Clock enable input | SDA | Serial data I/O |
| $\overline{CS0}$ ~ $\overline{CS1}$ | Chip select input | SCL | Serial clock |
| $\overline{RAS}$ | Row address strobe | DU | Don't use |
| $\overline{CAS}$ | Column address strobe | NC | No connection |

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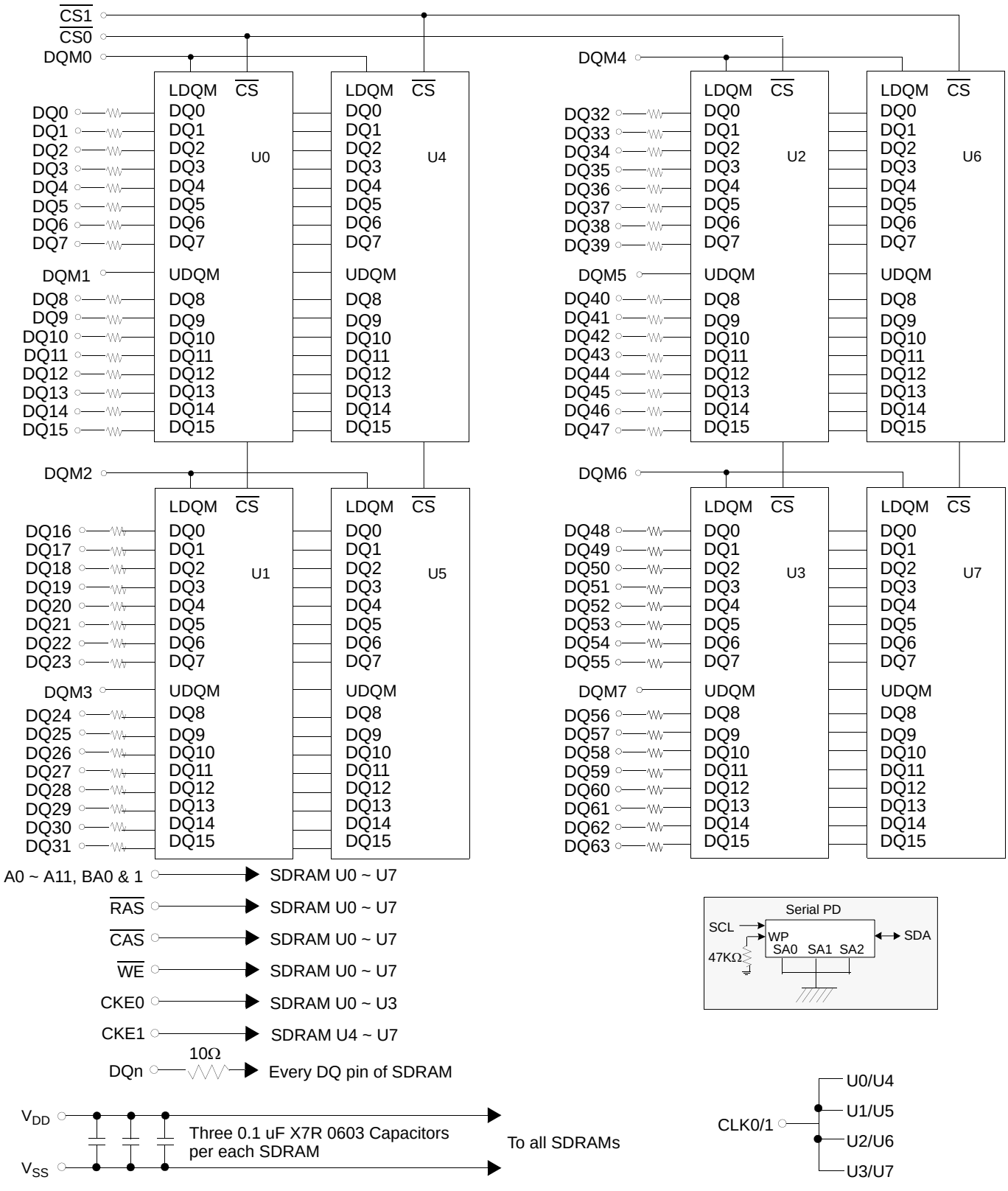
## 6.0 Pin Configuration Description

| Pin | Name | Input Function |
|---|---|---|
| CLK | *System clock* | Active on the positive going edge to sample all inputs. |
| $\overline{CS}$ | *Chip select* | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM |
| CKE | *Clock enable* | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tSS prior to valid command. |
| A0 ~ A11 | *Address* | Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11 Column address : (x16 : CA0 ~ CA8) |
| BA0 ~ BA1 | *Bank select address* | Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time. |
| $\overline{RAS}$ | *Row address strobe* | Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge. |
| $\overline{CAS}$ | *Column address strobe* | Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access. |
| $\overline{WE}$ | *Write enable* | Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active. |
| DQM0 ~ 7 | *Data input/output mask* | Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking) |
| $DQ_{0 \sim 63}$ | *Data input/output* | Data inputs/outputs are multiplexed on the same pins. |
| $V_{DD}/V_{SS}$ | *Power supply/ground* | Power and ground for the input buffers and the core logic. |

## 7.0 Functional Block Diagram

### 7.1 128MB, 16Mx64 Module (M464S1724KLS)

(Populated as 2 bank of x16 SDRAM Module)




Note : Use a zero ohm jumper to isolate A12 from the SDRAM pins in non-256Mbit designs.

## 8.0 Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | -1.0 ~ 4.6 | V |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$, $V_{DDQ}$ | -1.0 ~ 4.6 | V |
| Storage temperature | $T_{STG}$ | -55 ~ +150 | °C |
| Power dissipation | $P_D$ | 1.0 * # of component | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

Note :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## 9.0 DC Operating Conditions And Characteristics

Recommended operating conditions (Voltage referenced to $V_{SS}$ = 0V, $T_A$ = 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V | |
| Input high voltage | $V_{IH}$ | 2.0 | 3.0 | $V_{DDQ}$+0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | -0.3 | 0 | 0.8 | V | 2 |
| Output high voltage | $V_{OH}$ | 2.4 | - | - | V | $I_{OH}$ = -2mA |
| Output low voltage | $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 2mA |
| Input leakage current | $I_{LI}$ | -10 | - | 10 | uA | 3 |

Note :
1. $V_{IH}$ (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. $V_{IL}$ (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ $V_{IN}$ ≤ $V_{DDQ}$. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## 10.0 Capacitance(Max.)

($V_{DD}$ = 3.3V, $T_A$ = 23°C, f = 1MHz, $V_{REF}$ = 1.4V ± 200 mV)

| Parameter | Symbol | M464S1724KLS | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Input capacitance ($A_0$ ~ $A_{11}$, BA0 ~ BA1) | $C_{IN1}$ | 25 | 45 | pF |
| Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | $C_{IN2}$ | 25 | 45 | pF |
| Input capacitance (CKE0 ~ CKE1) | $C_{IN3}$ | 15 | 25 | pF |
| Input capacitance (CLK0 ~ CLK1) | $C_{IN4}$ | 15 | 21 | pF |
| Input capacitance ($\overline{CS0}$ ~ $\overline{CS1}$) | $C_{IN5}$ | 15 | 25 | pF |
| Input capacitance (DQM0 ~ DQM7) | $C_{IN6}$ | 10 | 12 | pF |
| Data input/output capacitance (DQ0 ~ DQ63) | $C_{OUT}$ | 10 | 12 | pF |

# 11.0 DC CHARACTERISTICS

## 11.1 M464S1724KUS (16M x 64, 128MB Module)

(Recommended operating condition unless otherwise noted, $T_A$ = 0 to 70°C)

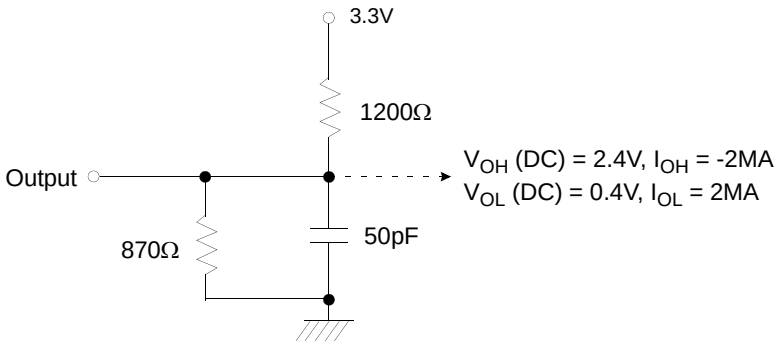
| Parameter | Symbol | Test Condition | | Version | Unit | Note |
|---|---|---|---|---|---|---|
| | | | | 7A | | |
| Operating current (One bank active) | $I_{CC1}$ | Burst length = 1, tRC ≥ tRC(min), IO = 0 mA | | 520 | mA | 1 |
| Precharge standby current in power-down mode | $I_{CC2P}$ | CKE ≤ $V_{IL}$(max), tCC = 10ns | | 16 | mA | |
| | $I_{CC2PS}$ | CKE & CLK ≤ $V_{IL}$(max), tCC =∞ | | 16 | | |
| Precharge standby current in non power-down mode | $I_{CC2N}$ | CKE ≥ $V_{IH}$(min), $\overline{CS}$ ≥ $V_{IH}$(min), tCC = 10ns<br>Input signals are changed one time during 20ns | | 160 | mA | |
| | $I_{CC2NS}$ | CKE ≥ $V_{IH}$(min), CLK ≤ $V_{IL}$(max), tCC =∞<br>Input signals are stable | | 80 | | |
| Active standby current in power-down mode | $I_{CC3P}$ | CKE ≤ $V_{IL}$(max), tCC = 10ns | | 40 | mA | |
| | $I_{CC3PS}$ | CKE & CLK ≤ $V_{IL}$(max), tCC =∞ | | 40 | | |
| Active standby current in non power-down mode (One bank active) | $I_{CC3N}$ | CKE ≥ $V_{IH}$(min), $\overline{CS}$ ≥ $V_{IH}$(min), tCC = 10ns<br>Input signals are changed one time during 20ns | | 240 | mA | |
| | $I_{CC3NS}$ | CKE ≥ $V_{IH}$(min), CLK ≤ $V_{IL}$(max), tCC =∞<br>Input signals are stable | | 200 | mA | |
| Operating current (Burst mode) | $I_{CC4}$ | IO = 0 mA,<br>Page burst 4Banks activated tCCD = 2CLKs | | 680 | mA | 1 |
| Refresh current | $I_{CC5}$ | tRC ≥ tRC(min) | | 920 | mA | 2 |
| Self refresh current | $I_{CC6}$ | CKE ≤ 0.2V | C | 16 | mA | |
| | | | L | 6.4 | mA | |

**Notes :** 1. Measured with outputs open.
2. Refresh period is 64ms.

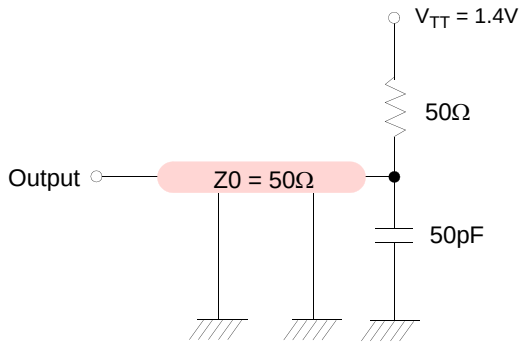
## 12.0 AC Operating Test Conditions

($V_{DD}$ = 3.3V ± 0.3V, $T_A$ = 0 to 70°C)

| Parameter | Value | Unit |
|---|---|---|
| AC input levels ($V_{IH}$/$V_{IL}$) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | tr/tf = 1/1 | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |




(Fig. 1) DC output load circuit




(Fig. 2) AC output load circuit

## 13.0 OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter | | Symbol | Version | Unit | Note |
|---|---|---|---|---|---|
| | | | 7A | | |
| Row active to row active delay | | tRRD(min) | 15 | ns | 1 |
| $\overline{RAS}$ to $\overline{CAS}$ delay | | tRCD(min) | 20 | ns | 1 |
| Row precharge time | | tRP(min) | 20 | ns | 1 |
| Row active time | | tRAS(min) | 45 | ns | 1 |
| | | tRAS(max) | 100 | us | |
| Row cycle time | | tRC(min) | 65 | ns | 1 |
| Last data in to row precharge | | tRDL(min) | 2 | CLK | 2 |
| Last data in to Active delay | | tDAL(min) | 2 CLK + tRP | - | |
| Last data in to new col. address delay | | tCDL(min) | 1 | CLK | 2 |
| Last data in to burst stop | | tBDL(min) | 1 | CLK | 2 |
| Col. address to col. address delay | | tCCD(min) | 1 | CLK | 3 |
| Number of valid output data | CAS latency=3 | | 2 | ea | 4 |
| | CAS latency=2 | | 1 | | |

Note :

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.
6. tRC =tRFC, tRDL = tWR.

## 14.0 AC CHARACTERISTICS

### REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

(AC operating conditions unless otherwise noted)

| Parameter | | Symbol | - 7A | | Unit | Note |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| CLK cycle time | CAS latency=3 | tCC | 7.5 | 1000 | ns | 1 |
| | CAS latency=2 | | 10 | | | |
| CLK to valid output delay | CAS latency=3 | tSAC | | 5.4 | ns | 1,2 |
| | CAS latency=2 | | | 6 | | |
| Output data hold time | CAS latency=3 | tOH | 3 | | ns | 2 |
| | CAS latency=2 | | 3 | | | |
| CLK high pulse width | | tCH | 2.5 | | ns | 3 |
| CLK low pulse width | | tCL | 2.5 | | ns | 3 |
| Input setup time | | tSS | 1.5 | | ns | 3,4 |
| Input hold time | | tSH | 0.8 | | ns | 3,4 |
| CLK to output in Low-Z | | tSLZ | 1 | | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | tSHZ | | 5.4 | ns | |
| | CAS latency=2 | | | 6 | | |

Note :

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.
4. tSS applies for address setup time, clock enable setup time, commend setup time and data setup time
   tSH applies for address holde time, clock enable hold time, commend hold time and data hold time

## 15.0 SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

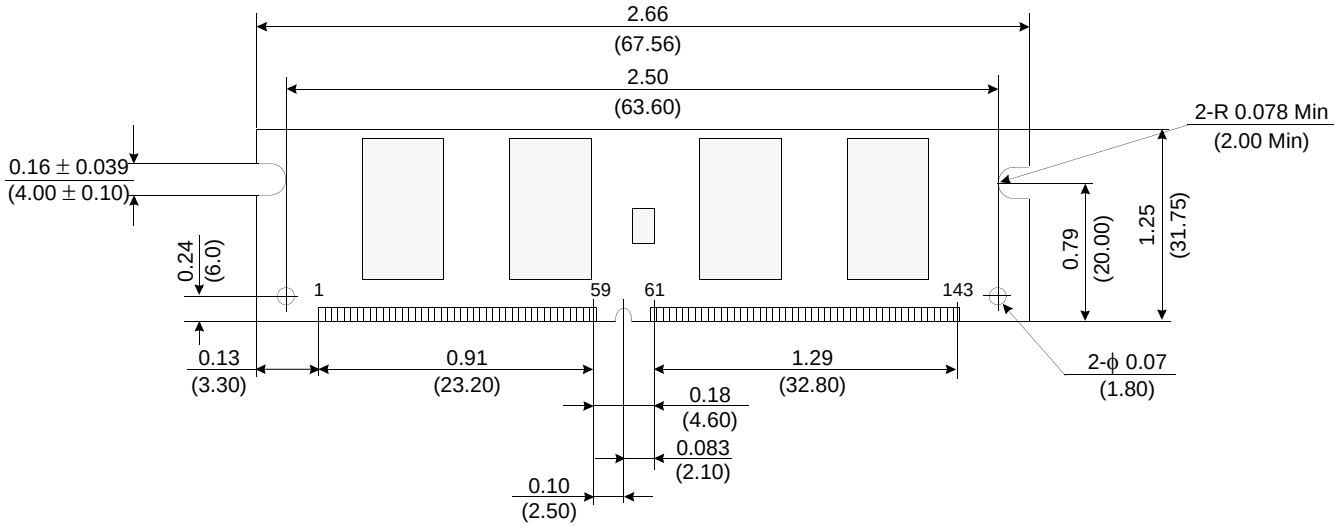
| Command | | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | $BA_{0,1}$ | $A_{10}$/AP | $A_0$ ~ $A_9$, $A_{11}$ | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Mode register set | | H | X | L | L | L | L | X | OP code | | | 1,2 |
| Refresh | Auto refresh | | H | H | L | L | L | H | X | X | | | 3 |
| | Self refresh | Entry | | L | | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank active & row addr. | | | H | X | L | L | H | H | X | V | Row address | | |
| Read & column address | Auto precharge disable | | H | X | L | H | L | H | X | V | L | Column address | 4 |
| | Auto precharge enable | | | | | | | | | | H | | 4,5 |
| Write & column address | Auto precharge disable | | H | X | L | H | L | L | X | V | L | Column address | 4 |
| | Auto precharge enable | | | | | | | | | | H | | 4,5 |
| Burst stop | | | H | X | L | H | H | L | X | X | | | 6 |
| Precharge | Bank selection | | H | X | L | L | H | L | X | V | L | X | |
| | All banks | | | | | | | | | X | H | | |
| Clock suspend or active power down | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | V | V | V | | | | | |
| | | Exit | L | H | X | X | X | X | X | | | | |
| Precharge power down mode | | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |
| | | Exit | L | H | H | X | X | X | X | | | | |
| | | | | | L | V | V | V | | | | | |
| DQM | | | H | X | | | | | V | X | | | 7 |
| No operation command | | | H | X | H | X | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | | |

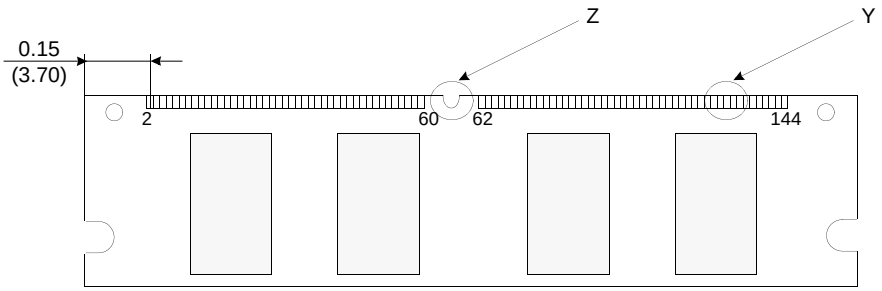
Note :
1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

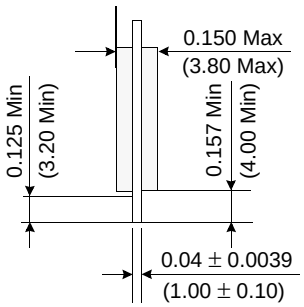
# 16.0 PHYSICAL DIMENSIONS

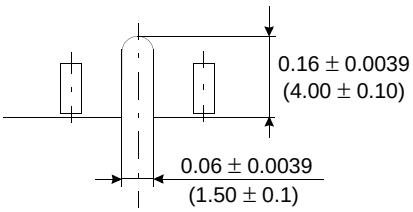
## 16.1 16Mx64 (M464S1724KLS)

Units : Inches (Millimeters)

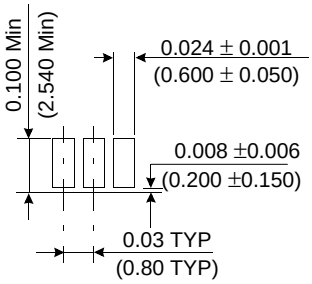



**Detail Z**




**Detail Y**

Tolerances : ±.006(.15) unless otherwise specified

The used device is 8Mx16 SDRAM, TSOPII
SDRAM Part No. : K4S281632K