

**M466S0823DT2 SDRAM SODIMM**

8Mx64 SDRAM SODIMM based on 8Mx8, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

**GENERAL DESCRIPTION**

The Samsung M466S0823DT2 is a 8M bit x 64 Synchronous Dynamic RAM high density memory module. The Samsung M466S0823DT2 consists of eight CMOS 8M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil package and a 2K EEPROM in 8-pin TSSOP package on a 144-pin glass-epoxy substrate. Two 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M466S0823DT2 is a Small Outline Dual In-line Memory Module and is intended for mounting into 144-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

**FEATURE**

- Performance range

Part No.	Max Freq. (Speed)
M466S0823DT2-L10/C10	66MHz (@ CL=2 & CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs  
Latency (Access from column address)  
Burst length (1, 2, 4, 8 & Full page)  
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,150mil)** , double sided component

**PIN CONFIGURATIONS (Front side/back side)**

1	Vss	2	Vss	51	DQ14	52	DQ46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQ15	54	DQ47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	Vss	56	Vss	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	VDD	102	VDD
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	VDD	12	VDD	<b>Voltage Key</b>				105	A8	106	BA0
13	DQ4	14	DQ36					107	Vss	108	Vss
15	DQ5	16	DQ37	61	CLK0	62	CKE0	109	A9	110	BA1
17	DQ6	18	DQ38	63	VDD	64	VDD	111	A10/AP	112	A11
19	DQ7	20	DQ39	65	RAS	66	CAS	113	VDD	114	VDD
21	Vss	22	Vss	67	WE	68	*CKE1	115	DQM2	116	DQM6
23	DQM0	24	DQM4	69	CS0	70	*A12	117	DQM3	118	DQM7
25	DQM1	26	DQM5	71	*CS1	72	*A13	119	Vss	120	Vss
27	VDD	28	VDD	73	DU	74	CLK1	121	DQ24	122	DQ56
29	A0	30	A3	75	Vss	76	Vss	123	DQ25	124	DQ57
31	A1	32	A4	77	NC	78	NC	125	DQ26	126	DQ58
33	A2	34	A5	79	NC	80	NC	127	DQ27	128	DQ59
35	Vss	36	Vss	81	VDD	82	VDD	129	VDD	130	VDD
37	DQ8	38	DQ40	83	DQ16	84	DQ48	131	DQ28	132	DQ60
39	DQ9	40	DQ41	85	DQ17	86	DQ49	133	DQ29	134	DQ61
41	DQ10	42	DQ42	87	DQ18	88	DQ50	135	DQ30	136	DQ62
43	DQ11	44	DQ43	89	DQ19	90	DQ51	137	DQ31	138	DQ63
45	VDD	46	VDD	91	Vss	92	Vss	139	Vss	140	Vss
47	DQ12	48	DQ44	93	DQ20	94	DQ52	141	**SDA	142	**SCL
49	DQ13	50	DQ45					143	VDD	144	VDD

**PIN NAMES**

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CLK0 ~ CLK1	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
SDA	Serial data I/O
SCL	Serial clock
DU	Don't use
NC	No connection

\* These pins are not used in this module.  
\*\* These pins should be NC in the system which does not support SPD.

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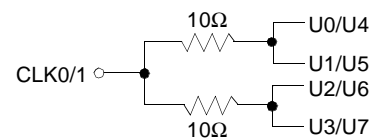
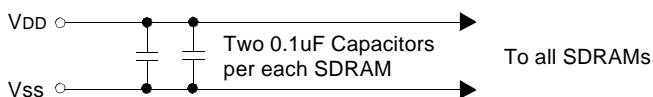
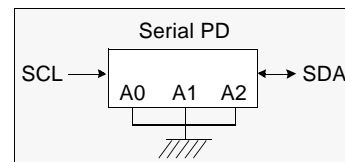
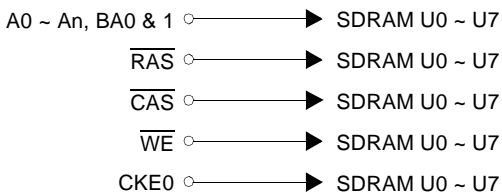
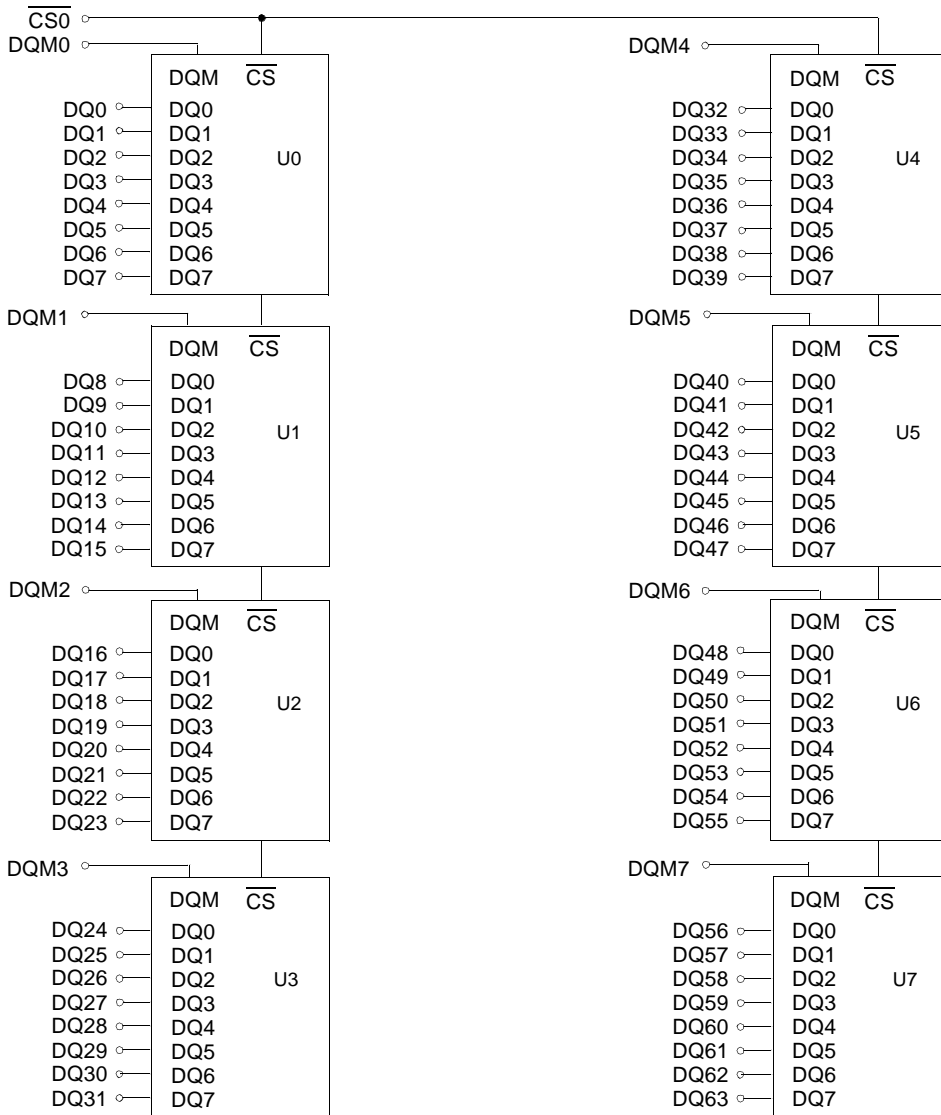


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## PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA8
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	8	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

Recommended operating conditions (Voltage referenced to Vss = 0V, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	
Input high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current	I <sub>LI</sub>	-10	-	10	uA	3

**Notes :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

**CAPACITANCE** (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A <sub>0</sub> ~ A <sub>11</sub> , BA <sub>0</sub> ~ BA <sub>1</sub> )	C <sub>IN1</sub>	23	40	pF
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ )	C <sub>IN2</sub>	23	40	pF
Input capacitance (CKE <sub>0</sub> )	C <sub>IN3</sub>	23	40	pF
Input capacitance (CLK <sub>0</sub> ~ CLK <sub>1</sub> )	C <sub>IN4</sub>	15	21	pF
Input capacitance ( $\overline{\text{CS0}}$ )	C <sub>IN5</sub>	25	45	pF
Input capacitance (DQM <sub>0</sub> ~ DQM <sub>7</sub> )	C <sub>IN6</sub>	8	10	pF
Data input/output capacitance (DQ <sub>0</sub> ~ DQ <sub>63</sub> )	C <sub>OUT</sub>	9	12	pF

**DC CHARACTERISTICS**

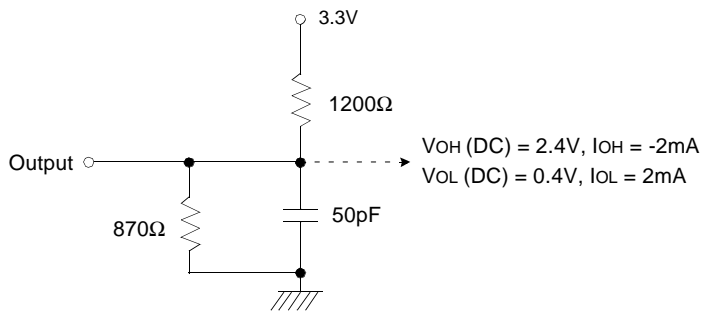
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note	
			-10			
Operating current (One bank active)	ICC1	Burst length = 1 $t_{RC} \geq t_{RC}(\min)$ $I_O = 0 \text{ mA}$	560	mA	1	
Precharge standby current in power-down mode	ICC2P	$CKE \leq V_{IL}(\max)$ , $t_{CC} = 10\text{ns}$	8	mA		
	ICC2PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$ , $t_{CC} = \infty$	8			
Precharge standby current in non power-down mode	ICC2N	$CKE \geq V_{IH}(\min)$ , $\overline{CS} \geq V_{IH}(\min)$ , $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	120	mA		
	ICC2NS	$CKE \geq V_{IH}(\min)$ , $CLK \leq V_{IL}(\max)$ , $t_{CC} = \infty$ Input signals are stable	48			
Active standby current in power-down mode	ICC3P	$CKE \leq V_{IL}(\max)$ , $t_{CC} = 10\text{ns}$	24	mA		
	ICC3PS	$CKE \ \& \ CLK \leq V_{IL}(\max)$ , $t_{CC} = \infty$	24			
Active standby current in non power-down mode (One bank active)	ICC3N	$CKE \geq V_{IH}(\min)$ , $\overline{CS} \geq V_{IH}(\min)$ , $t_{CC} = 10\text{ns}$ Input signals are changed one time during 20ns	200	mA		
	ICC3NS	$CKE \geq V_{IH}(\min)$ , $CLK \leq V_{IL}(\max)$ , $t_{CC} = \infty$ Input signals are stable	120	mA		
Operating current (Burst mode)	ICC4	$I_O = 0 \text{ mA}$ Page burst 4Banks activated $t_{CCD} = 2CLKs$	760	mA	1	
Refresh current	ICC5	$t_{RC} \geq t_{RC}(\min)$	1,000	mA	2	
Self refresh current	ICC6	$CKE \leq 0.2V$	C	8	mA	
			L	3.2	mA	

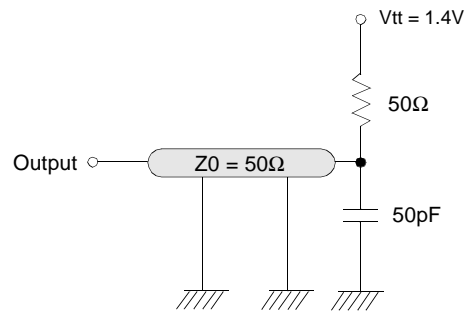
- Notes :**
1. Measured with outputs open.
  2. Refresh period is 64ms.
  3. Unless otherwise noted, input swing level is CMOS( $V_{IH}/V_{IL} = V_{DDQ}/V_{SSQ}$ )

**AC OPERATING TEST CONDITIONS** ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^\circ C$ )

Parameter	Value	Unit
AC input levels ( $V_{ih}/V_{il}$ )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER** (AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-10		
Row active to row active delay	$t_{RRD}(min)$	20	ns	1
RAS to CAS delay	$t_{RCD}(min)$	24	ns	1
Row precharge time	$t_{RP}(min)$	24	ns	1
Row active time	$t_{RAS}(min)$	50	ns	1
Row cycle time	$t_{RAS}(max)$	100	us	
	$t_{RC}(min)$	80	ns	1
Last data in to row precharge	$t_{RD}(min)$	2	CLK	2,5
Last data in to Active delay	$t_{DAL}(min)$	$2 CLK + 20ns$	-	5
Last data in to new col. address delay	$t_{CDL}(min)$	1	CLK	2
Last data in to burst stop	$t_{BDL}(min)$	1	CLK	2
Col. address to col. address delay	$t_{CCD}(min)$	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	CAS latency=2	1		

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.
  5. For -10,  $t_{RD}=1CLK$  and  $t_{DAL}=1CLK+20ns$  is also supported .  
SAMSUNG recommends  $t_{RD}=2CLK$  and  $t_{DAL}=2CLK + 20ns$ .

**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)  
**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-10		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	10	1000	ns	1
	CAS latency=2		13			
CLK to valid output delay	CAS latency=3	tSAC		7	ns	1,2
	CAS latency=2			7		
Output data hold time	CAS latency=3	tOH	3		ns	2
	CAS latency=2		3			
CLK high pulse width		tCH	3.5		ns	3
CLK low pulse width		tCL	3.5		ns	3
Input setup time		tSS	2.5		ns	3
Input hold time		tSH	1.5		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		7	ns	
	CAS latency=2			7		

- Notes :**
- Parameters depend on programmed CAS latency.
  - If clock rising time is longer than 1ns,  $(tr/2-0.5)ns$  should be added to the parameter.
  - Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.  
 If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered,  
 i.e.,  $[(tr + tf)/2-1]ns$  should be added to the parameter.

## SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA <sub>0,1</sub>	A <sub>10/AP</sub>	A <sub>11</sub> , A <sub>9</sub> ~ A <sub>0</sub>	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A <sub>0</sub> ~ A <sub>8</sub> )		4
	Auto precharge enable									H			4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A <sub>0</sub> ~ A <sub>8</sub> )		4
	Auto precharge enable									H			4,5
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X				
				L	V	V	V						
Precharge power down mode	Entry	H	L	H	X	X	X	X	X				
				L	H	H	H						
	Exit	L	H	H	X	X	X	X	X				
				L	V	V	V						
DQM		H	X					V	X			7	
No operation command		H	X	H	X	X	X	X	X				
				L	H	H	H						

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

**Notes :** 1. OP Code : Operand codeA<sub>0</sub> ~ A<sub>11</sub> & BA<sub>0</sub> ~ BA<sub>1</sub> : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA<sub>0</sub> ~ BA<sub>1</sub> : Bank select addresses.If both BA<sub>0</sub> and BA<sub>1</sub> are "Low" at read, write, row active and precharge, bank A is selected.If both BA<sub>0</sub> is "Low" and BA<sub>1</sub> is "High" at read, write, row active and precharge, bank B is selected.If both BA<sub>0</sub> is "High" and BA<sub>1</sub> is "Low" at read, write, row active and precharge, bank C is selected.If both BA<sub>0</sub> and BA<sub>1</sub> are "High" at read, write, row active and precharge, bank D is selected.If A<sub>10/AP</sub> is "High" at row precharge, BA<sub>0</sub> and BA<sub>1</sub> is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t<sub>RP</sub> after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)



