PC66 SODIMM(144pin) SPD Specification
(128Mb C-die base)

Rev. 0.1

May 2000

M466S0924CT0-L1L, C1L

- Organization : 8Mx64
- Composition : 8Mx16*4
- Used component part # : K4S281632C-TL1L, C1L
- # of banks in module : 1 bank
- # of banks in component : 4 banks
- Feature : 1,000mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	60h	2
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	12ns	C0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	CCh	

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	0	30h	
80	..... Manufacturer part # (Module depth)	9	39h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	0	30h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	0	30h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M466S1723CT2-L1L, C1L

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832C-TL1L, C1L
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	60h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	12ns	C0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	D5h	

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
2. This value is based on the component specification.
3. These bytes are programmed by code of Date Week & Date Year.
4. These bytes are programmed by Samsung ′s own Assembly Serial # system. All modules may have different unique serial #.
5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M466S1723CT3-L1L, C1L

- Organization : 16Mx64
- Composition : 16Mx8 *8
- Used component part # : K4S280832C-TL1L, C1L
- # of banks in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,050mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module Rows on this assembly	1 Row	01h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	60h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x8	08h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	12ns	C0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	1 Row of 128MB	20h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	D5h	

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	3	33h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	3	33h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	3	33h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
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5. These bytes are Undefined and can be used for Samsung ′s own purpose.

M466S1724CT2-L1L, C1L

- Organization : 16Mx64
- Composition : 8Mx16 *8
- Used component part # : K4S281632C-TL1L, C1L
- # of banks in module : 2 Rows
- # of banks in component : 4 banks
- Feature : 1,150mil height & double sided component
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	9	09h	1
5	# of module Rows on this assembly	2 Rows	02h	
6	Data width of this assembly	64 bits	40h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	10ns	A0h	2
10	SDRAM access time from clock @CAS latency of 3	6ns	60h	
11	DIMM configuraion type	Non parity	00h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x16	10h	
14	Error checking SDRAM width	None	00h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	2 & 3	06h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Non-buffered, non-registered & redundant addressing	00h	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	12ns	C0h	2
24	SDRAM access time from clock @CAS latency of 2	7ns	70h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	2
26	SDRAM access time from clock @CAS latency of 1	-	00h	2
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	20ns	14h	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	50ns	32h	
31	Module Row density	2 Rows of 64MB	10h	
32~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	2nd edition	01h	
63	Checksum for bytes 0 ~ 62	-	CDh	

Byte #	Function Described	Function Supported	Hex value	Note
		-1L	-1L	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM configuration)	4	34h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	6	36h	
77	..... Manufacturer part # (Data bits)	6	36h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	7	37h	
81	Manufacturer part # (Refresh, # of banks in Comp. & interface)	2	32h	
82	Manufacturer part # (Composition component)	4	34h	
83	Manufacturer part # (Component revision)	C	43h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	2	32h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	L / C	4Ch / 43h	
88	Manufacturer part # (Minimum cycle time)	1	31h	
89	Manufacturer part # (Minimum cycle time)	0	30h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	2	32h	
92	..... Manufacturer revision code (For component)	C-die (4th Gen.)	43h	
93	Manufacturing date (Week)	-	-	3
94	Manufacturing date (Year)	-	-	3
95~98	Assembly serial #	-	-	4
99~12	Manufacturer specific data (may be used in future)	Undefined	-	5
126	System frequency for 66MHz	66MHz	66h	
127	CAS latency for 66MHz	CAS latency of both 2 & 3	06h	
128+	Unused storage locations	Undefined	-	5

Note : 1. The bank select address is excluded in counting the total # of addresses.
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