DDR SDRAM Unbuffered SODIMM

(DDR400 Module)

200pin Unbuffered SODIMM based on 256Mb E-die

64/72-bit ECC/Non ECC

Revision 1.2

March. 2004

Revision History

Revision 1.0 (July, 2003)
- First release

Revision 1.1 (August, 2003)
- Finalized

Revision 1.2 (March, 2004)
- Corrected package dimension.

200Pin Unbuffered SODIMM based on 256Mb E-die (x8)

Ordering Information

Part Number	Density	Organization	Component Composition	Height
M470L6423EN0-C(L)CC	512MB	64M x 64	32Mx8 (K4H560838E) * 16EA	1,250mil

Operating Frequencies

	CC(DDR400@CL=3)
Speed @CL3	200MHz
CL-tRCD-tRP	3-3-3

Feature

- Power supply : Vdd: 2.6V ± 0.1V, Vddq: 2.6V ± 0.1V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 3 (clock) for DDR400 , 2.5 (clock) for DDR333
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1,250 (mil), double(512MB) sided
- SSTL_2 Interface
- 54pin sTSOP(II)-300 package

Pin Configurations (Front side/back side)

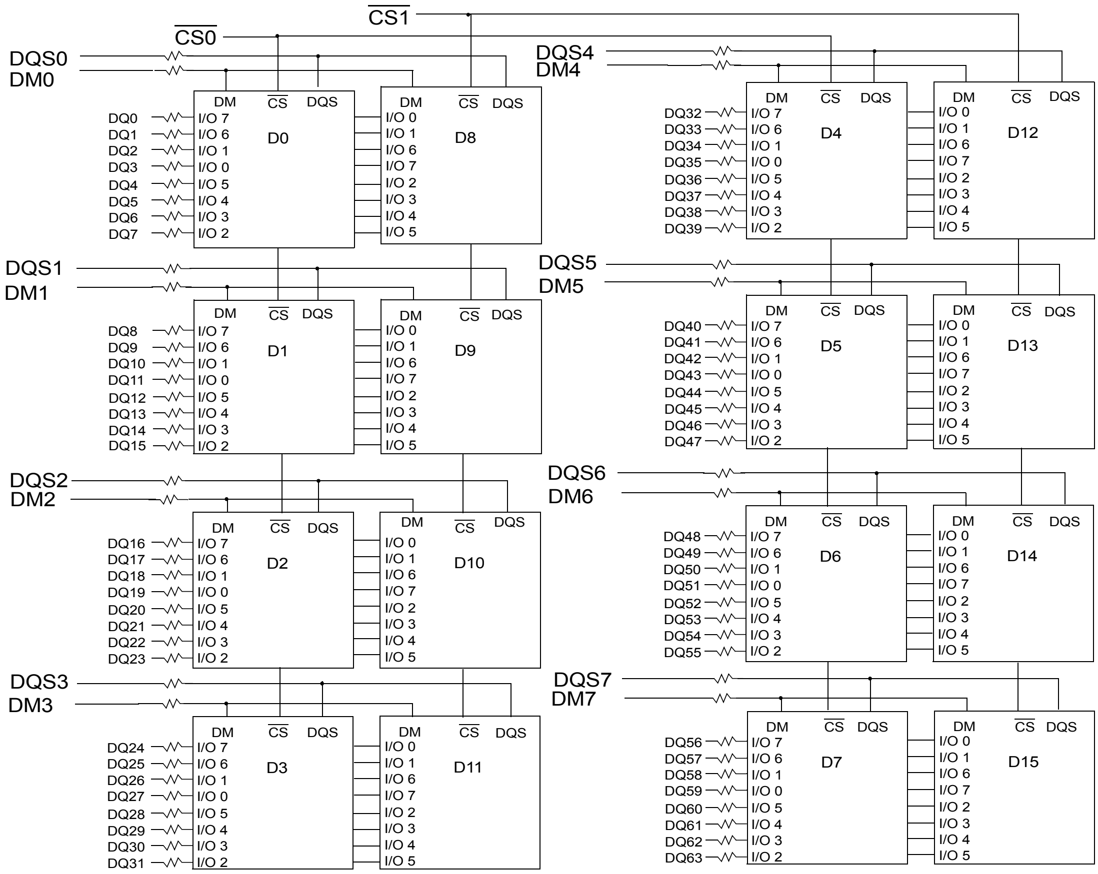
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	67	DQ27	135	DQ34	2	VREF	68	DQ31	136	DQ38
3	VSS	69	VDD	137	VSS	4	VSS	70	VDD	138	VSS
5	DQ0	*71	CB0	139	DQ35	6	DQ4	*72	CB4	140	DQ39
7	DQ1	*73	CB1	141	DQ40	8	DQ5	*74	CB5	142	DQ44
9	VDD	75	VSS	143	VDD	10	VDD	76	VSS	144	VDD
11	DQS0	*77	DQS8	145	DQ41	12	DM0	*78	DM8	146	DQ45
13	DQ2	*79	CB2	147	DQS5	14	DQ6	*80	CB6	148	DM5
15	VSS	81	VDD	149	VSS	16	VSS	82	VDD	150	VSS
17	DQ3	*83	CB3	151	DQ42	18	DQ7	*84	CB7	152	DQ46
19	DQ8	85	DU	153	DQ43	20	DQ12	86	*DU/(RESET)	154	DQ47
21	VDD	87	VSS	155	VDD	22	VDD	88	VSS	156	VDD
23	DQ9	*89	CK2	157	VDD	24	DQ13	90	VSS	158	/CK1
25	DQS1	*91	/CK2	159	VSS	26	DM1	92	VDD	160	CK1
27	VSS	93	VDD	161	VSS	28	VSS	94	VDD	162	VSS
29	DQ10	*95	CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52
31	DQ11	97	DU	165	DQ49	32	DQ15	98	DU(BA2)	166	DQ53
33	VDD	99	A12	167	VDD	34	VDD	100	A11	168	VDD
35	CK0	101	A9	169	DQS6	36	VDD	102	A8	170	DM6
37	/CK0	103	VSS	171	DQ50	38	VSS	104	VSS	172	DQ54
39	VSS	105	A7	173	VSS	40	VSS	106	A6	174	VSS
KEY		107	A5	175	DQ51	KEY		108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7
49	DQ18	117	BA0	185	VSS	50	DQ22	118	/RAS	186	VSS
51	VSS	119	/WE	187	DQ58	52	VSS	120	/CAS	188	DQ62
53	DQ19	121	/CS0	189	DQ59	54	DQ23	*122	/CS1	190	DQ63
55	DQ24	123	*DU(A13)	191	VDD	56	DQ28	124	DU	192	VDD
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2

Note 1. * : These pins are not used in this module.
2. Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are reserved for x72 module, and are not used on x64 module.
Pin 95,122 are NC for 8Mx16 based module & used for 16Mx8 based module.
3. Pins 89, 91 are reserved for x72 modules.

Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~ 7	Data - in mask
BA0 ~ BA1	Bank Select Address	VDD	Power supply (2.6V)
DQ0 ~ DQ63	Data input/output	VDDQ	Power Supply for DQS(2.6V)
DQS0 ~ DQS7	Data Strobe input/output	VSS	Ground
CK0,$\overline{\text{CK0}}$ ~ CK1, $\overline{\text{CK1}}$	Clock input	VREF	Power supply for reference
CKE0 ~ CKE1	Clock enable input	VDDSPD	Serial EEPROM Power
$\overline{\text{CS0}}$ ~ $\overline{\text{CS1}}$	Chip select input	SDA	Serial data I/O
$\overline{\text{RAS}}$	Row address strobe	SCL	Serial clock
$\overline{\text{CAS}}$	Column address strobe	SA0 ~ 2	Address in EEPROM
$\overline{\text{WE}}$	Write enable	NC	No connection

FUNCTIONAL BLOCK DIAGRAM



BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D15

A0 - A12 → A0-A12 : DDR SDRAMs D0 - D15

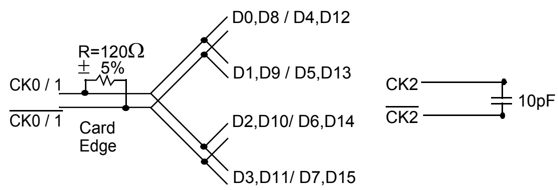
$\overline{RAS}$ → $\overline{RAS}$: DDR SDRAMs D0 - D15

$\overline{CAS}$ → $\overline{CAS}$: DDR SDRAMs D0 - D15

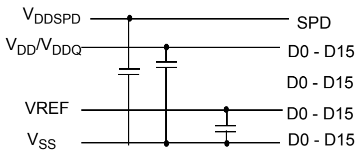
CKE1 → CKE : DDR SDRAMs D8 - D15

CKE0 → CKE : DDR SDRAMs D0 - D7

$\overline{WE}$ → $\overline{WE}$: DDR SDRAMs D0 - D15



*Clock Net Wiring



Notes :
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/$\overline{CS}$ relationships must be maintained as shown
3. DQ, DQS, DM/DQS resistors: 22 Ohm.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.5 * # of component	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommend operation condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

Recommended operating conditions(Voltage referenced to VSS=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 2.5V)	VDD	2.5	2.7		5
I/O Supply voltage	VDDQ	2.5	2.7	V	5
I/O Reference voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	1
I/O Termination voltage(system)	V_{TT}	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	VIH(DC)	VREF+0.15	VDDQ+0.3	V	
Input logic low voltage	VIL(DC)	-0.3	VREF-0.15	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	VIN(DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	VID(DC)	0.36	VDDQ+0.6	V	3
V-I Matching: Pullup to Pulldown Current Ratio	VI(Ratio)	0.71	1.4	-	4
Input leakage current	II	-2	2	uA	
Output leakage current	IOZ	-5	5	uA	
Output High Current(Normal strengh driver) ;$V_{OUT} = V_{TT} + 0.84V$	IOH	-16.8		mA	
Output High Current(Normal strengh driver) ;$V_{OUT} = V_{TT} - 0.84V$	IOL	16.8		mA	
Output High Current(Half strengh driver) ;$V_{OUT} = V_{TT} + 0.45V$	IOH	-9		mA	
Output High Current(Half strengh driver) ;$V_{OUT} = V_{TT} - 0.45V$	IOL	9		mA	

Note : 1.VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on VREF may not exceed +/-2% of the dc value.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
3. VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1/7 for device drain to source voltages from 0.1 to 1.0.
5. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20MHz. Any noise above 20MHz at the DRAM generated from any source other than the DRAM itself may not exceed the DC voltage range of 2.6V +/-100mV.

DDR SDRAM module IDD spec table

Symbol		CC(DDR333@CL3.0)	Unit	Notes
IDD0		1440	mA	
IDD1		1640	mA	
IDD2P		65	mA	
IDD2F		480	mA	
IDD2Q		400	mA	
IDD3P		880	mA	
IDD3N		1200	mA	
IDD4R		2080	mA	
IDD4W		2120	mA	
IDD5		2040	mA	
IDD6	Normal	48	mA	
	Low power	24	mA	Optional
IDD7A		3080	mA	

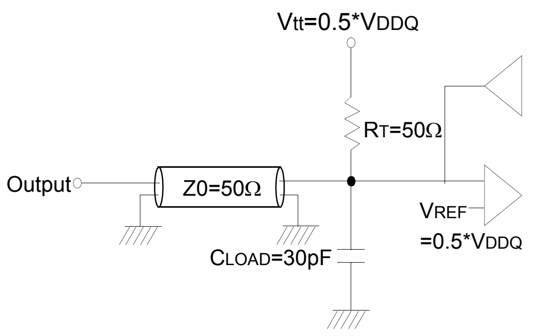
* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note 1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (VDD=2.6V, VDDQ=2.6V, TA= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	Vtt	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE (VDD=2.6V, VDDQ=2.6V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A_0 ~ A_{12}, BA_0 ~ BA_1,$\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN1}	38	47	pF
Input capacitance(CKE0/CKE1)	C_{IN2}	38	47	pF
Input capacitance($\overline{CS0}$/$\overline{CS1}$)	C_{IN3}	36	44	pF
Input capacitance(CLK0, CLK1)	C_{IN4}	36	40	pF
Data & DQS input/output capacitance(DQ_0~DQ_{63})	C_{OUT}	12	14	pF
Input capacitance(DM_0~DM_7)	C_{IN5}	12	14	pF

AC Timing Parameters and Specifications

Parameter		Symbol	CC(DDR400@CL=3)		Unit	Note
			Min	Max		
Row cycle time		tRC	55		ns	
Refresh row cycle time		tRFC	70		ns	
Row active time		tRAS	40	70K	ns	
RAS to CAS delay		tRCD	15		ns	
Row precharge time		tRP	15		ns	
Row active to Row active delay		tRRD	10		ns	
Write recovery time		tWR	15		ns	
Internal write to read command delay		tWTR	2		tCK	
Clock cycle time	CL=3.0	tCK	5	10	ns	16
	CL=2.5		6	12	ns	
Clock high level width		tCH	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	tCK	
DQS-out access time from CK/CK		tDQSCK	-0.55	+0.55	ns	
Output data access time from CK/CK		tAC	-0.65	+0.65	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.4	ns	13
Read Preamble		tRPRE	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.72	1.28	tCK	
Write preamble setup time		tWPRES	0		ps	5
Write preamble		tWPRE	0.25		tCK	
Write postamble		tWPST	0.4	0.6	tCK	4
DQS falling edge to CK rising-setup time		tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		tCK	
DQS-in high level width		tDQSH	0.35		tCK	
DQS-in low level width		tDQSL	0.35		tCK	
Address and Control Input setup time		tIS	0.6		ns	h,7~10
Address and Control Input hold time		tIH	0.6		ns	h,7~10
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-	tAC max	ns	3
Data-out low impedence time from CK/$\overline{CK}$		tLZ	tAC min	tAC max	ns	3
Mode register set cycle time		tMRD	2		tCK	
DQ & DM setup time to DQS, slew rate 0.5V/ns		tDS	0.4		ns	i, j
DQ & DM hold time to DQS, slew rate 0.5V/ns		tDH	0.4		ns	i, j
DQ & DM input pulse width		tDIPW	1.75		ns	9
Control & Address input pulse width for each input		tIPW	2.2		ns	9
Refresh interval time	Up to 128Mb	tREFI		15.6	us	6
	256Mb, 512Mb, 1Gb			7.8	us	
Output DQS valid window		tQH	tHP -tQHS	-	ns	12
Clock half period		tHP	min tCH/tCL	-	ns	11, 12

Parameter	Symbol	CC(DDR400@CL=3)		Unit	Note
		Min	Max		
Data hold skew factor	tQHS		0.5	ns	12
Auto Precharge write recovery + precharge time	tDAL	-	-	ns	14
Exit self refresh to non-READ command	tXSNR	75		ns	15
Exit self refresh to READ command	tXSRD	200	-	tCK	

Component Notes

1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

2. The value of VIX is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. these parameters are not referenced to a specific voltage level but specify when the device output in no longer driving (HZ), or begins driving (LZ).

4. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but sys tem performance (bus turnaround) will degrade accordingly.

5. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previ ously in progress on the bus, DQS will be tran sitioning from High- Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

6. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.

7. For command/address input slew rate ≥ 0.5 V/ns

8. For CK & $\overline{CK}$ slew rate ≥ 0.5 V/ns

9. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

10. Slew Rate is measured between VOH(ac) and VOL(ac).

11. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

12. tQH = tHP - tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one tansition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

13. tDQSQ
Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

14. tDAL = (tWR/tCK) + (tRP/tCK)
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR400(CC) at CL=3 and tCK=5ns tDAL = (15 ns / 5 ns) + (15 ns/ 5ns) = (3) + (3)
tDAL = 6 clocks

15. In all circumstances, tXSNR can be satisfied using tXSNR=tRFCmin+1*tCK

16. The only time that the clock frequency is allowed to change is during self-refresh mode.

System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR400 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS		DDR400			
PARAMETER	SYMBOL	MIN	MAX	Units	Notes
DQ/DM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4.0	V/ns	a, k

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tIS	tIH	Units	Notes
0.5 V/ns	0	0	ps	h
0.4 V/ns	+50	0	ps	h
0.3 V/ns	+100	0	ps	h

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	tDS	tDH	Units	Notes
0.5 V/ns	0	0	ps	j
0.4 V/ns	+75	+75	ps	j
0.3 V/ns	+150	+150	ps	j

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	tDS	tDH	Units	Notes
+/- 0.0 V/ns	0	0	ps	i
+/- 0.25 V/ns	+50	+50	ps	i
+/- 0.5 V/ns	+100	+100	ps	i

Table 5 : Output Slew Rate Characteristice (X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g

Table 6 : Output Slew Rate Characteristice (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS	DDR400		
PARAMETER	MIN	MAX	Notes
Output Slew Rate Matching Ratio (Pullup to Pulldown)	-	-	e,k

System Notes :

a. Pullup slew rate is characteristized under the test conditions as shown in Figure 1.

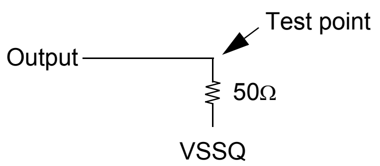


Figure 1 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 2.

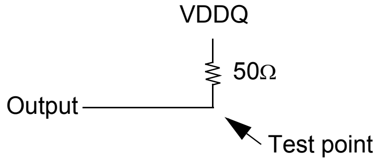


Figure 2 : Pulldown slew rate test load

c. Pullup slew rate is measured between (VDDQ/2 - 320 mV +/- 250 mV)
Pulldown slew rate is measured between (VDDQ/2 + 320 mV +/- 250 mV)
Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.
Example : For typical slew rate, DQ0 is switching
For minmum slew rate, all DQ bits are switching from either high to low, or low to high.
For Maximum slew rate, only one DQ is switching from either high to low, or low to high.
The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions
Typical : 25 °C (T Ambient), VDDQ = 2.6V, typical process
Minimum : 70 °C (T Ambient), VDDQ = 2.5V, slow - slow process
Maximum : 0 °C (T Ambient), VDDQ = 2.7V, fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOPII package divices only.

h. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates detemined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.

i. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either VIH(AC) to VIL(AC) or VIH(DC) to VIL(DC), similarly for rising transitions.
The delta rise/fall rate is calculated as:
{1/(Slew Rate1)} - {1/(Slew Rate2)}

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

j. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser on the lesser of the AC - AC slew rate and the DC- DC slew rate. The inut slew rate is based on the lesser of the slew rates deter mined by either VIH(ac) to VIL(ac) or VIH(DC) to VIL(DC), and similarly for rising transitions.

k. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transi tions through the DC region must be monotony.

Command Truth Table

(V=Valid, X=Don′t Care, H=Logic High, L=Logic Low)

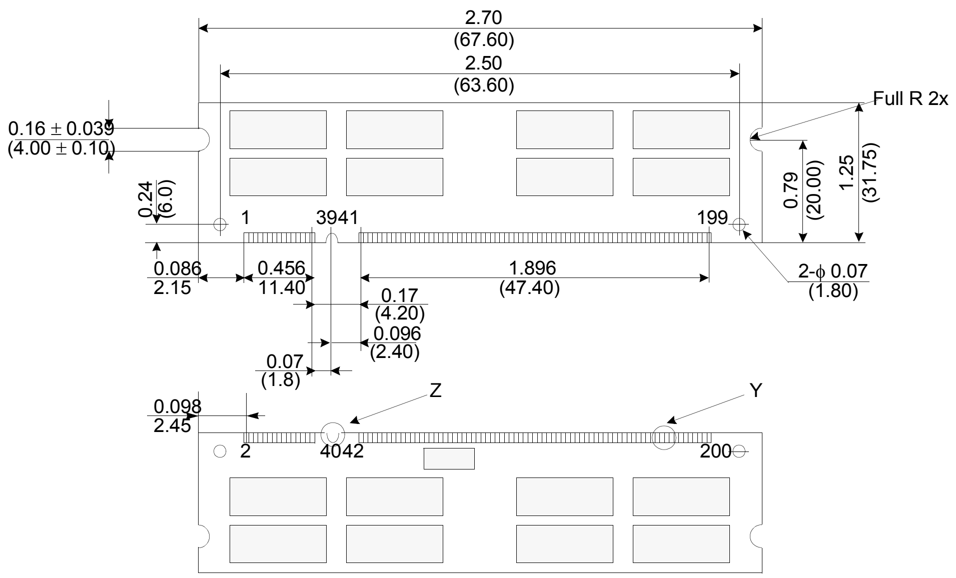
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A12, A11 A9 ~ A0	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry	H	L	L	L	L	H	X			3
	Self Refresh	Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

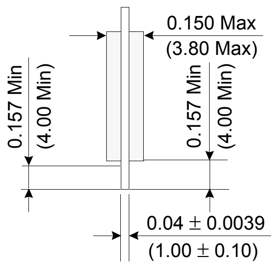
Note : 1. OP Code : Operand Code. $A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@EMRS/MRS)

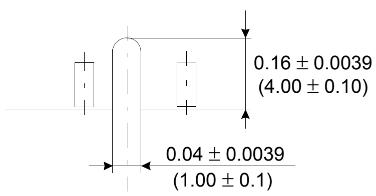
2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

PACKAGE DIMENSIONS

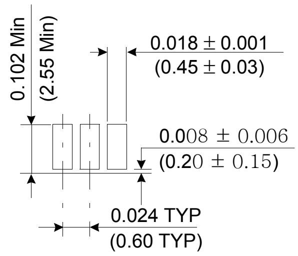
Units : Inches (Millimeters)







Detail Z



Detail Y

Tolerances : ±.006(.15) unless otherwise specified

The used device is 32Mx8 DDR SDRAM, sTSOP-300mil
SDRAM Part No. : K4H560838E-N***