

M485L0914DT0

200pin DDR SDRAM SODIMM

64MB DDR SDRAM MODULE

(8Mx72 based on 8Mx16 DDR SDRAM)

200pin SODIMM
72-bit ECC/Parity

Revision 1.0

Dec. 2002

M485L0914DT0

200pin DDR SDRAM SODIMM

Revision History

Revision 1.0 (Dec. 2002)

1. First release.

M485L0914DT0

200pin DDR SDRAM SODIMM

M485L0914DT0 200pin DDR SDRAM SODIMM

8Mx72 200pin DDR SDRAM SODIMM based on 8Mx16

GENERAL DESCRIPTION

The Samsung M485L0914DT0 is 8M bit x 72 Double Data Rate SDRAM high density memory modules based on first gen of 128Mb DDR SDRAM respectively.

The Samsung M485L0914DT0 consists of five CMOS 8M x 16 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 200pin glass-epoxy substrate. Three 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM.

The M485L0914DT0 is Dual In-line Memory Modules and intended for mounting into 200pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No.	Max Freq.	Interface
M485L0914DT0-C(L)B3	133MHz(6ns@CL=2.5)	SSTL_2
M485L0914DT0-C(L)A2	133MHz(7.5ns@CL=2)	
M485L0914DT0-C(L)B0	133MHz(7.5ns@CL=2.5)	

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and \overline{CK})
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 15.6us refresh interval(4K/64ms refresh)
- Serial presence detect with EEPROM
- JEDEC standard PCB
- PCB: Height 1250(mil), double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	VREF	67	DQ27	135	DQ34	2	VREF	68	DQ31	136	DQ38		
3	VSS	69	VDD	137	VSS	4	VSS	70	VDD	138	VSS		
5	DQ0	71	CB0	139	DQ35	6	DQ4	72	CB4	140	DQ39		
7	DQ1	73	CB1	141	DQ40	8	DQ5	74	CB5	142	DQ44		
9	VDD	75	VSS	143	VDD	10	VDD	76	VSS	144	VDD		
11	DQS0	77	DQS8	145	DQ41	12	DM0	78	DM8	146	DQ45		
13	DQ2	79	CB2	147	DQS5	14	DQ6	80	CB6	148	DM5		
15	VSS	81	VDD	149	VSS	16	VSS	82	VDD	150	VSS		
17	DQ3	83	CB3	151	DQ42	18	DQ7	84	CB7	152	DQ46		
19	DQ8	85	DU	153	DQ43	20	DQ12	86	DU/(RESET)	154	DQ47		
21	VDD	87	VSS	155	VDD	22	VDD	88	VSS	156	VDD		
23	DQ9	89	CK2	157	VDD	24	DQ13	90	VSS	158	/CK1		
25	DQS1	91	/CK2	159	VSS	26	DM1	92	VDD	160	CK1		
27	VSS	93	VDD	161	VSS	28	VSS	94	VDD	162	VSS		
29	DQ10	95	CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52		
31	DQ11	97	DU(A13)	165	DQ49	32	DQ15	98	DU(BA2)	166	DQ53		
33	VDD	99	A12	167	VDD	34	VDD	100	A11	168	VDD		
35	CK0	101	A9	169	DQS6	36	VDD	102	A8	170	DM6		
37	/CK0	103	VSS	171	DQ50	38	VSS	104	VSS	172	DQ54		
	Key	105	A7	173	VSS		Key	106	A6	174	VSS		
		107	A5	175	DQ51			108	A4	176	DQ55		
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60		
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD		
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61		
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7		
49	DQ18	117	BA0	185	VSS	50	DQ22	118	/RAS	186	VSS		
51	VSS	119	/WE	187	DQ58	52	VSS	120	/CAS	188	DQ62		
53	DQ19	121	/CS0	189	DQ59	54	DQ23	122	*/CS1	190	DQ63		
55	DQ24	123	DU	191	VDD	56	DQ28	124	DU	192	VDD		
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0		
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1		
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2		
63	VSS	131	VDD	199	VDDID	64	VSS	132	VDD	200	DU		
65	DQ26	133	DQS4			66	DQ30	134	DM4				

PIN DESCRIPTION

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0~ CK2, CK0~ CK2	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DM0 ~ DM7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

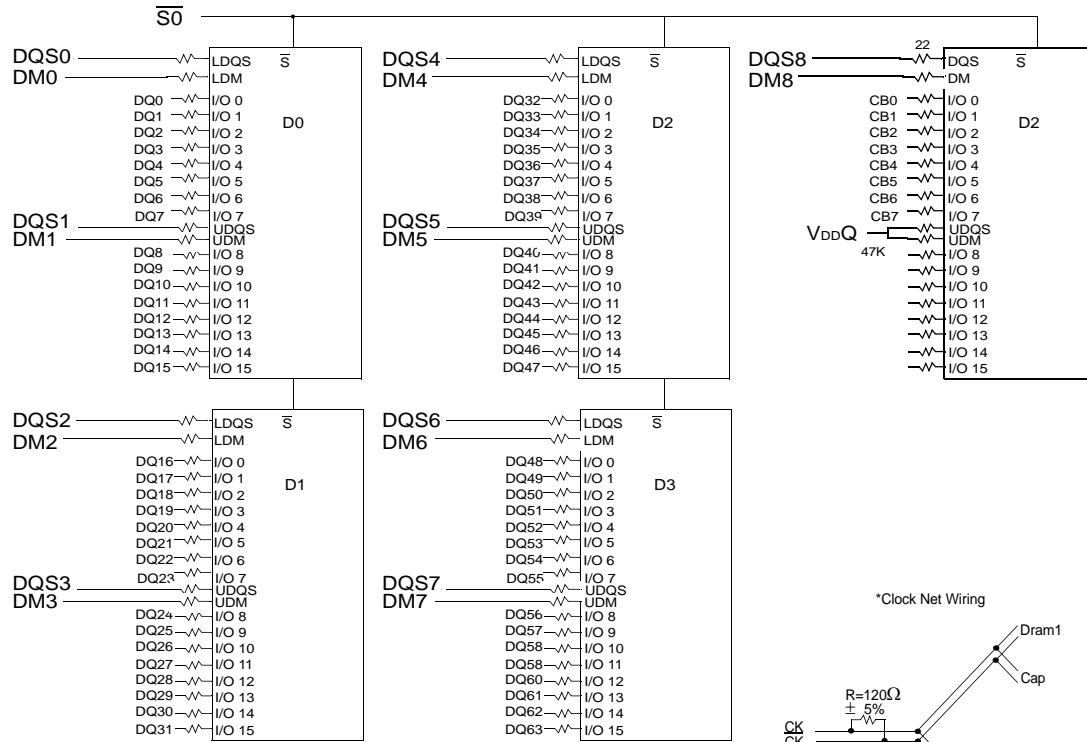
* These pins are not used in this module.

SAMSUNG ELECTRONICS CO., Ltd. reserves the right to change products and specifications without notice.

M485L0914DT0

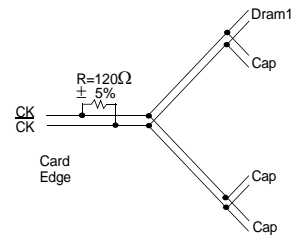
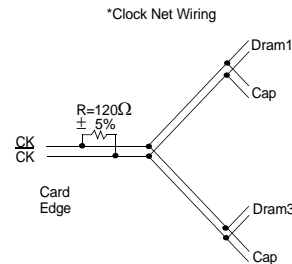
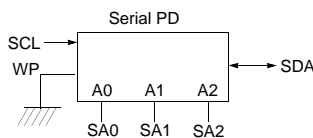
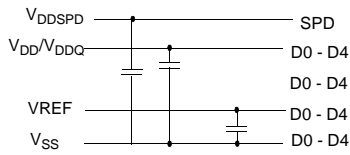
200pin DDR SDRAM SODIMM

FUNCTIONAL BLOCK DIAGRAM



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D4
- A0 - A11 → A0-A11: DDR SDRAMs D0 - D4
- $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: SDRAMs D0 - D4
- $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: SDRAMs D0 - D4
- CKE0 → CKE: SDRAMs D0 - D4
- $\overline{\text{WE}}$ → $\overline{\text{WE}}$: SDRAMs D0 - D4

Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	2 SDRAMs
CK1/CK1	2 SDRAMs
CK2/CK2	1 SDRAMs



- Notes:
- DQ-to-I/O wiring is shown as recommended but may be changed.
 - DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
 - DQ, DQS, DM/DQS resistors: 22 Ohms.

M485L0914DT0

200pin DDR SDRAM SODIMM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	VDDQ	-0.5 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	5	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 2.5V)	VDD	2.3	2.7		
I/O Supply voltage	VDDQ	2.3	2.7	V	
I/O Reference voltage	VREF	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V _{TT}	VREF-0.04	VREF+0.04	V	2
Input logic high voltage	V _{IH} (DC)	VREF+0.15	VDDQ+0.3	V	4
Input logic low voltage	V _{IL} (DC)	-0.3	VREF-0.15	V	4
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	V _{IN} (DC)	-0.3	VDDQ+0.3	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	V _{ID} (DC)	0.3	VDDQ+0.6	V	3
Input crossing point voltage, CK and $\overline{\text{CK}}$ inputs	V _{IX} (DC)	1.15	1.35	V	5
Input leakage current	I _I	-2	2	uA	
Output leakage current	I _{OZ}	-5	5	uA	
Output High Current(Normal strength driver) ;V _{OUT} = V _{TT} + 0.84V	I _{OH}	-16.8		mA	
Output High Current(Normal strength driver) ;V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8		mA	
Output High Current(Half strength driver) ;V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9		mA	
Output High Current(Half strength driver) ;V _{OUT} = V _{TT} - 0.45V	I _{OL}	9		mA	

- Notes**
- Includes ± 25mV margin for DC offset on VREF, and a combined total of ± 50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of ≤ 3nH.
 - V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
 - V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.
 - These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
 - The value of V_{IX} is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.
 - These characteristics obey the SSTL-2 class II standards.

M485L0914DT0

200pin DDR SDRAM SODIMM

DDR SDRAM module I_{DD} spec table

Symbol		A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	Unit	Notes
IDD0		400	400	mA	
IDD1		500	500	mA	
IDD2P		12.5	12.5	mA	
IDD2F		120	120	mA	
IDD2Q		75	75	mA	
IDD3P		175	175	mA	
IDD3N		250	250	mA	
IDD4R		725	725	mA	
IDD4W		625	625	mA	
IDD5		725	725	mA	
IDD6	Normal	10	10	mA	
	Low power	5	5	mA	Optional
IDD7A		1500	1500	mA	

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

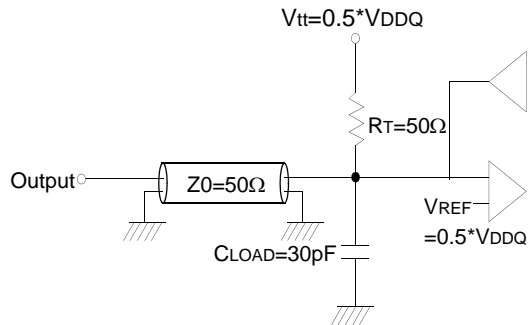
- Note 1. VID is the magnitude of the difference between the input level on CK and the input on \overline{CK} .
 2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
 3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V, V_{DDQ}=2.5V, T_A= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	V _{tt}	V	
Output load condition	See Load Circuit		

M485L0914DT0

200pin DDR SDRAM SODIMM



Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE ($V_{DD}=2.5V$, $V_{DDQ}=2.5V$, $T_A=25^{\circ}C$, $f=1MHz$)

Parameter	Symbol	Min	Max	Unit
Input capacitance($A_0 \sim A_{11}$, $BA_0 \sim BA_1$, \overline{RAS} , \overline{CAS} , \overline{WE})	CIN1	15	20	pF
Input capacitance(CKE_0)	CIN2	15	20	pF
Input capacitance(\overline{CS}_0)	CIN3	15	20	pF
Input capacitance(CLK_0 , CLK_1 , CLK_2)	CIN4	15	20	pF
Data & DQS input/output capacitance($DQ_0 \sim DQ_{63}$)	COUT	9	10	pF
Input capacitance($DM_0 \sim DM_8$)	CIN5	9	10	pF

M485L0914DT0

200pin DDR SDRAM SODIMM

AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)

Parameter	Symbol	A2(DDR266@CL=2)		B0(DDR266@CL=2.5)		Unit	Note	
		Min	Max	Min	Max			
Row cycle time	tRC	65		65		ns		
Refresh row cycle time	tRFC	75		75		ns		
Row active time	tRAS	45	120K	45	120K	ns		
RAS to CAS delay	tRCD	20		20		ns		
Row precharge time	tRP	20		20		ns		
Row active to Row active delay	tRRD	15		15		ns		
Write recovery time	tWR	2		2		tCK		
Last data in to Read command	tCDLR	1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	10	12	ns	5
		CL=2.5	7.5	12	7.5	12	ns	5
Clock high level width	tCH	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSK	-0.75	+0.75	-0.75	+0.75	ns		
Output data access time from CK/CK	tAC	-0.75	+0.75	-0.75	+0.75	ns		
Data strobe edge to output data edge	tDQSQ	-	+0.5	-	+0.5	ns	5	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		ns	2	
DQS-in hold time	tWPREH	0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time	tIS	0.9		0.9		ns	6	
Address and Control Input hold time	tIH	0.9		0.9		ns	6	
Data-out high impedance time from CK/CK	tHZ	tACmin - 400ps	tACmax - 400ps	tACmin - 400ps	tACmax - 400ps	ps		
Data-out low impedance time from CK/CK	tLZ	tACmin - 400ps	tACmax - 400ps	tACmin - 400ps	tACmax - 400ps	ps		
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		V/ns	6	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		V/ns	7	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	V/ns	10	
Output Slew Rate(x16)	tSL(O)	0.7	5	0.7	5	V/ns	10	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5			

M485L0914DT0

200pin DDR SDRAM SODIMM

Parameter	Symbol	A2(DDR266@CL=2)		B0(DDR266@CL=2.5)		Unit	Note
		Min	Max	Min	Max		
Mode register set cycle time	tMRD	15		15		ns	
DQ & DM setup time to DQS	tDS	0.5		0.5		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		0.5		ns	7,8,9
DQ & DM input pulse width	tDIPW	1.75		1.75		ns	
Power down exit time	tPDEX	10		10		ns	
Exit self refresh to write command	tXSW	95				ns	
Exit self refresh to bank active command	tXSA	75		75		ns	4
Exit self refresh to read command	tXSR	200		200		Cycle	
Refresh interval time	tREF	15.6		15.6		us	1
Output DQS valid window	tQH	tHPmin -tQHS	-	tHPmin -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.75		0.75	ns	
DQS write postamble time	tWPST	0.25		0.25		tCK	3

Note :

- Maximum burst refresh of 8
- The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with tRCD satisfied after this command.
- For registered DINNs, tCL and tCH are $\geq 45\%$ of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.

6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt_{IS}	Δt_{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	Δt_{DS}	Δt_{DH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

M485L0914DT0

200pin DDR SDRAM SODIMM

8. I/O Setup/Hold Plateau Derating

I/O Input Level	Δt_{DS}	Δt_{DH}
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase t_{DS}/t_{DH} in the case where the input level is flat below $V_{REF} \pm 310mV$ for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	Δt_{DS}	Δt_{DH}
(ns/V)	(ps)	(ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as $1/SlewRate1-1/SlewRate2$. For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guaranteed by design.

M485L0914DT0

200pin DDR SDRAM SODIMM

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0,1	A10/AP	A11 A9 ~ A0	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L							3	
		Exit	L	H	L	H	H	H	X		3	
	H		X	X	X	3						
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable								H	4		
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable								H	4, 6		
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry	H	L	H	X	X	X	X				
				L	V	V	V					
	Exit	L	H	X	X	X	X					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X				
				L	H	H	H					
	Exit	L	H	H	X	X	X					
				L	V	V	V					
DM		H	X					X		8		
No operation (NOP) : Not defined		H	X	H	X	X	X	X		9		
				L	H	H	H			9		

Note : 1. OP Code : Operand Code. A0 ~ A11 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at tRP after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

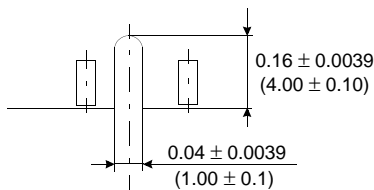
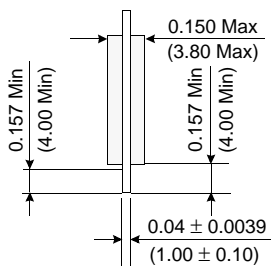
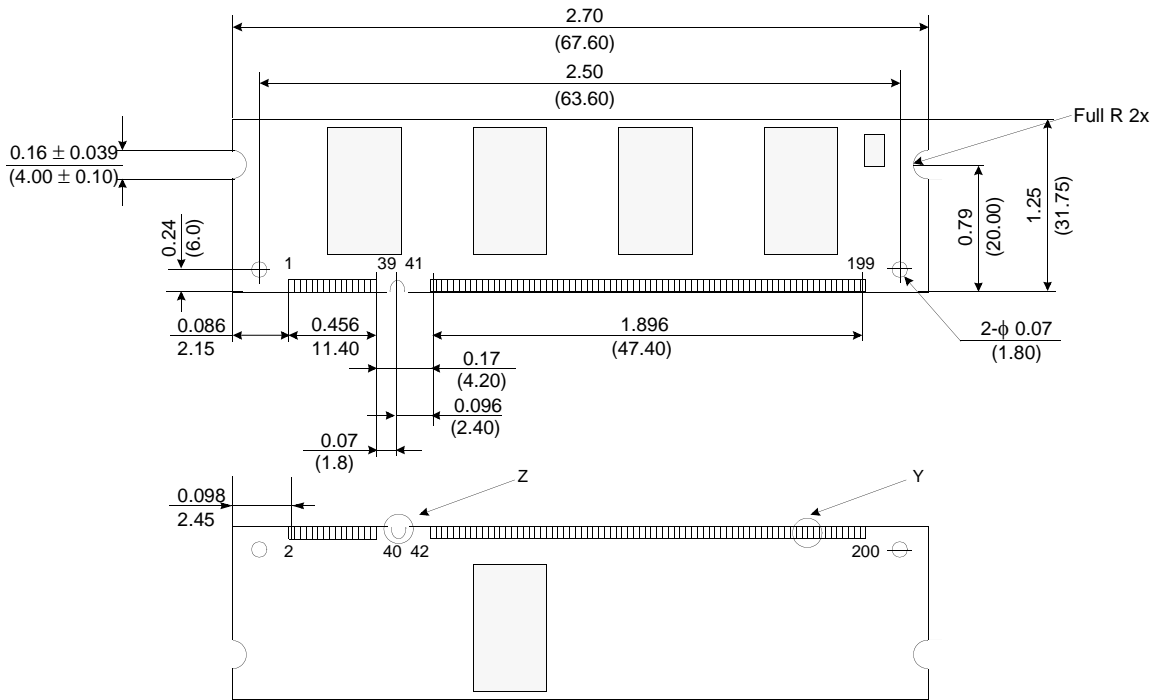
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

M485L0914DT0

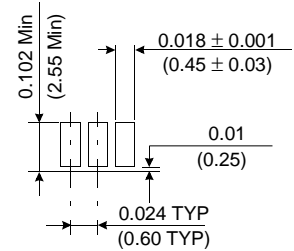
200pin DDR SDRAM SODIMM

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances : ±.006(.15) unless otherwise specified

The used device is 8Mx16 DDR SDRAM, TSOP
 DDR SDRAM Part No. : K4H281638D-TC/L