

**DRAM MODULE**

**M53210224DE2/DJ2**

**M53210224DE2/DJ2 with Fast Page Mode**

2M x 32 DRAM SIMM using 1Mx16, 1K Refresh, 5V

**GENERAL DESCRIPTION**

The Samsung M53210224D is a 2Mx32bits Dynamic RAM high density memory module. The Samsung M53210224D consists of four CMOS 1Mx16bits DRAMs in 42-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M53210224D is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

**FEATURES**

- Part Identification
  - M53210224DE2-C(1024 cycles/16ms Ref, SOJ, Solder)
  - M53210224DJ2-C(1024 cycles/16ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- CAS-before-RAS refresh capability
- RAS-only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height(750mil), double sided component

**PERFORMANCE RANGE**

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>
-50	50ns	15ns	90ns
-60	60ns	15ns	110ns

**PIN CONFIGURATIONS**

Pin	Symbol	Pin	Symbol
1	V <sub>ss</sub>	37	NC
2	DQ0	38	NC
3	DQ16	39	<u>V<sub>ss</sub></u>
4	DQ1	40	<u>CAS0</u>
5	DQ17	41	<u>CAS2</u>
6	DQ2	42	<u>CAS3</u>
7	DQ18	43	<u>CAS1</u>
8	DQ3	44	<u>RAS0</u>
9	DQ19	45	<u>RAS1</u>
10	V <sub>cc</sub>	46	<u>NC</u>
11	NC	47	<u>W</u>
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	Res(A10)	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	V <sub>cc</sub>
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	Res(A11)	65	DQ15
30	V <sub>cc</sub>	66	NC
31	A8	67	PD1
32	<u>A9</u>	68	PD2
33	<u>RAS1</u>	69	PD3
34	<u>RAS0</u>	70	PD4
35	NC	71	NC
36	NC	72	V <sub>ss</sub>

**PIN NAMES**

Pin Name	Function
A0 - A9	Address Inputs
DQ0 - DQ31	Data In/Out
<u>W</u>	Read/Write Enable
<u>RAS0</u> , <u>RAS1</u>	Row Address Strobe
<u>CAS0</u> - <u>CAS3</u>	Column Address Strobe
PD1 -PD4	Presence Detect
V <sub>cc</sub>	Power(+5V)
V <sub>ss</sub>	Ground
NC	No Connection
Res	Reserved Pin

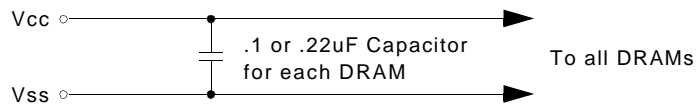
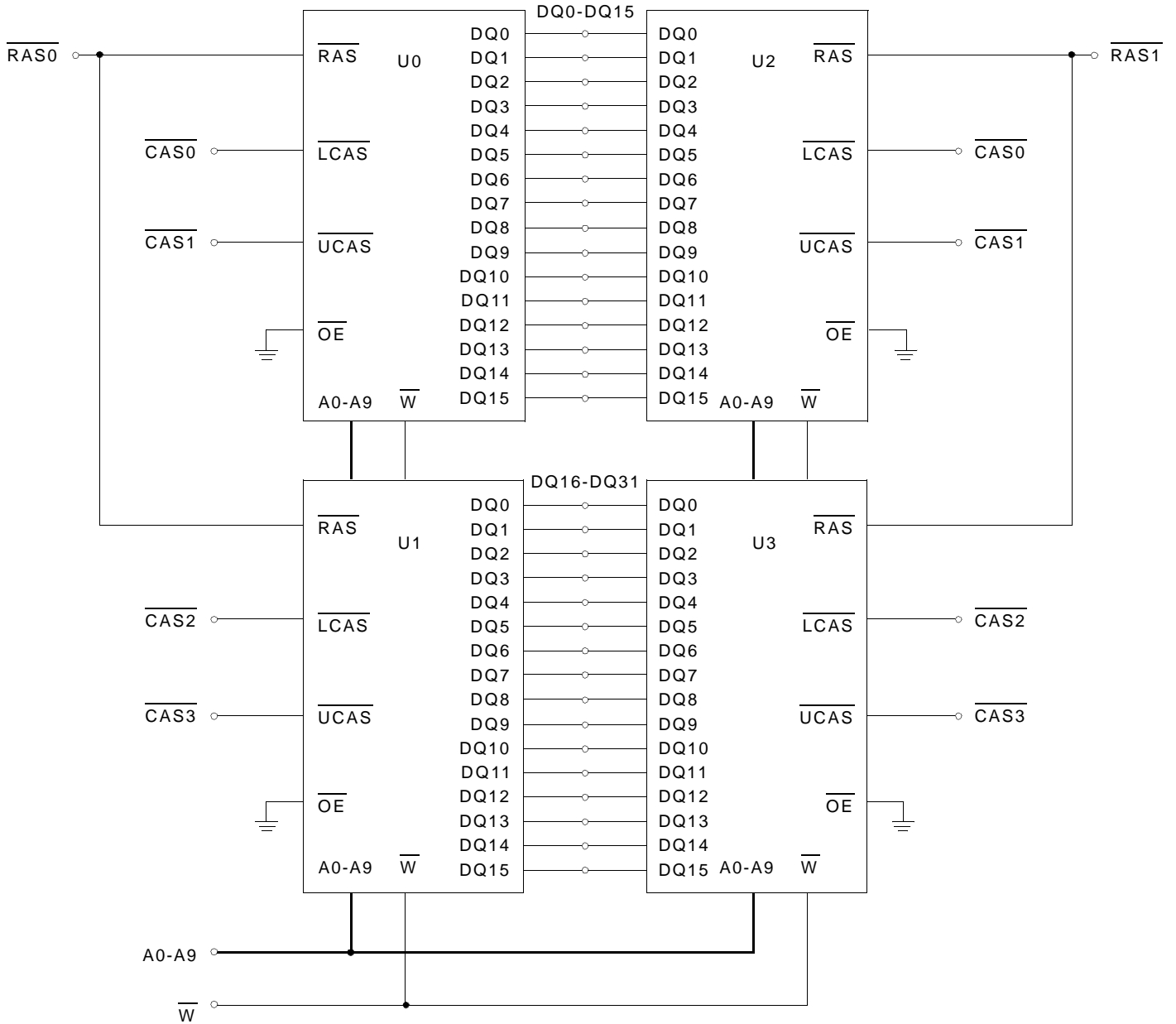
**PRESENCE DETECT PINS (Optional)**

Pin	50NS	60NS
PD1	NC	NC
PD2	NC	NC
PD3	V <sub>ss</sub>	NC
PD4	V <sub>ss</sub>	NC

\* Pin connection changing available

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FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS \***

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>d</sub>	4	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to Vss, T<sub>A</sub> = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> +1 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-1.0 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+2.0V/20ns, Pulse width is measured at V<sub>CC</sub>.

\*2 : -2.0V/20ns, Pulse width is measured at V<sub>SS</sub>.

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53210224DE2/DJ2		Unit
		Min	Max	
I <sub>CC1</sub>	-50	-	304	mA
	-60	-	284	mA
I <sub>CC2</sub>	Don't care	-	8	mA
I <sub>CC3</sub>	-50	-	304	mA
	-60	-	284	mA
I <sub>CC4</sub>	-50	-	184	mA
	-60	-	164	mA
I <sub>CC5</sub>	Don't care	-	4	mA
I <sub>CC6</sub>	-50	-	304	mA
	-60	-	284	mA
I <sub>I(L)</sub>	Don't care	-20	20	uA
I <sub>O(L)</sub>		-10	10	uA
V <sub>OH</sub>	Don't care	2.4	-	V
V <sub>OL</sub>		-	0.4	V

I<sub>CC1</sub> : Operating Current \* (R<sub>AS</sub>, L<sub>CAS</sub> or U<sub>CAS</sub>, Address cycling @t<sub>RC</sub>=min)

I<sub>CC2</sub> : Standby Current (R<sub>AS</sub>=L<sub>CAS</sub>=U<sub>CAS</sub>=W=V<sub>IH</sub>)

I<sub>CC3</sub> : R<sub>AS</sub> Only Refresh Current \* (L<sub>CAS</sub>=U<sub>CAS</sub>=V<sub>IH</sub>, R<sub>AS</sub> cycling @t<sub>RC</sub>=min)

I<sub>CC4</sub> : Fast Page Mode Current \* (R<sub>AS</sub>=V<sub>IL</sub>, L<sub>CAS</sub> or U<sub>CAS</sub> cycling : t<sub>PC</sub>=min)

I<sub>CC5</sub> : Standby Current (R<sub>AS</sub>=L<sub>CAS</sub>=U<sub>CAS</sub>=W=V<sub>CC</sub>-0.2V)

I<sub>CC6</sub> : CAS-Before-RAS Refresh Current \* (R<sub>AS</sub> and C<sub>AS</sub> cycling @t<sub>RC</sub>=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input 0≤V<sub>IN</sub>≤V<sub>CC</sub>+0.5V, all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled, 0V≤V<sub>OUT</sub>≤V<sub>CC</sub>)

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -5mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 4.2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while R<sub>AS</sub>=V<sub>IL</sub>. In I<sub>CC4</sub>, address can be changed maximum once within one page mode cycle, t<sub>PC</sub>.

**DRAM MODULE**

**M53210224DE2/DJ2**

**CAPACITANCE** (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A9]	CIN1	-	35	pF
Input capacitance[W]	CIN2	-	45	pF
Input capacitance[RAS0 , RAS1]	CIN3	-	40	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	30	pF
Input/Output capacitance[DQ0-31]	CDQ	-	30	pF

**AC CHARACTERISTICS** (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4
Access time from CAS	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
CAS to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	ns	6
Transition time(rise and fall)	tT	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
CAS hold time	tCSH	50		60		ns	
CAS pulse width	tCAS	13	10K	15	10K	ns	
$\overline{\text{RAS}}$ to CAS delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
CAS to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to CAS	tRCH	0		0		ns	8
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to CAS lead time	tCWL	13		15		ns	
Data-in set-up time	tDS	0		0		ns	9
Data-in hold time	tDH	10		10		ns	9
Refresh period	tREF		16		16	ms	
Write command set-up time	tWCS	0		0		ns	7
CAS setup time(CAS-before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
CAS hold time(CAS-before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ precharge to CAS hold time	tRPC	5		5		ns	
Access time from CAS precharge	tCPA		30		35	ns	3

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=5.0V ± 10%. See notes 1,2.)

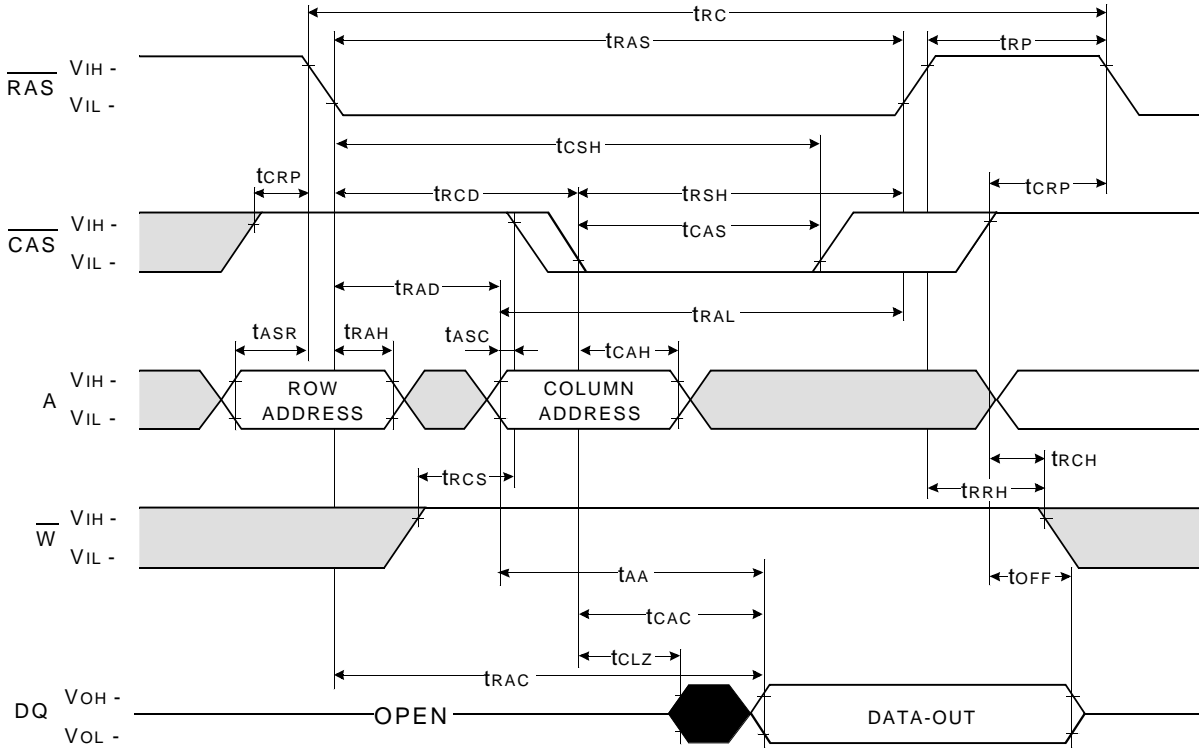
Test condition : VIH/VIIL=2.4/0.8V, VOH/VOL=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Fast page mode cycle time	tPC	35		40		ns	
CAS precharge time(Fast page cycle)	tCP	10		10		ns	
RAS pulse width(Fast page cycle)	tRASP	50	200K	60	200K	ns	
W to RAS precharge time(C-B-R refresh)	tWRP	10		10		ns	
W to RAS hold time(C-B-R refresh)	tWRH	10		10		ns	

NOTES

- An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
- VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
- Assumes that tRCD ≥ tRCD(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
- twcs is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs ≥ twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either tRCH or tRRH must be satisfied for a read cycle.
- These parameter are referenced to the CAS leading edge in early write cycles.
- Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.

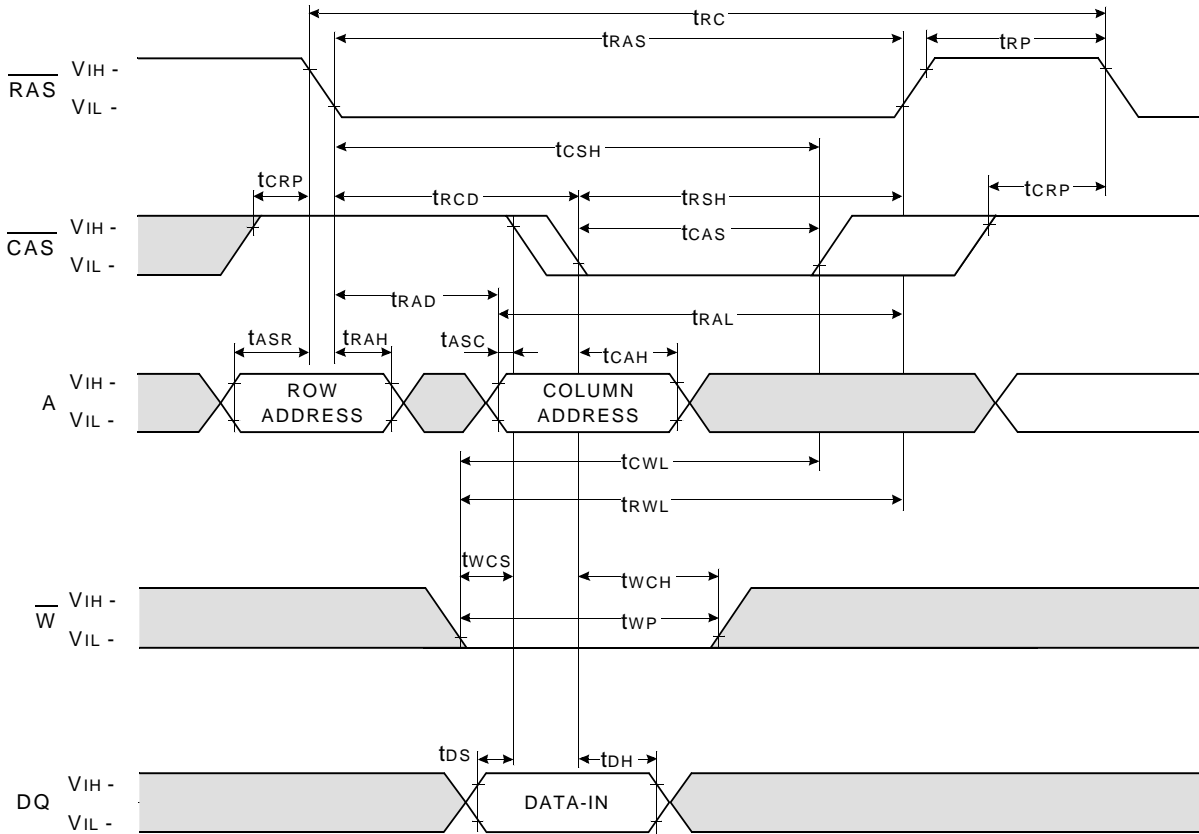
READ CYCLE



□ Don't care  
■ Undefined

WRITE CYCLE ( EARLY WRITE )

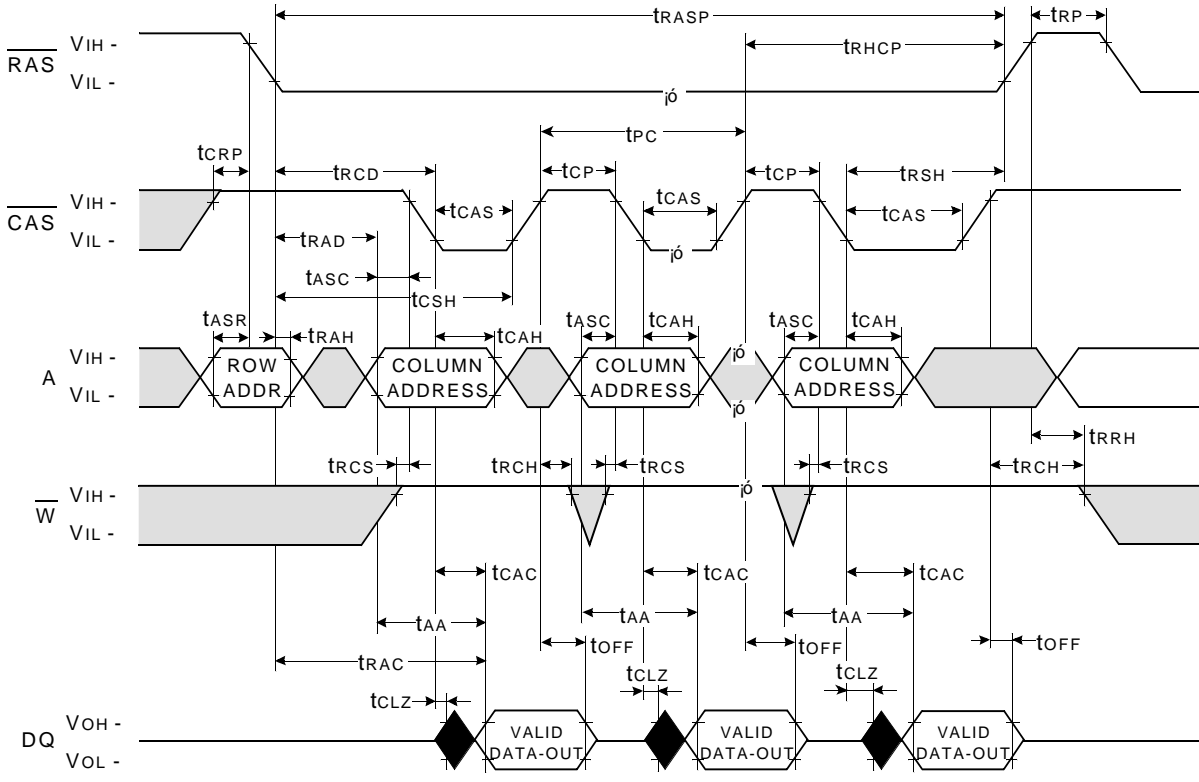
NOTE : DOUT = OPEN



□ Don't care  
■ Undefined

FAST PAGE READ CYCLE

NOTE : DOUT = OPEN

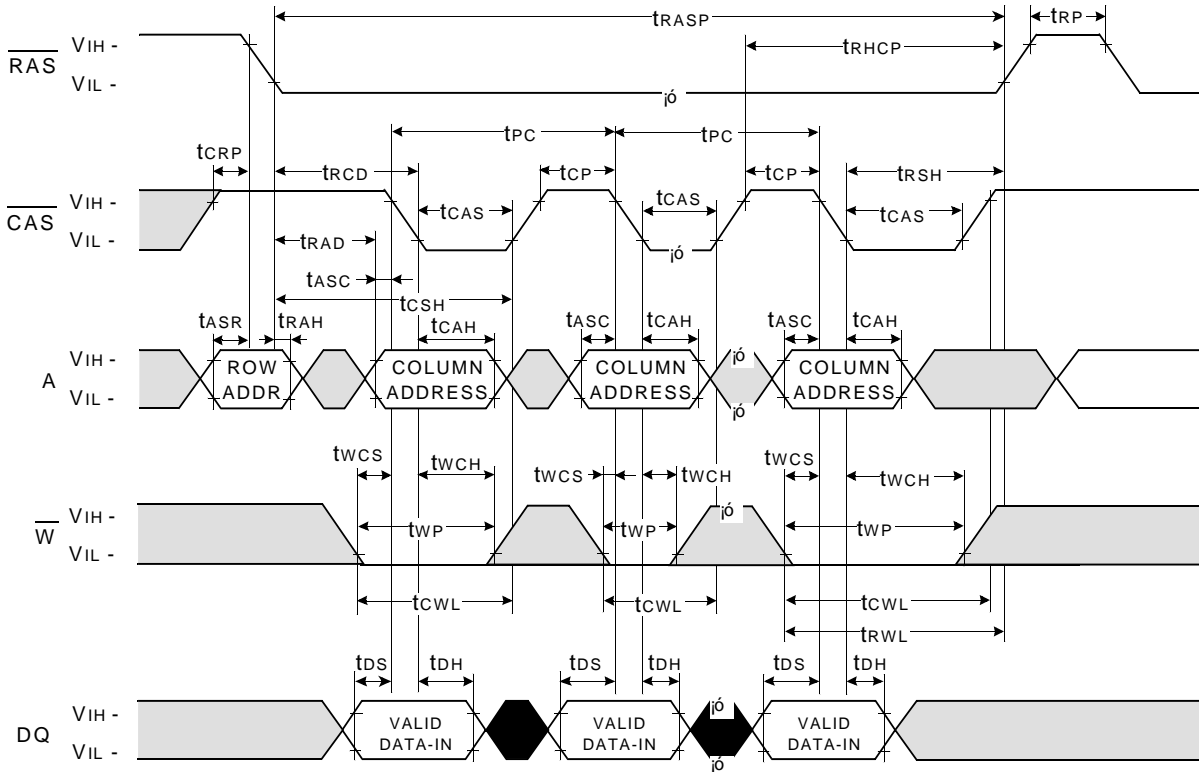


Don't care  
Undefined



FAST PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



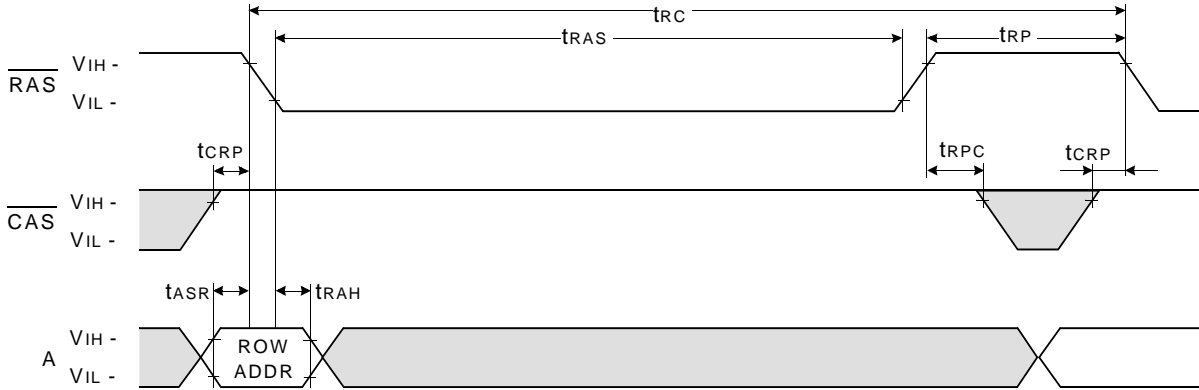
□ Don't care  
■ Undefined

DRAM MODULE

**RAS - ONLY REFRESH CYCLE**

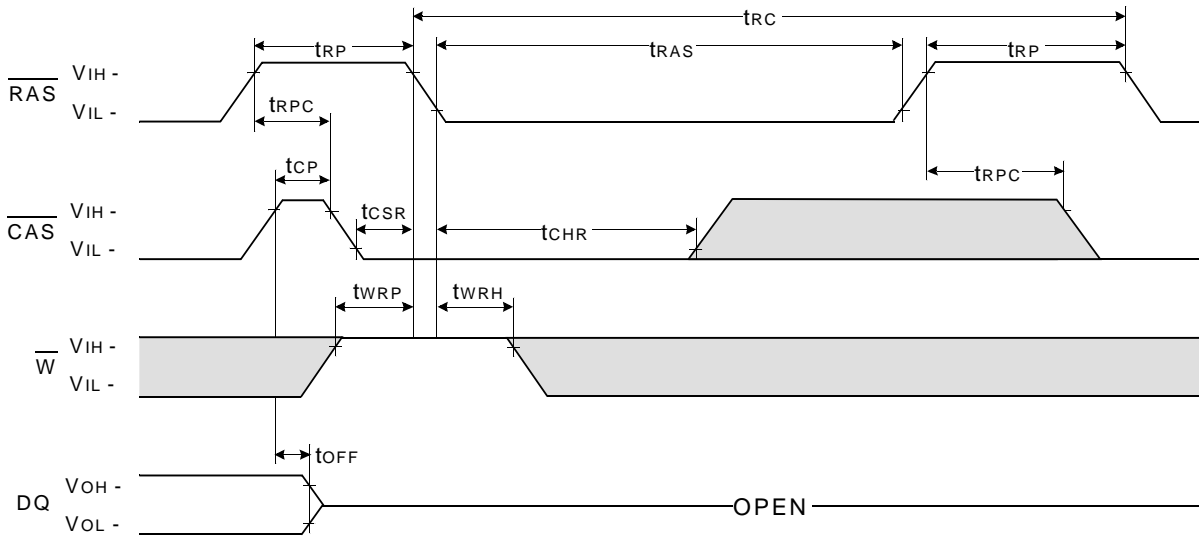
NOTE :  $\overline{W}$ ,  $\overline{OE}$ ,  $DIN$  = Don't care

DOUT = OPEN



**CAS - BEFORE - RAS REFRESH CYCLE**

NOTE :  $\overline{OE}$ ,  $A$  = Don't care

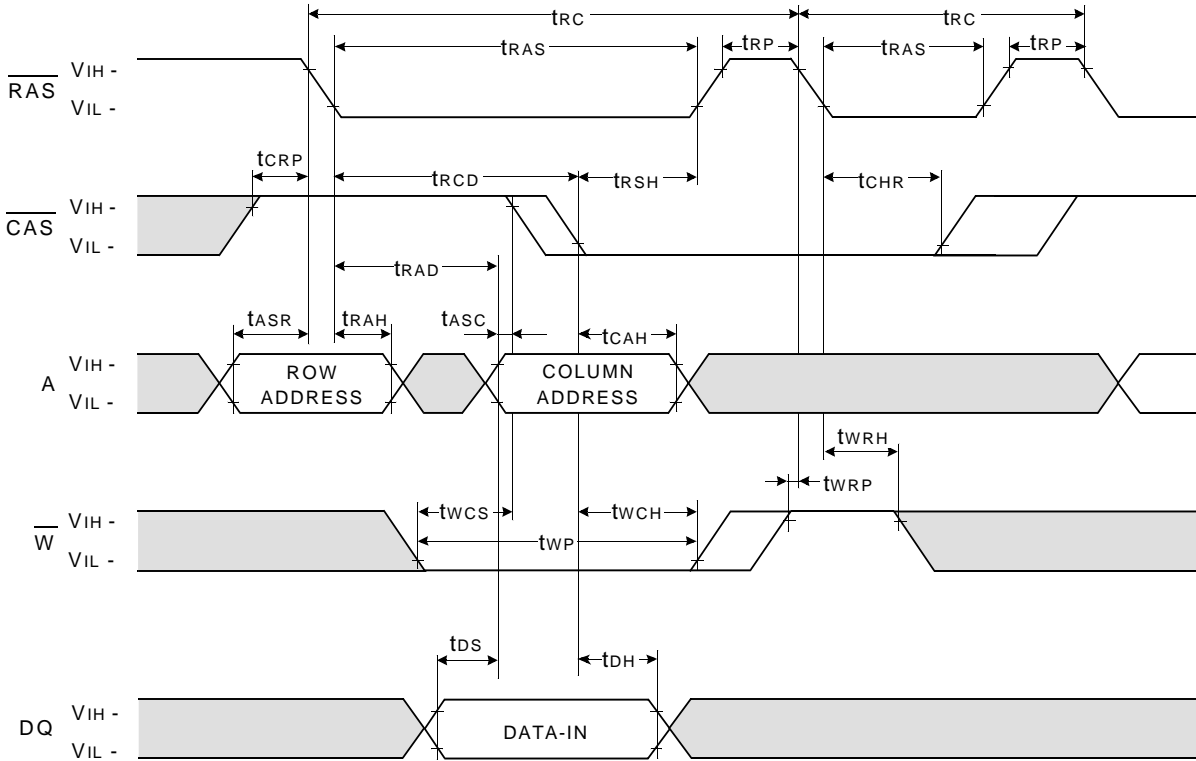


Don't care  
 Undefined



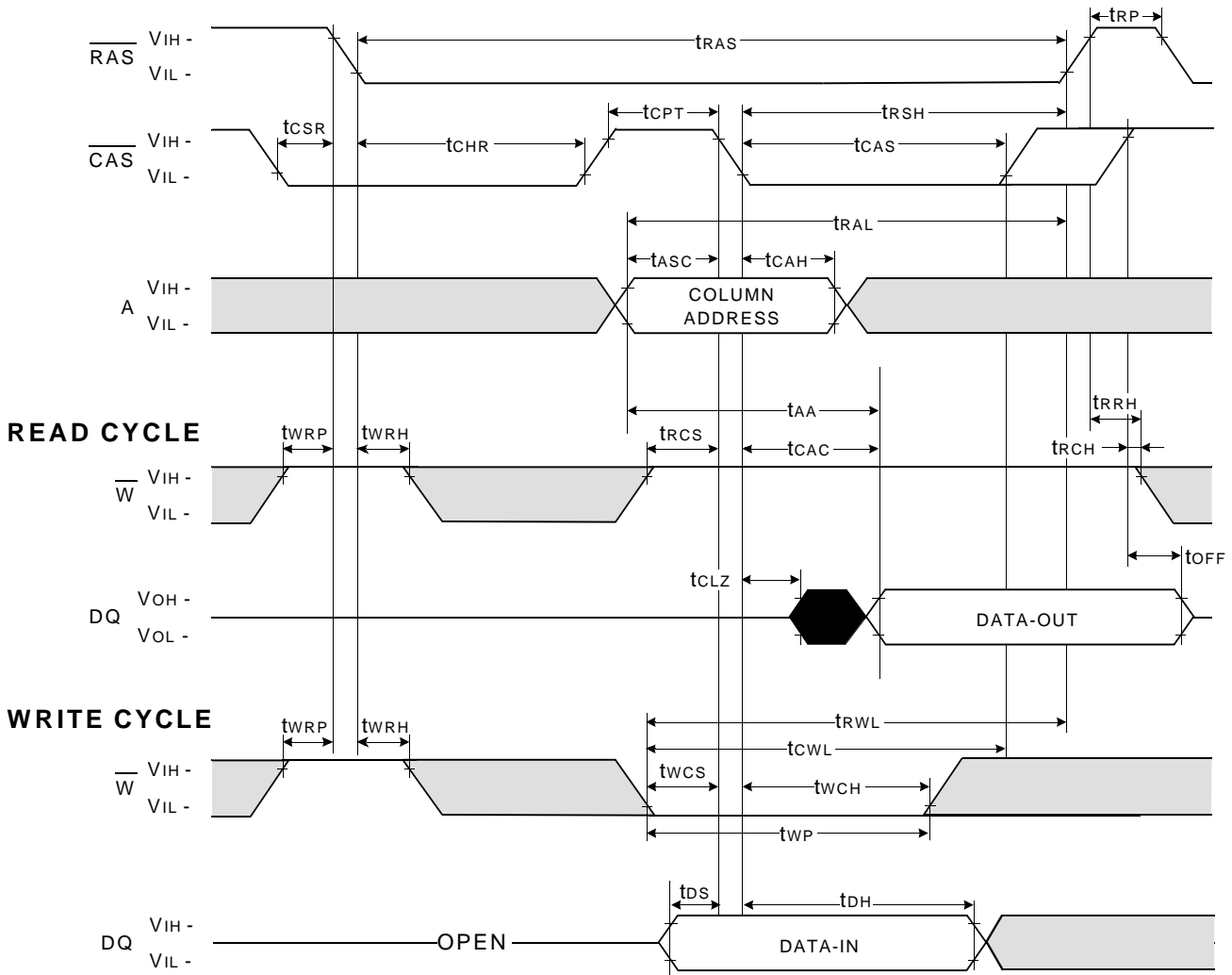
HIDDEN REFRESH CYCLE ( WRITE )

NOTE : DOUT = OPEN



□ Don't care  
■ Undefined

CAS-BEFORE-RAS REFRESH CYCLE

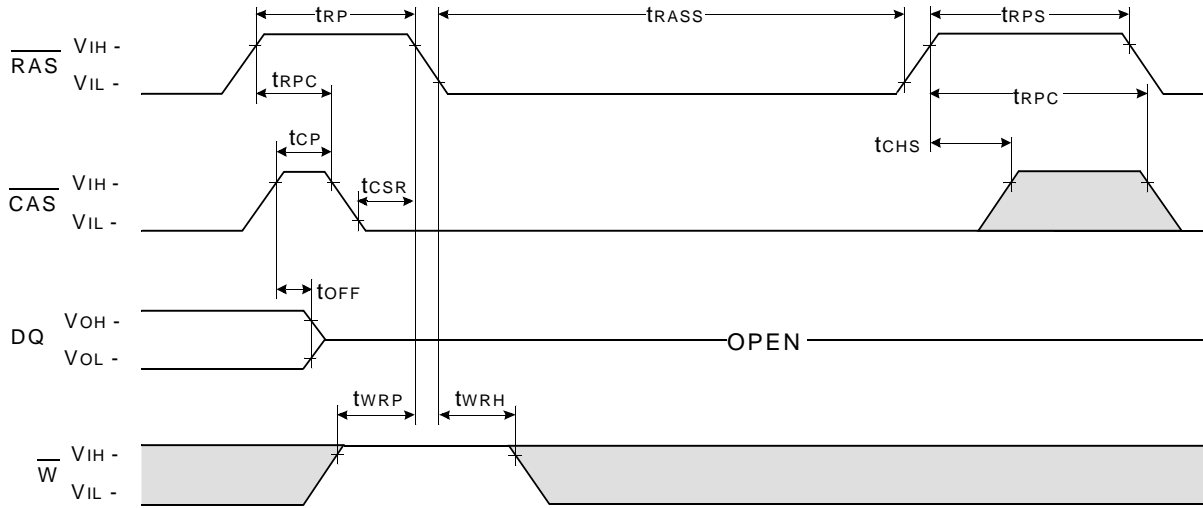


□ Don't care  
■ Undefined

NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

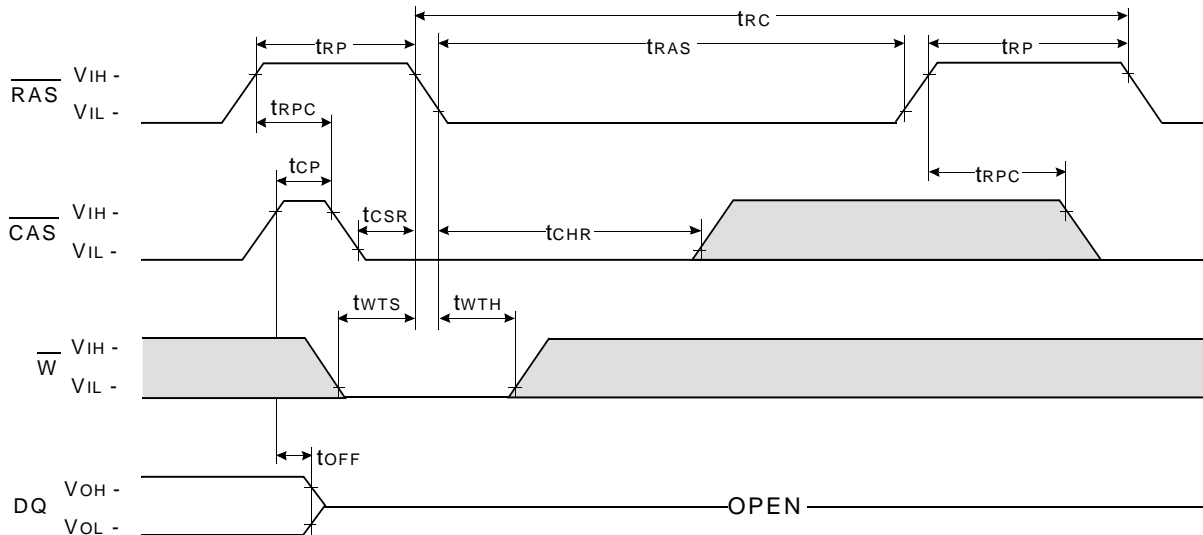
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

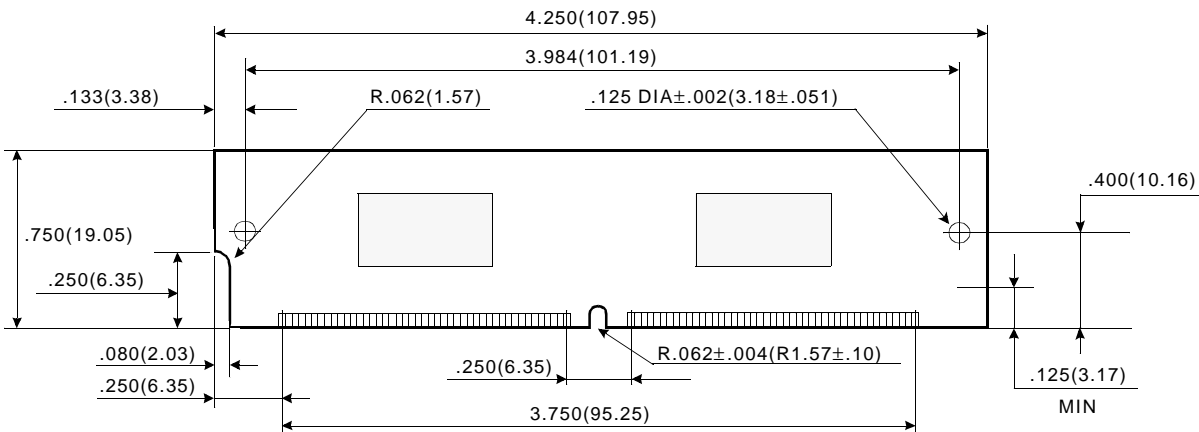
NOTE :  $\overline{OE}$ , A = Don't care



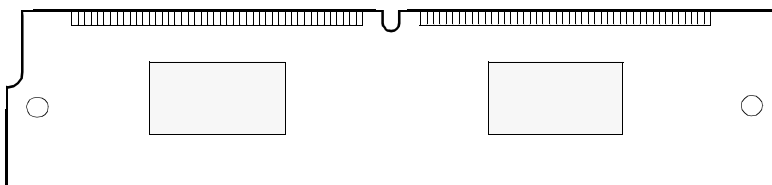
□ Don't care  
■ Undefined

**PACKAGE DIMENSIONS**

Units : Inches (millimeters)

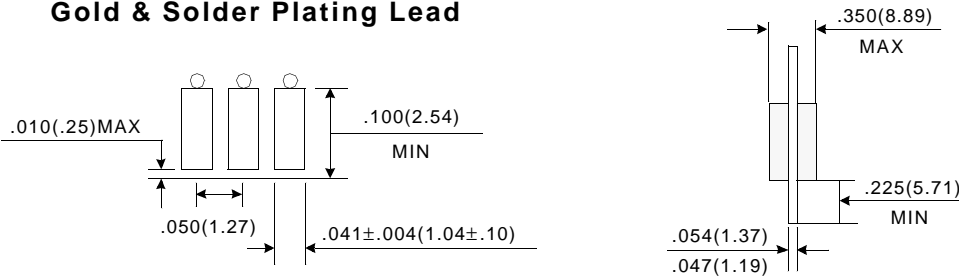


( Front view )



( Back view )

**Gold & Solder Plating Lead**



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 1Mx16 DRAM

DRAM Part No. : M53210224DE2/DJ2 -- K4F151611D-J(400 mil)

Revision History  
Rev 0.0 : Oct. 1999