

**DRAM MODULE**

**M53230800CW0/CB0 & M53230810CW0/CB0 EDO Mode**

8M x 32 DRAM SIMM using 4Mx4, 4K/2K Refresh, 5V

**GENERAL DESCRIPTION**

The Samsung M5323080(1)0C is a 8Mx32bits Dynamic RAM high density memory module. The Samsung M5323080(1)0C consists of sixteen CMOS 4Mx4bits DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M5323080(1)0C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

**PERFORMANCE RANGE**

Speed	tRAC	tCAC	tRC	tHPC
-50	50ns	13ns	90ns	25ns
-60	60ns	15ns	110ns	30ns

**FEATURES**

- Part Identification
  - M53230800CW0-C(4096 cycles/64ms Ref, SOJ, Solder)
  - M53230800CB0-C(4096 cycles/64ms Ref, SOJ, Gold)
  - M53230810CW0-C(2048 cycles/32ms Ref, SOJ, Solder)
  - M53230810CB0-C(2048 cycles/32ms Ref, SOJ, Gold)
- Extended Data Out
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- 1st Gen. JEDEC standard PDPin & pinout
- PCB : Height(1000mil), double sided component

**PIN CONFIGURATIONS**

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	$\overline{\text{Vss}}$
4	DQ1	40	$\overline{\text{CAS0}}$
5	DQ17	41	$\overline{\text{CAS2}}$
6	DQ2	42	$\overline{\text{CAS3}}$
7	DQ18	43	$\overline{\text{CAS1}}$
8	DQ3	44	$\overline{\text{RAS0}}$
9	DQ19	45	RAS1
10	Vcc	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	A11	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{\text{RAS1}}$	69	PD3
34	$\overline{\text{RAS0}}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

**PIN NAMES**

Pin Name	Function
A0 - A11	Address Inputs(4K Ref)
A0 - A10	Address Inputs(2K Ref)
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}, \overline{\text{RAS1}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

**PRESENCE DETECT PINS (Optional)**

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

\* Pin connection changing available

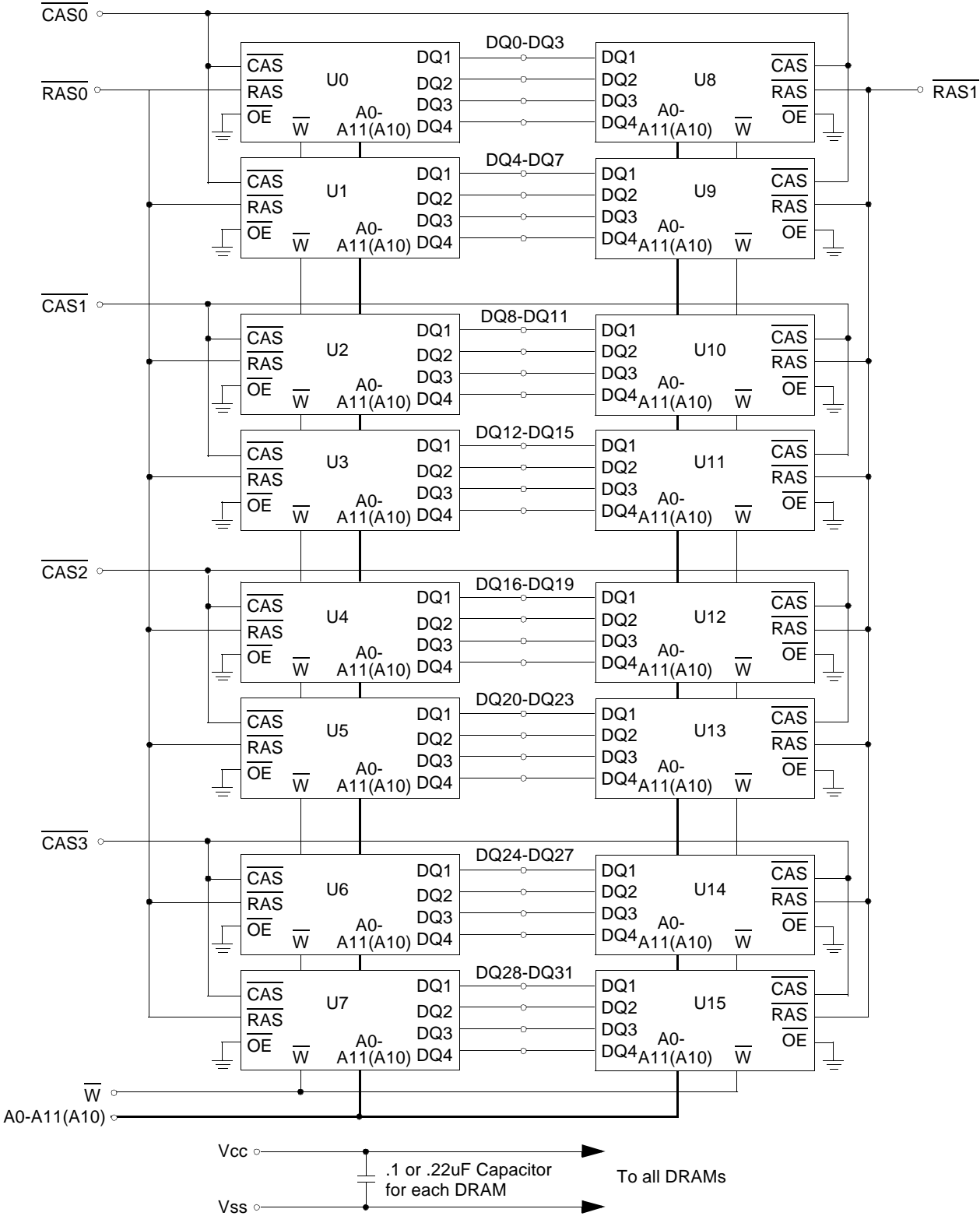
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\* NOTE : A11 is used for only M53230800CW0/CB0 (4K ref.)



DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS \*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>d</sub>	16	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> +1 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-1.0 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+2.0V/20ns, Pulse width is measured at V<sub>CC</sub>.

\*2 : -2.0V/20ns, Pulse width is measured at V<sub>SS</sub>.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53230800CW0/CB0		M53230810CW0/CB0		Unit
		Min	Max	Min	Max	
I <sub>CC1</sub>	-50	-	736	-	896	mA
	-60	-	656	-	816	mA
I <sub>CC2</sub>	Don't care	-	32	-	32	mA
I <sub>CC3</sub>	-50	-	736	-	896	mA
	-60	-	656	-	816	mA
I <sub>CC4</sub>	-50	-	656	-	736	mA
	-60	-	576	-	656	mA
I <sub>CC5</sub>	Don't care	-	16	-	16	mA
I <sub>CC6</sub>	-50	-	736	-	896	mA
	-60	-	656	-	816	mA
I <sub>I(L)</sub>	Don't care	-80	80	-80	80	uA
I <sub>O(L)</sub>	Don't care	-10	10	-10	10	uA
V <sub>OH</sub>	Don't care	2.4	-	2.4	-	V
V <sub>OL</sub>	Don't care	-	0.4	-	0.4	V

I<sub>CC1</sub> : Operating Current \* ( $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ , Address cycling @trc=min)

I<sub>CC2</sub> : Standby Current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$ )

I<sub>CC3</sub> : RAS Only Refresh Current \* ( $\overline{\text{CAS}}=\text{V}_{\text{IH}}$ ,  $\overline{\text{RAS}}$  cycling @trc=min)

I<sub>CC4</sub> : EDO Mode Current \* ( $\overline{\text{RAS}}=\text{V}_{\text{IL}}$ ,  $\overline{\text{CAS}}$  Address cycling : t<sub>HPC</sub>=min)

I<sub>CC5</sub> : Standby Current ( $\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$ )

I<sub>CC6</sub> :  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh Current \* ( $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  cycling @trc=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input  $0\leq\text{V}_{\text{IN}}\leq\text{V}_{\text{CC}}+0.5\text{V}$ , all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled,  $0\text{V}\leq\text{V}_{\text{OUT}}\leq\text{V}_{\text{CC}}$ )

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -5mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 4.2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{\text{RAS}}=\text{V}_{\text{IL}}$ . In I<sub>CC4</sub>, address can be changed maximum once within one EDO mode cycle, t<sub>HPC</sub>.



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**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC}=5\text{V}$ ,  $f = 1\text{MHz}$ )

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	100	pF
Input capacitance[W]	CIN2	-	130	pF
Input capacitance[RAS0, RAS1]	CIN3	-	70	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	30	pF
Input/Output capacitance[ $\overline{\text{DQ0-31}}$ ]	CDQ	-	20	pF

**AC CHARACTERISTICS** ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ,  $V_{CC}=5.0\text{V} \pm 10\%$ . See notes 1,2.)

Test condition :  $V_{ih}/V_{il}=2.4/0.8\text{V}$ ,  $V_{oh}/V_{ol}=2.0/0.8\text{V}$ , Output loading  $CL=100\text{pF}$

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	90		110		ns	
Access time from $\overline{\text{RAS}}$	t <sub>RAC</sub>		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t <sub>CAC</sub>		13		15	ns	3,4,5
Access time from column address	t <sub>AA</sub>		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t <sub>CLZ</sub>	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	t <sub>CEZ</sub>	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	t <sub>T</sub>	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	t <sub>RP</sub>	30		40		ns	
$\overline{\text{RAS}}$ pulse width	t <sub>RAS</sub>	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t <sub>RSH</sub>	13		15		ns	
$\overline{\text{CAS}}$ hold time	t <sub>CSH</sub>	38		45		ns	
$\overline{\text{CAS}}$ pulse width	t <sub>CAS</sub>	8	10K	10	10K	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t <sub>RCD</sub>	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	t <sub>RAD</sub>	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t <sub>CRP</sub>	5		5		ns	
Row address set-up time	t <sub>ASR</sub>	0		0		ns	
Row address hold time	t <sub>RAH</sub>	10		10		ns	
Column address set-up time	t <sub>ASC</sub>	0		0		ns	
Column address hold time	t <sub>CAH</sub>	8		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t <sub>RAL</sub>	25		30		ns	
Read command set-up time	t <sub>RCS</sub>	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t <sub>RCH</sub>	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0		0		ns	8
Write command hold time	t <sub>WCH</sub>	10		10		ns	
Write command pulse width	t <sub>WP</sub>	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t <sub>RWL</sub>	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	t <sub>CWL</sub>	8		10		ns	
Data-in set-up time	t <sub>DS</sub>	0		0		ns	9
Data-in hold time	t <sub>DH</sub>	8		10		ns	9
Refresh period (4K Ref)	t <sub>REF</sub>		64		64	ms	
Refresh period (2K Ref)	t <sub>REF</sub>		32		32	ms	
Write command set-up time	t <sub>WCS</sub>	0		0		ns	7
$\overline{\text{CAS}}$ setup time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t <sub>CSR</sub>	5		5		ns	
$\overline{\text{CAS}}$ hold time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t <sub>CHR</sub>	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t <sub>RPC</sub>	5		5		ns	



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### AC CHARACTERISTICS (0°C≤T<sub>A</sub>≤70°C, V<sub>CC</sub>=5.0V±10%. See notes 1,2.)

Test condition : V<sub>Ih</sub>/V<sub>il</sub>=2.4/0.8V, V<sub>oh</sub>/V<sub>ol</sub>=2.0/0.8V, Output loading CL=100pF

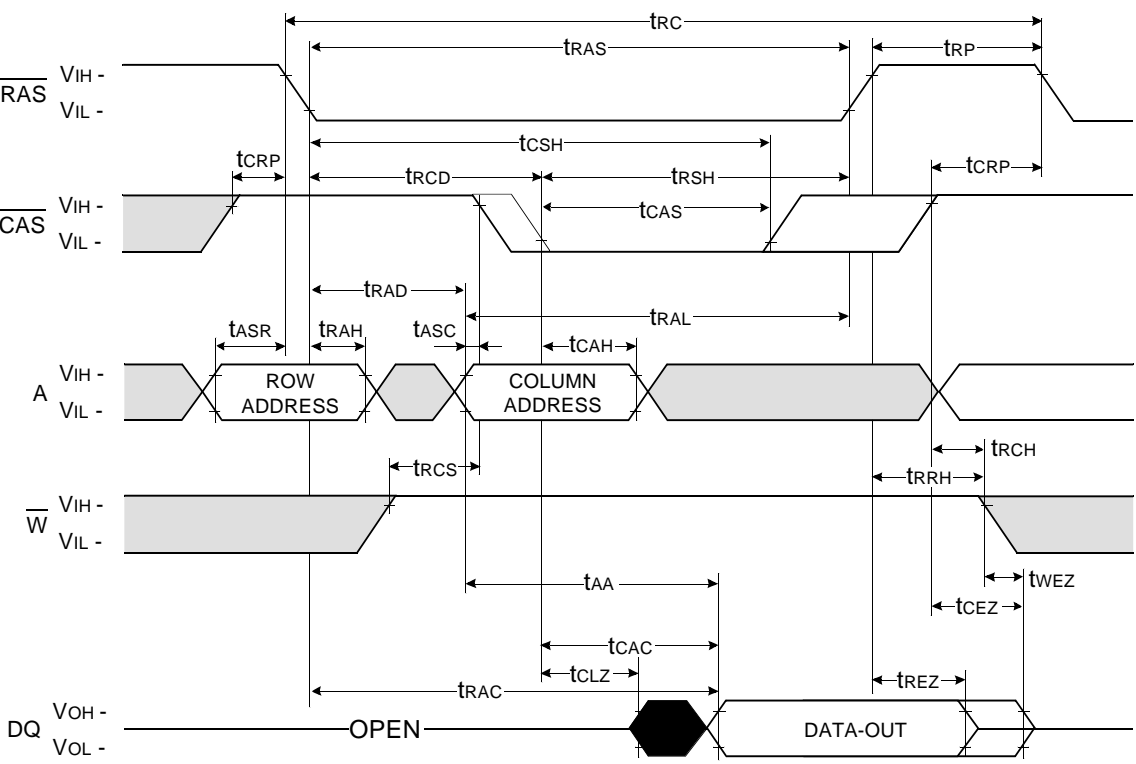
Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
CAS precharge time (C-B-R counter test cycle)	t <sub>CPT</sub>	20		20		ns	
Access time from CAS precharge	t <sub>CPA</sub>		30		35	ns	3
Hyper page mode cycle time	t <sub>HPC</sub>	25		30		ns	13
CAS precharge time(Hyper page cycle)	t <sub>CP</sub>	8		10		ns	
RAS pulse width(Hyper page cycle)	t <sub>RASP</sub>	50	200K	60	200K	ns	
RAS hold time from CAS precharge	t <sub>RHCP</sub>	30		35		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	t <sub>WRP</sub>	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	t <sub>WRH</sub>	10		10		ns	
Output data hold time	t <sub>DOH</sub>	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t <sub>REZ</sub>	3	13	3	15	ns	7,11,12
Output buffer turn off delay from $\overline{W}$	t <sub>WEZ</sub>	3	13	3	15	ns	7,11
$\overline{W}$ to data delay	t <sub>WED</sub>	15		15		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t <sub>WPE</sub>	5		5		ns	

### NOTES

- An initial pause of 200us is required after power-up followed by any 8  $\overline{RAS}$ -only or  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles before proper device operation is achieved.
- V<sub>IH</sub>(min) and V<sub>IL</sub>(max) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub>(min) and V<sub>IL</sub>(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the t<sub>RCd</sub>(max) limit insures that t<sub>RC</sub>(max) can be met. t<sub>RCd</sub>(max) is specified as a reference point only. If t<sub>RCd</sub> is greater than the specified t<sub>RCd</sub>(max) limit, then access time is controlled exclusively by t<sub>CAC</sub>.
- Assumes that t<sub>RCd</sub>≥t<sub>RCd</sub>(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
- t<sub>WCS</sub> is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If t<sub>WCS</sub>≥t<sub>WCS</sub>(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t<sub>TRC</sub> or t<sub>TRH</sub> must be satisfied for a read cycle.
- These parameter are referenced to the  $\overline{CAS}$  leading edge in early write cycles and to the  $\overline{W}$  leading edge in read-write cycles.
- Operation within the t<sub>RAD</sub>(max) limit insures that t<sub>RC</sub>(max) can be met. t<sub>RAD</sub>(max) is specified as reference point only. If t<sub>RAD</sub> is greater than the specified t<sub>RAD</sub>(max) limit, then access time is controlled by t<sub>AA</sub>.
- t<sub>CEZ</sub>(max), t<sub>REZ</sub>(max), t<sub>WEZ</sub>(max) and t<sub>OEZ</sub>(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- If  $\overline{RAS}$  goes to high before  $\overline{CAS}$  high going, the open circuit condition of the output is achieved by  $\overline{CAS}$  high going. If  $\overline{CAS}$  goes to high before  $\overline{RAS}$  high going, the open circuit condition of the output is achieved by  $\overline{RAS}$  high going.
- t<sub>ASC</sub>≥t<sub>CP</sub> min

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READ CYCLE



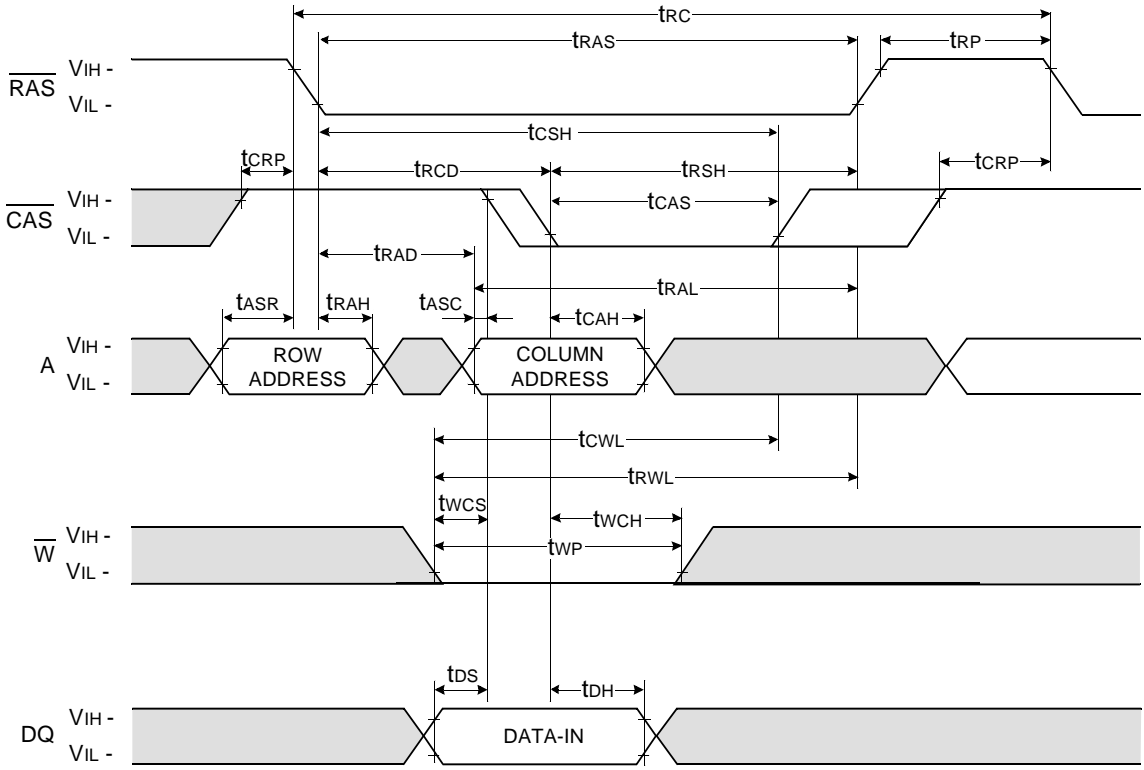
□ Don't care  
■ Undefined



**DRAM MODULE**

**WRITE CYCLE ( EARLY WRITE )**

NOTE : DOUT = OPEN

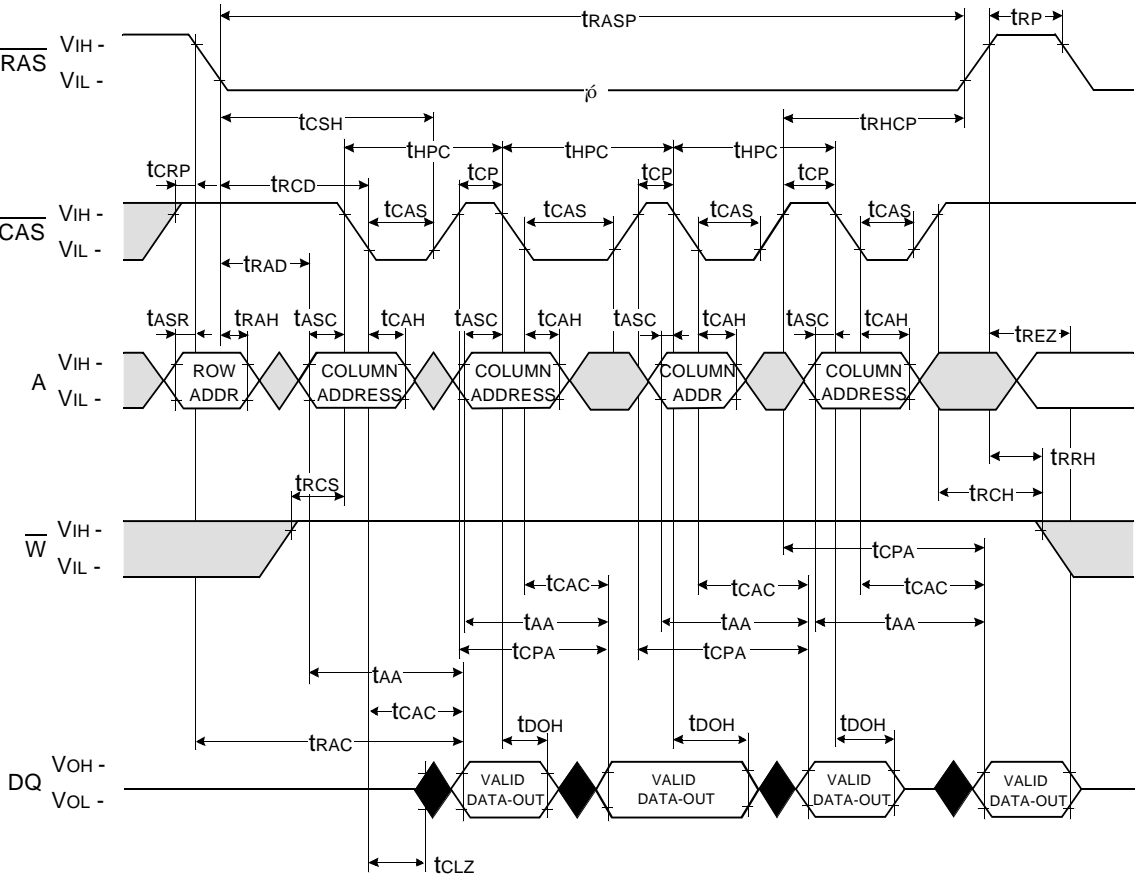


Don't care  
 Undefined



DRAM MODULE

HYPER PAGE READ CYCLE



□ Don't care  
■ Undefined

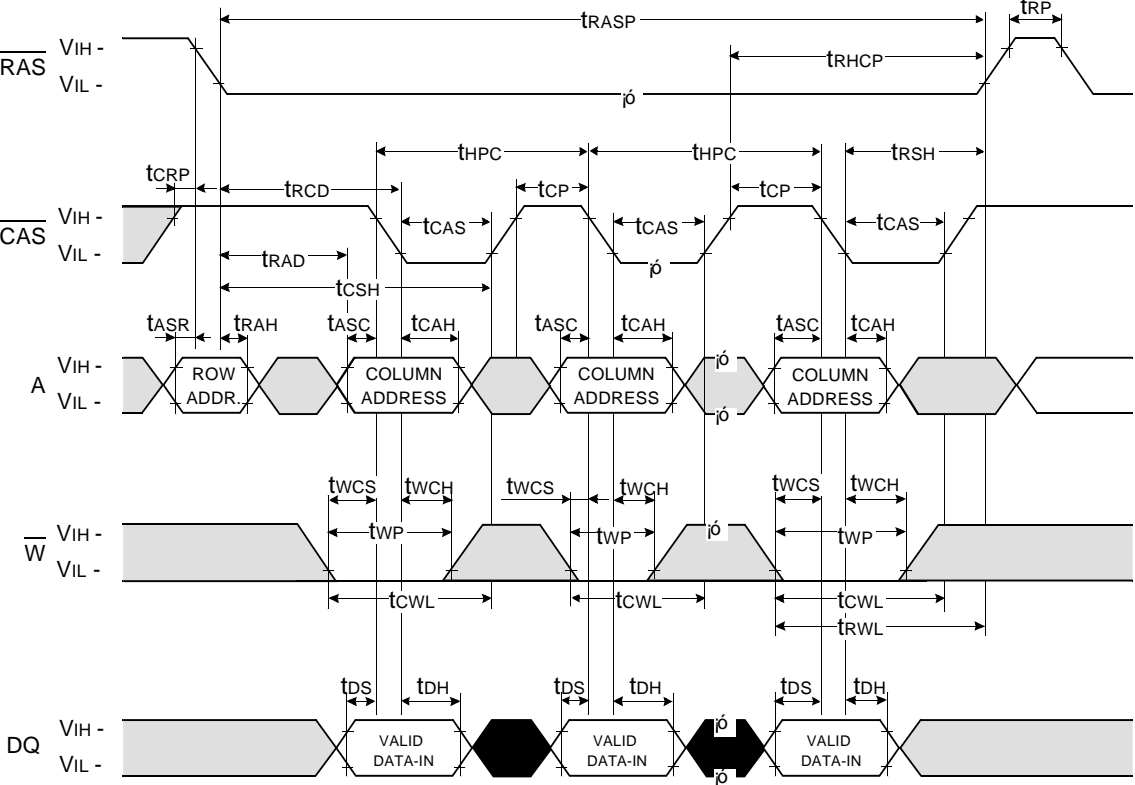




DRAM MODULE

HYPER PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



□ Don't care  
■ Undefined



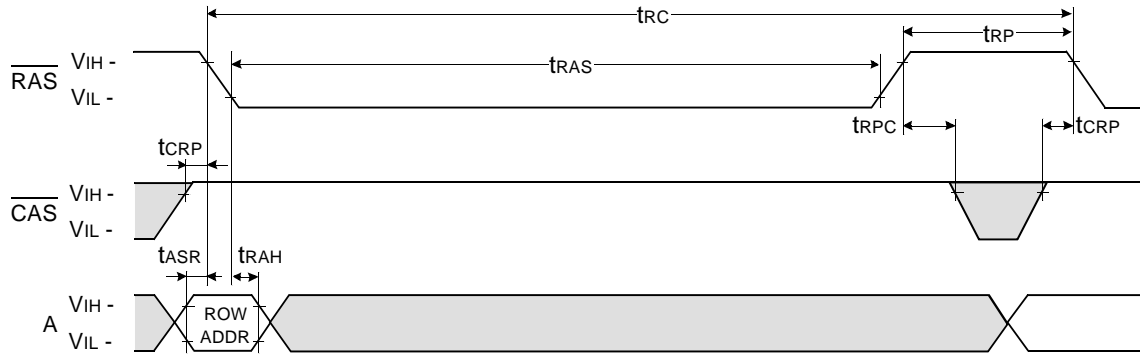
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**DRAM MODULE**

**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE\***

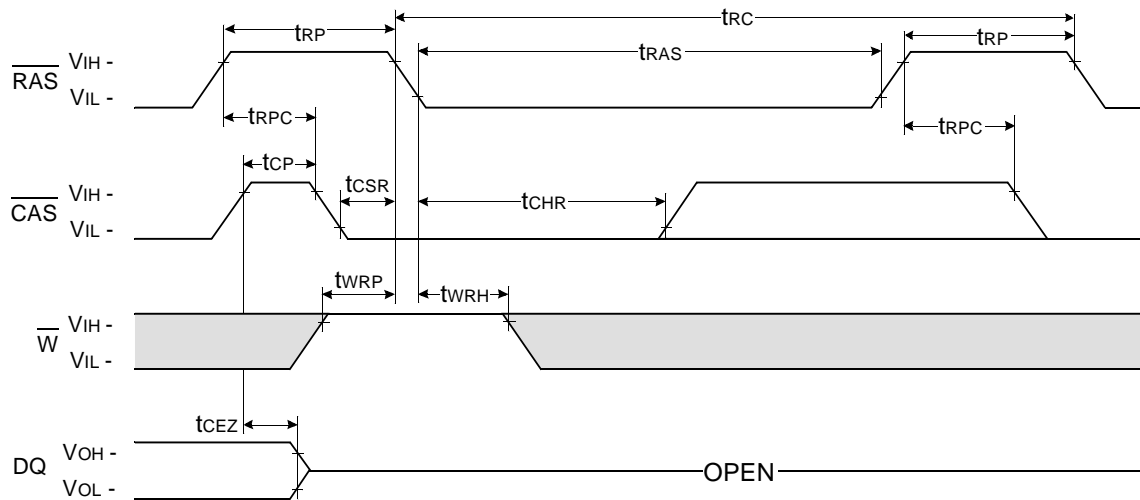
NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ , DIN = Don't care

DOUT = OPEN



**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

NOTE :  $\overline{\text{OE}}$ , A = Don't care



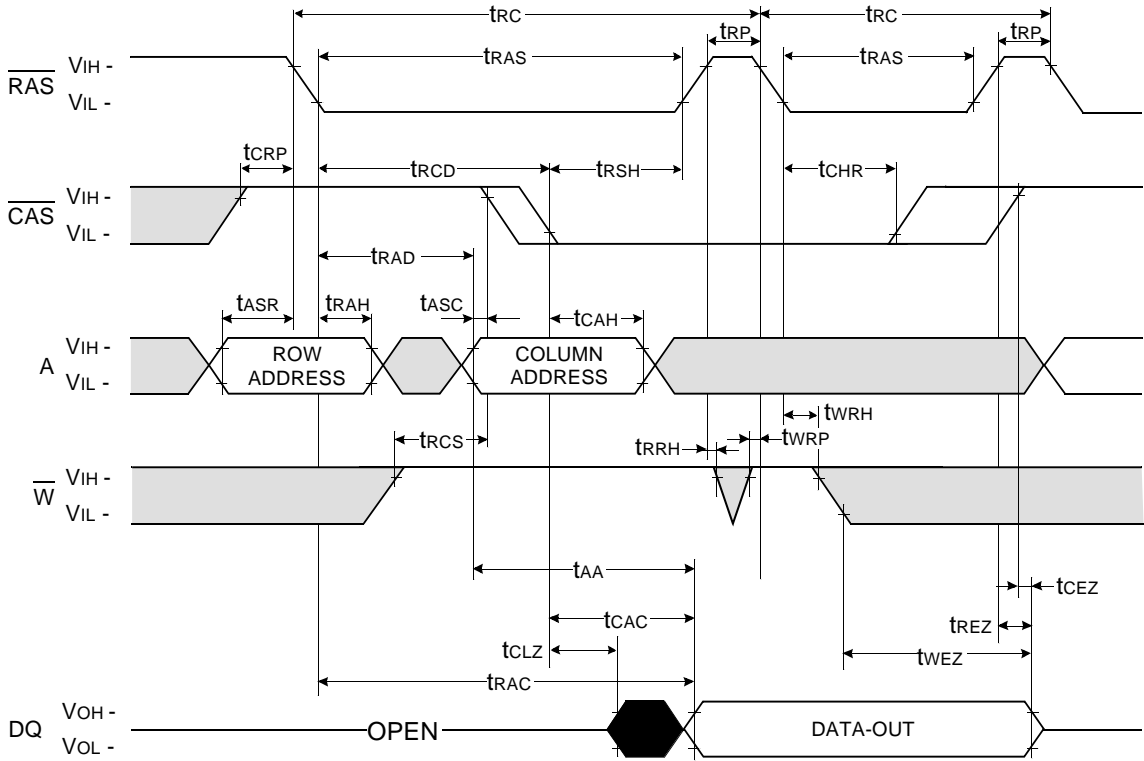
□ Don't care  
■ Undefined

\* In  $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when  $\overline{\text{CAS}}$  signal transits from Low to High, the valid data may be cut off.



DRAM MODULE

HIDDEN REFRESH CYCLE ( READ )



□ Don't care  
■ Undefined

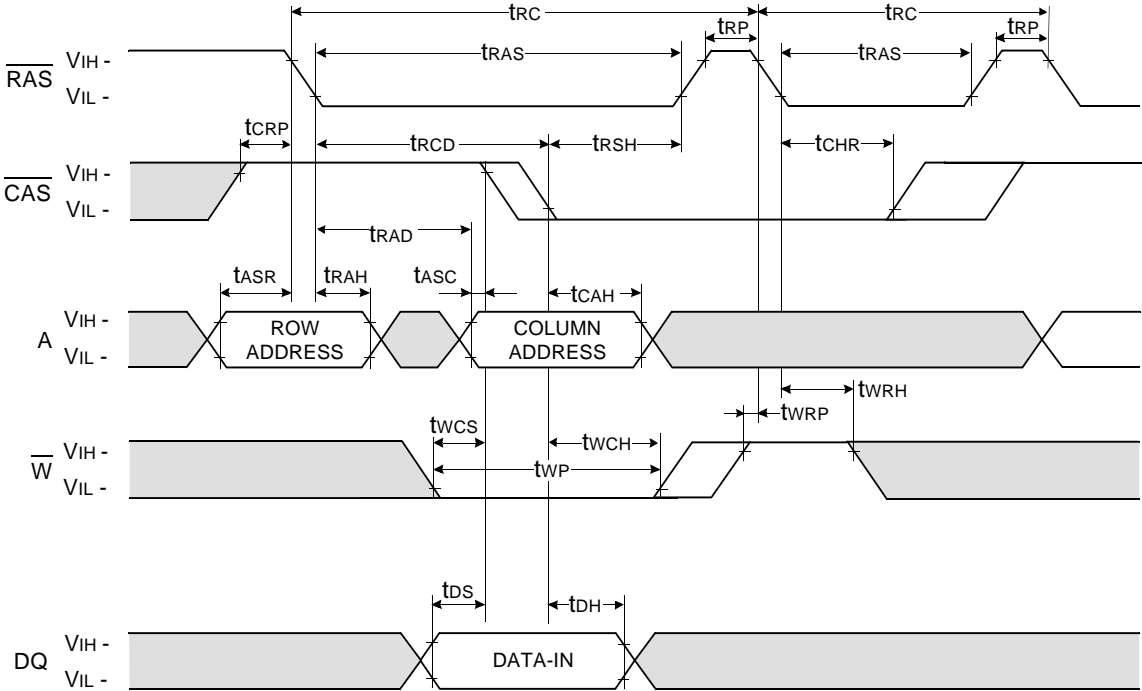


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**DRAM MODULE**

**HIDDEN REFRESH CYCLE ( WRITE )**

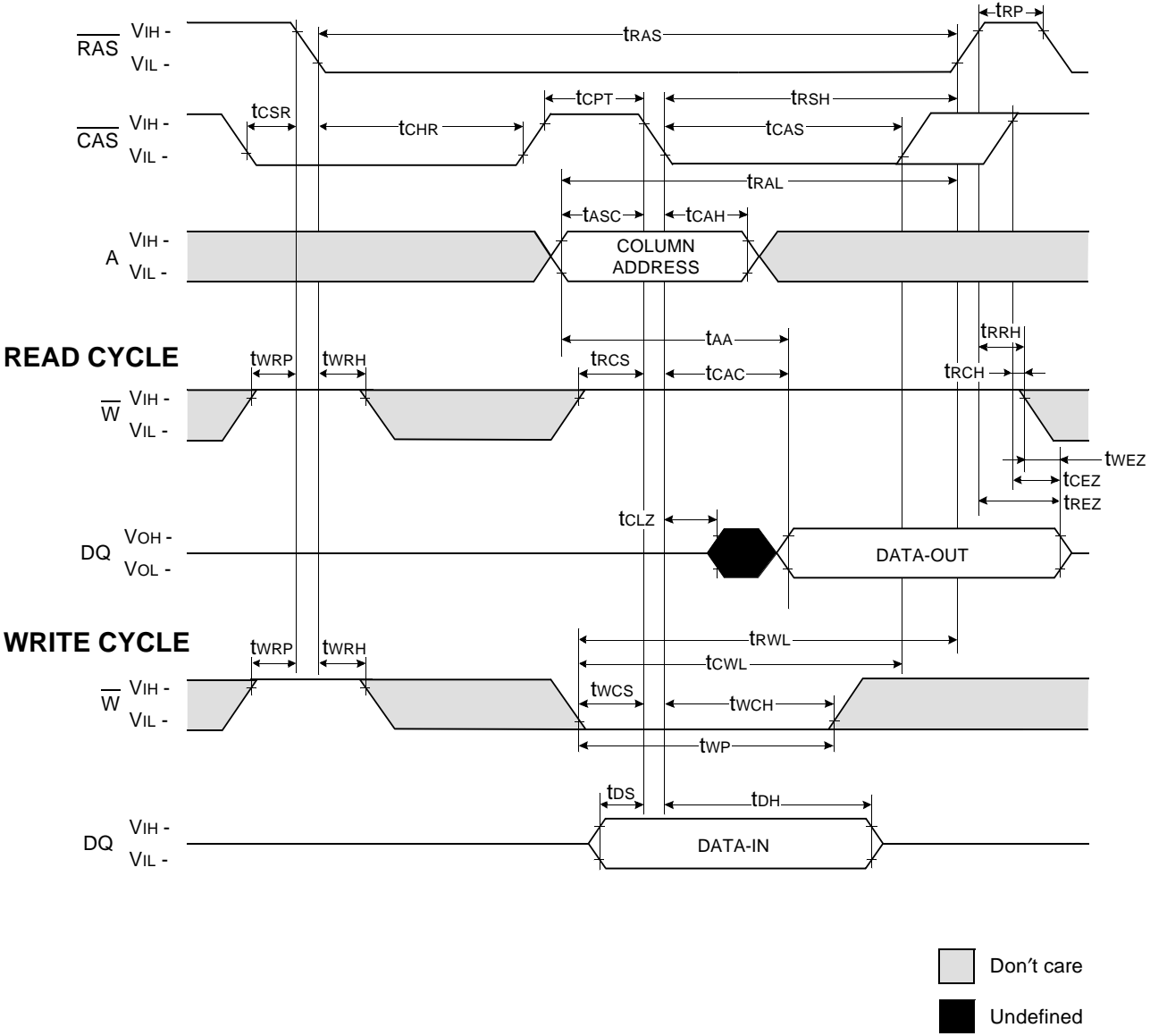
NOTE : DOUT = OPEN



Don't care  
 Undefined

DRAM MODULE

CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



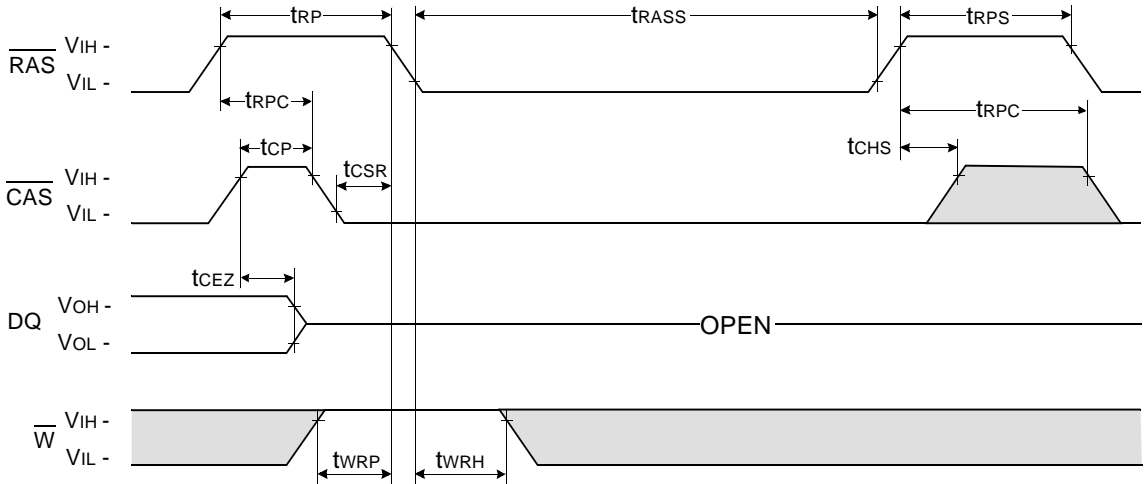
NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.



**DRAM MODULE**

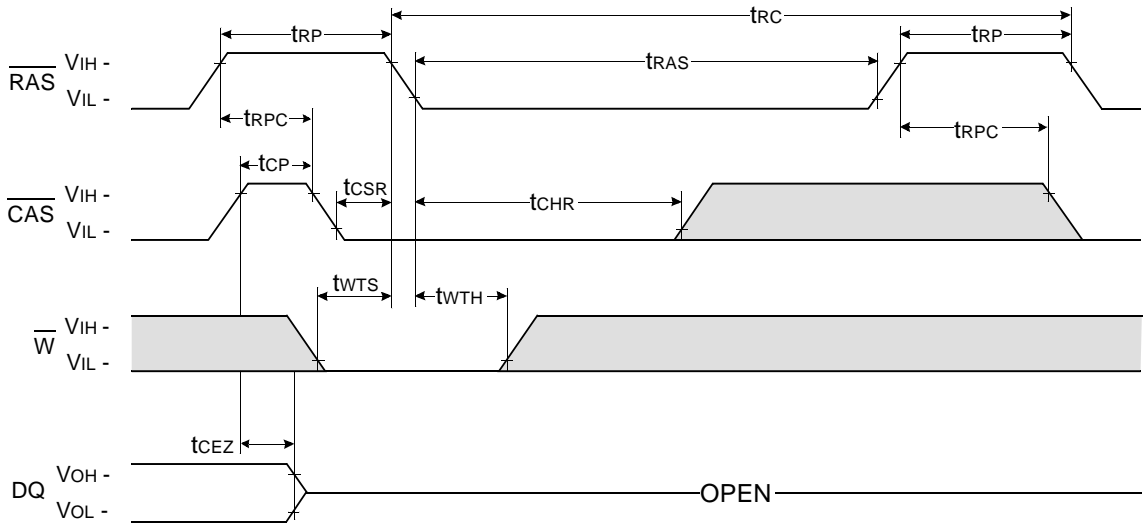
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



□ Don't care  
■ Undefined



