

DRAM MODULE

M53231600CE0/CJ0-C

4Byte 16Mx32 SIMM

(16Mx4 base)

Revision 0.0

June 1999

DRAM MODULE

M53231600CE0/CJ0-C

Revision History

Version 0.0 (June 1999)

- The 4th. generation of 64Mb DRAM components are applied for this module.

DRAM MODULE

M53231600CE0/CJ0-C

M53231600CE0/CJ0-C EDO Mode

16M x 32 DRAM SIMM Using 16Mx4, 4K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M53231600CE0/CJ0-C is a 16Mx32bits Dynamic RAM high density memory module. The Samsung M53231600CE0/CJ0-C consists of eight CMOS 16Mx4bits DRAMs in SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M53231600CE0/CJ0-C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

| Speed | tRAC | tCAC | tRC | tHPC |
|-------|------|------|-------|------|
| -C50 | 50ns | 13ns | 84ns | 20ns |
| -C60 | 60ns | 15ns | 104ns | 25ns |

FEATURES

- Part Identification
 - M53231600CE0-C(4K cycles/64ms Ref, SOJ, Solder)
 - M53231600CJ0-C(4K cycles/64ms Ref, SOJ, Gold)
- Extended Data Out Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ & Hidden Refresh capability
- $\overline{\text{RAS}}$ -only refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDpin & pinout
- PCB : Height(1250mil), double sided component

PIN CONFIGURATIONS

| Pin | Symbol | Pin | Symbol |
|-----|--------------------------|-----|--------------------------|
| 1 | Vss | 37 | NC |
| 2 | DQ0 | 38 | NC |
| 3 | DQ18 | 39 | $\overline{\text{Vss}}$ |
| 4 | DQ1 | 40 | $\overline{\text{CAS0}}$ |
| 5 | DQ19 | 41 | $\overline{\text{CAS2}}$ |
| 6 | DQ2 | 42 | $\overline{\text{CAS3}}$ |
| 7 | DQ20 | 43 | $\overline{\text{CAS1}}$ |
| 8 | DQ3 | 44 | $\overline{\text{RAS0}}$ |
| 9 | DQ21 | 45 | NC |
| 10 | Vcc | 46 | NC |
| 11 | NC | 47 | W |
| 12 | A0 | 48 | NC |
| 13 | A1 | 49 | DQ9 |
| 14 | A2 | 50 | DQ27 |
| 15 | A3 | 51 | DQ10 |
| 16 | A4 | 52 | DQ28 |
| 17 | A5 | 53 | DQ11 |
| 18 | A6 | 54 | DQ29 |
| 19 | A10 | 55 | DQ12 |
| 20 | DQ4 | 56 | DQ30 |
| 21 | DQ22 | 57 | DQ13 |
| 22 | DQ5 | 58 | DQ31 |
| 23 | DQ23 | 59 | Vcc |
| 24 | DQ6 | 60 | DQ32 |
| 25 | DQ24 | 61 | DQ14 |
| 26 | DQ7 | 62 | DQ33 |
| 27 | DQ25 | 63 | DQ15 |
| 28 | A7 | 64 | DQ34 |
| 29 | A11 | 65 | DQ16 |
| 30 | Vcc | 66 | NC |
| 31 | A8 | 67 | PD1 |
| 32 | A9 | 68 | PD2 |
| 33 | NC | 69 | PD3 |
| 34 | $\overline{\text{RAS2}}$ | 70 | PD4 |
| 35 | NC | 71 | NC |
| 36 | NC | 72 | Vss |

PIN NAMES

| Pin Name | Function |
|---|-----------------------|
| A0 - A11 | Address Inputs |
| DQ0-7, DQ9-16 DQ18-25, DQ27-34 | Data In/Out |
| $\overline{\text{W}}$ | Read/Write Enable |
| $\overline{\text{RAS0}}, \overline{\text{RAS2}}$ | Row Address Strobe |
| $\overline{\text{CAS0}} - \overline{\text{CAS3}}$ | Column Address Strobe |
| PD1 -PD4 | Presence Detect |
| Vcc | Power(+5V) |
| Vss | Ground |
| NC | No Connection |

PRESENCE DETECT PINS (Optional)

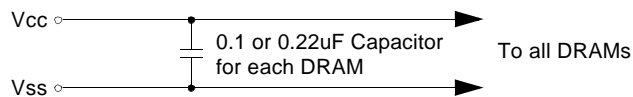
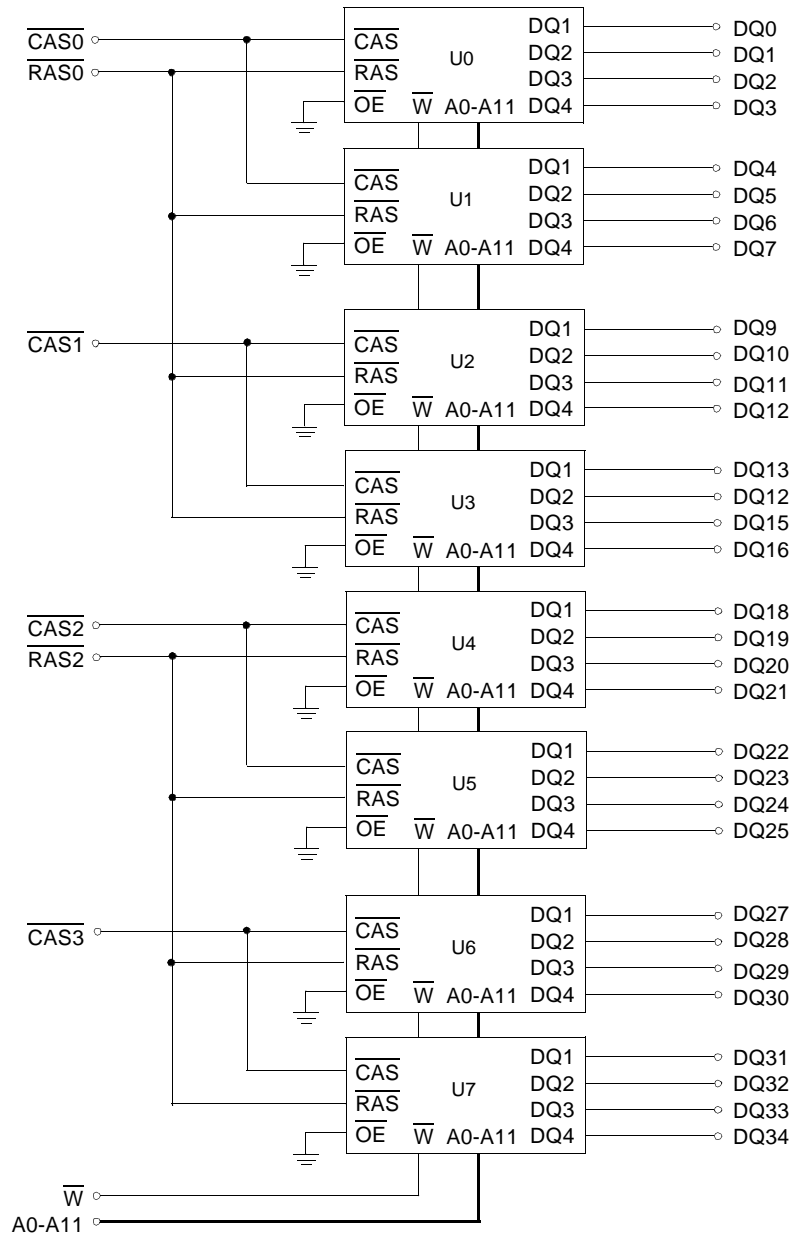
| Pin | 50NS | 60NS |
|-----|------|------|
| PD1 | Vss | Vss |
| PD2 | NC | NC |
| PD3 | Vss | NC |
| PD4 | Vss | NC |

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DRAM MODULE

M53231600CE0/CJ0-C

FUNCTIONAL BLOCK DIAGRAM



DRAM MODULE

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ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---------------------------------------|------------------------------------|-------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1 to +7.0 | V |
| Voltage on Vcc supply relative to Vss | V _{CC} | -1 to +7.0 | V |
| Storage Temperature | T _{stg} | -55 to +125 | °C |
| Power Dissipation | P _d | 8 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------|-----|--------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | V _{CC} *1 | V |
| Input Low Voltage | V _{IL} | -1.0*2 | - | 0.8 | V |

*1 : V_{CC}+2.0V at pulse width≤20ns, which is measured at V_{CC}.

*2 : -2.0V at pulse width≤20ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speed | M53231600CE0/CJ0 | | Unit |
|-------------------|------------|------------------|-----|------|
| | | Min | Max | |
| I _{CC1} | -50 | - | 960 | mA |
| | -60 | - | 880 | mA |
| I _{CC2} | Don't care | - | 16 | mA |
| I _{CC3} | -50 | - | 960 | mA |
| | -60 | - | 880 | mA |
| I _{CC4} | -50 | - | 880 | mA |
| | -60 | - | 800 | mA |
| I _{CC5} | Don't care | - | 8 | mA |
| I _{CC6} | -50 | - | 960 | mA |
| | -60 | - | 880 | mA |
| I _{I(L)} | Don't care | -10 | 10 | uA |
| I _{O(L)} | | -5 | 5 | uA |
| V _{OH} | Don't care | 2.4 | - | V |
| V _{OL} | | - | 0.4 | V |

I_{CC1} : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3} : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

I_{CC4} : Hyper Page Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6} : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.5V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

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CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Input capacitance[A0-A11] | CIN1 | - | 50 | pF |
| Input capacitance[W] | CIN2 | - | 66 | pF |
| Input capacitance[RAS0, RAS2] | CIN3 | - | 38 | pF |
| Input capacitance[CAS0 - CAS3] | CIN4 | - | 24 | pF |
| Input/Output capacitance[DQ0-7, 9-16,18-25, 27-34] | CDQ | - | 17 | pF |

AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

| Parameter | Symbol | -50 | | -60 | | Unit | Note |
|---|--------|-----|-----|-----|-----|------|--------|
| | | Min | ax | Min | Max | | |
| Random read or write cycle time | tRC | 84 | | 104 | | ns | |
| Access time from RAS | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from CAS | tCAC | | 13 | | 15 | ns | 3,4,5 |
| Access time from column address | tAA | | 25 | | 30 | ns | 3,10 |
| CAS to output in Low-Z | tCLZ | 3 | | 3 | | ns | 3 |
| Output buffer turn-off delay from CAS | tCEZ | 3 | 13 | 3 | 13 | ns | 6,12 |
| Transition time(rise and fall) | tr | 1 | 50 | 1 | 50 | ns | 2 |
| RAS precharge time | tRP | 30 | | 40 | | ns | |
| RAS pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| RAS hold time | tRSH | 13 | | 15 | | ns | |
| CAS hold time | tCSH | 38 | | 45 | | ns | |
| CAS pulse width | tCAS | 8 | 10K | 10 | 10K | ns | 4 |
| RAS to CAS delay time | tRCD | 20 | 37 | 20 | 45 | ns | 9 |
| RAS to column address delay time | tRAD | 15 | 25 | 15 | 30 | ns | |
| CAS to RAS precharge time | tCRP | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 8 | | 10 | | ns | |
| Column address to RAS lead time | tRAL | 25 | | 30 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referenced to CAS | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to RAS | tRRH | 0 | | 0 | | ns | 8 |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| Write command hold time | tWCH | 10 | | 10 | | ns | |
| Write command pulse width | tWP | 10 | | 10 | | ns | |
| Write command to RAS lead time | tRWL | 13 | | 15 | | ns | |
| Write command to CAS lead time | tCWL | 8 | | 10 | | ns | |
| Data set-up time | tDS | 0 | | 0 | | ns | 9 |
| Data hold time | tDH | 8 | | 10 | | ns | 9 |
| Refresh period | tREF | | 64 | | 64 | ms | |
| CAS setup time (CAS-before-RAS refresh) | tCSR | 5 | | 5 | | ns | |
| CAS hold time (CAS-before-RAS refresh) | tCHR | 10 | | 10 | | ns | |
| RAS to CAS precharge time | tRPC | 5 | | 5 | | ns | |
| Access time from CAS precharge | tCPA | | 28 | | 35 | ns | 3 |

DRAM MODULE

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AC CHARACTERISTICS (0°C≤TA≤70°C, Vcc=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

| Parameter | Symbol | -50 | | -60 | | Unit | Note |
|---|--------|-----|------|-----|------|------|------|
| | | Min | Max | Min | Max | | |
| Hyper page mode cycle time | tHPC | 20 | | 25 | | ns | 11 |
| CAS precharge time (Hyper page cycle) | tCP | 8 | | 10 | | ns | |
| RAS pulse width (Hyper page cycle) | tRASP | 50 | 200K | 60 | 200K | ns | |
| RAS hold time from CAS precharge | tRHCP | 30 | | 35 | | ns | |
| \overline{W} to RAS precharge time(C-B-R refresh) | tWRP | 10 | | 10 | | ns | |
| \overline{W} to RAS hold time(C-B-R refresh) | tWRH | 10 | | 10 | | ns | |
| Output data hold time | tDOH | 5 | | 5 | | ns | |
| Output buffer turn off delay from \overline{RAS} | tREZ | 3 | 13 | 3 | 15 | ns | 6,12 |
| Output buffer turn off delay from \overline{W} | tWEZ | 3 | 13 | 3 | 15 | ns | 6 |
| \overline{W} to data delay | tWED | 15 | | 15 | | ns | |
| \overline{W} pulse width | tWPE | 5 | | 5 | | ns | |

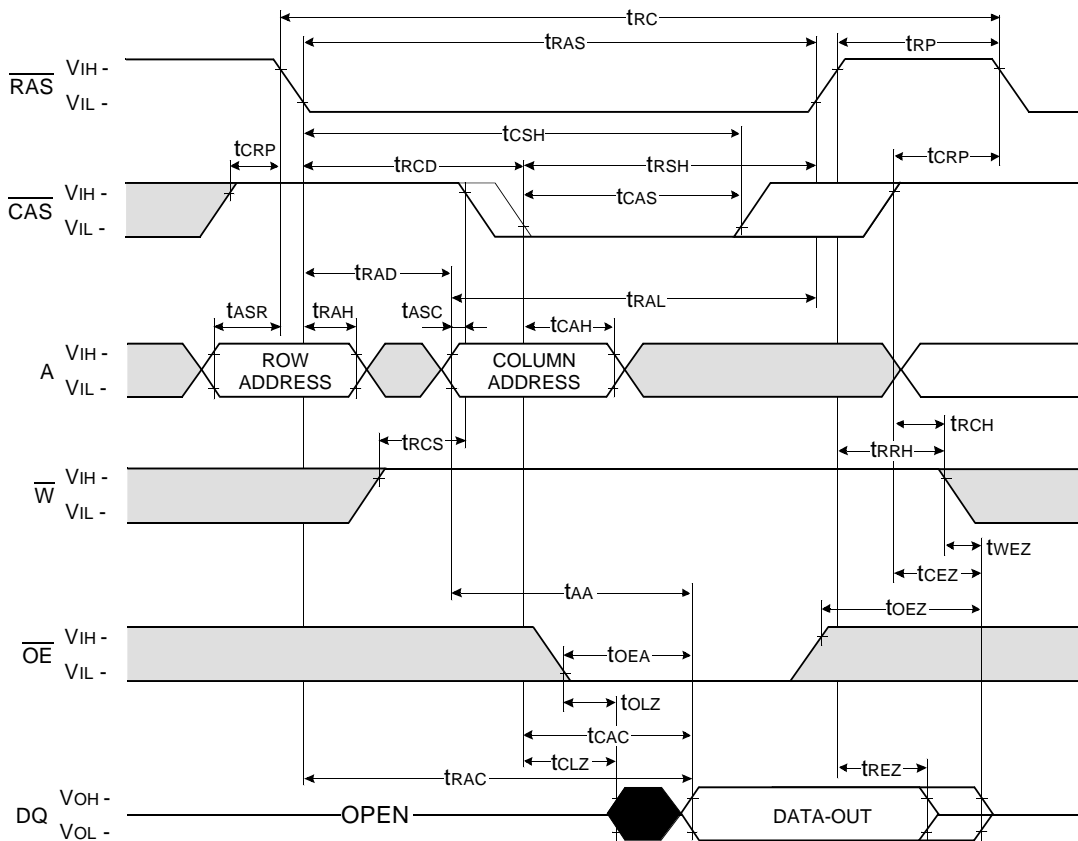
NOTES

- An initial pause of 200us is required after power-up followed by any 8 RAS-only or \overline{CAS} -before-RAS refresh cycles before proper device operation is achieved.
- Input voltage levels are Vih/Vil. VIH(min) and VIL(max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
- Assumes that tRCD≥tRCD(max).
- This parameter defines the time at which the output achieves the open circuit and is not referenced for VOH or VOL.
- twcs is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either tRCH or tRRH must be satisfied for a read cycle.
- These parameters are referenced to the \overline{CAS} leading edge in early write cycles.
- Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD(max) limit access time is controlled by tAA.
- tASC≥6ns, Assume tT=2.0ns.
- If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes high before RAS high going, the open circuit condition of the output is achieved by RAS going.

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READ CYCLE

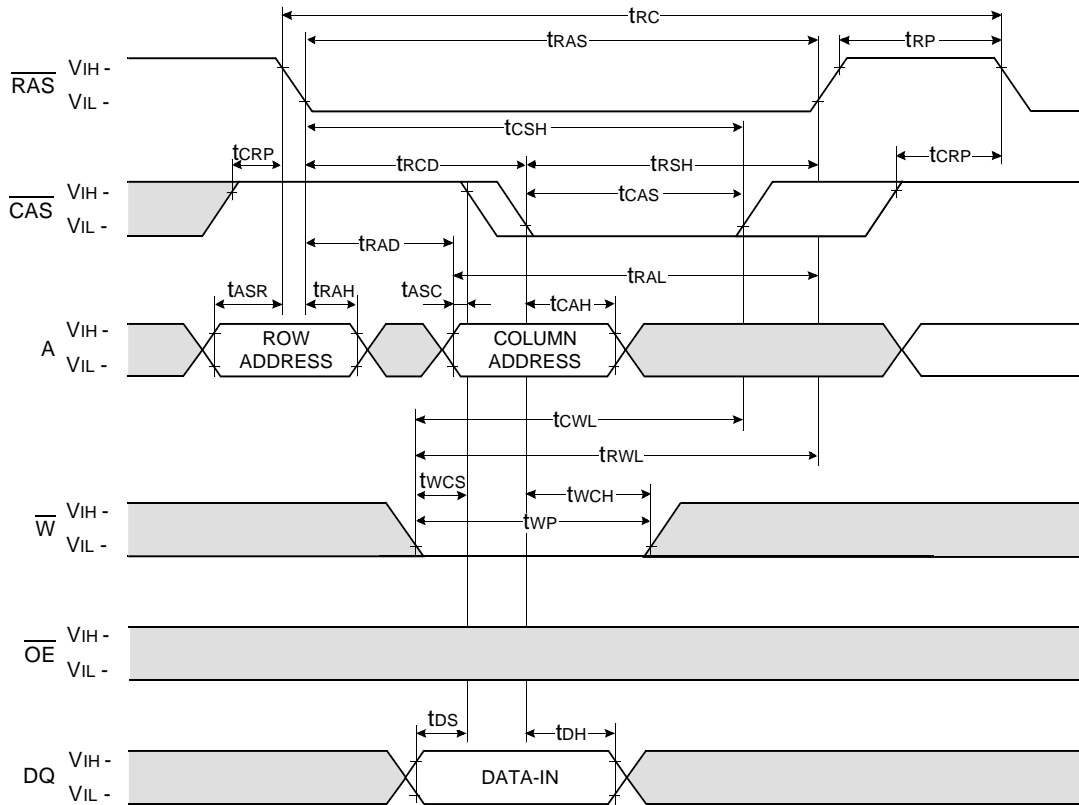


DRAM MODULE

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WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



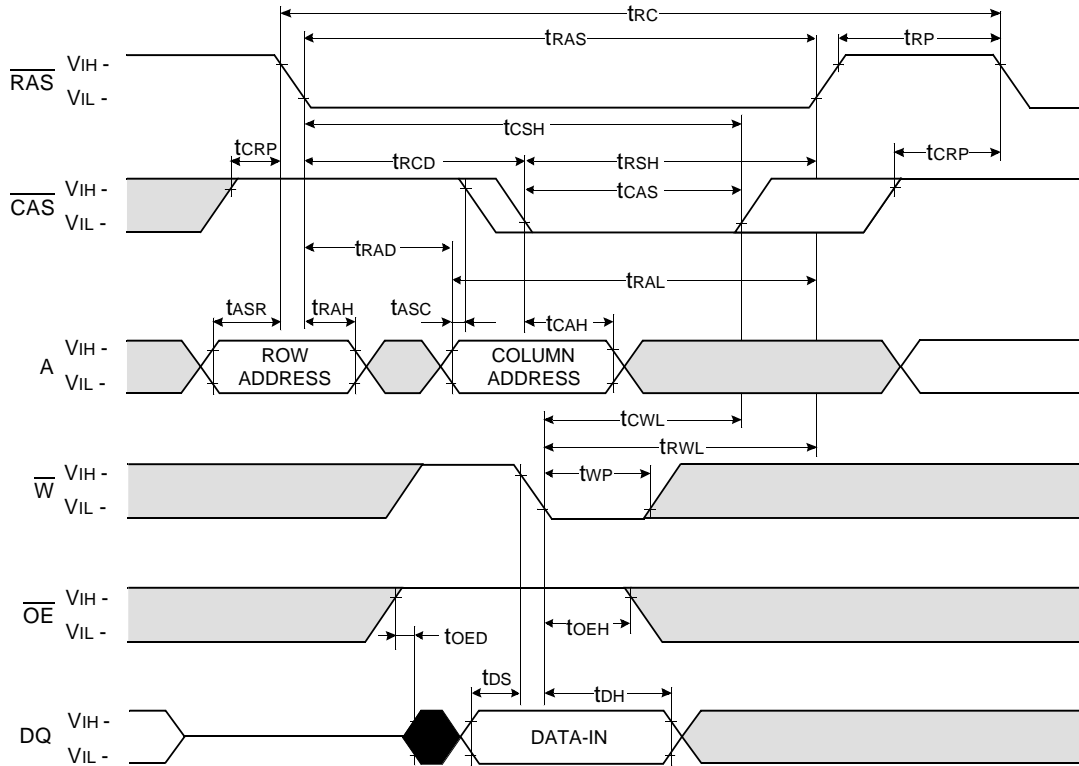
□ Don't care
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DRAM MODULE

M53231600CE0/CJ0-C

WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN

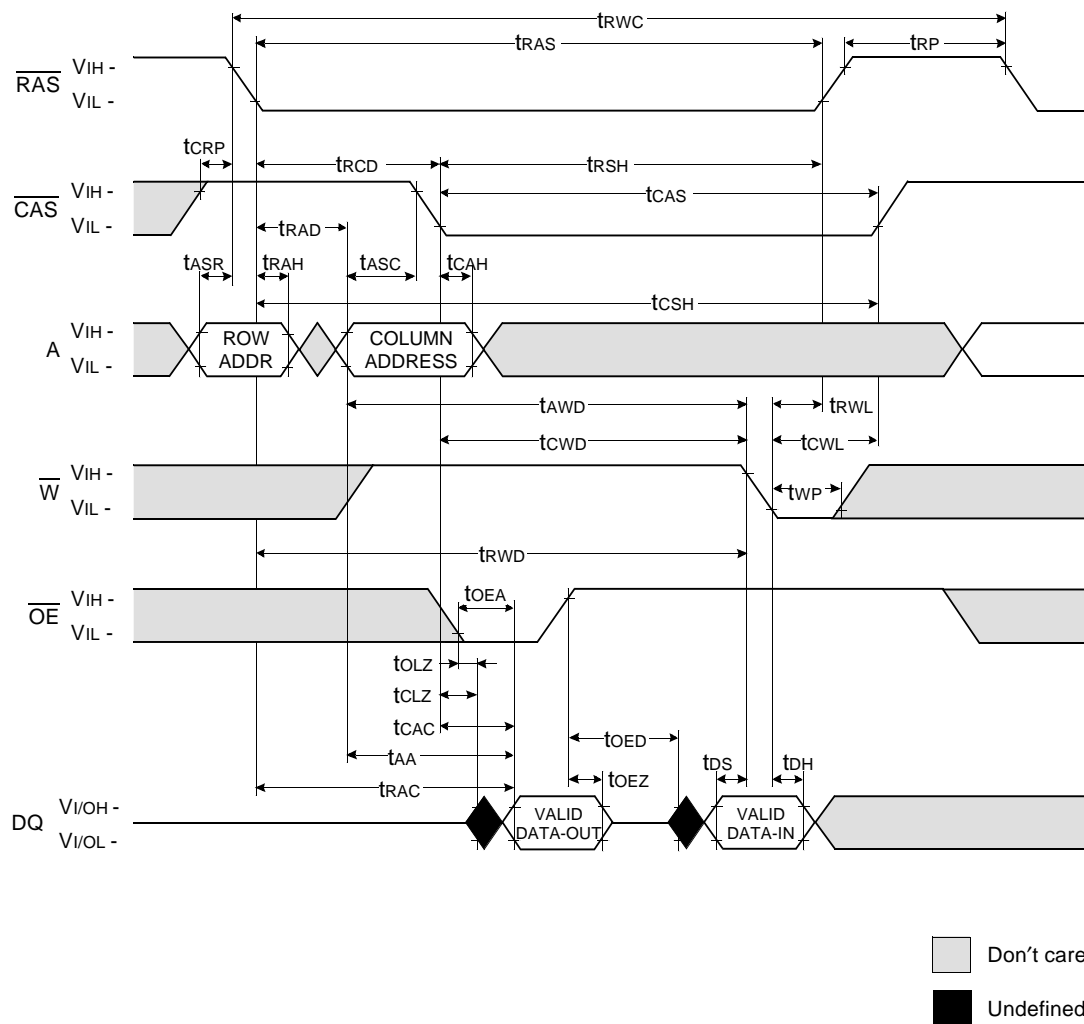


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DRAM MODULE

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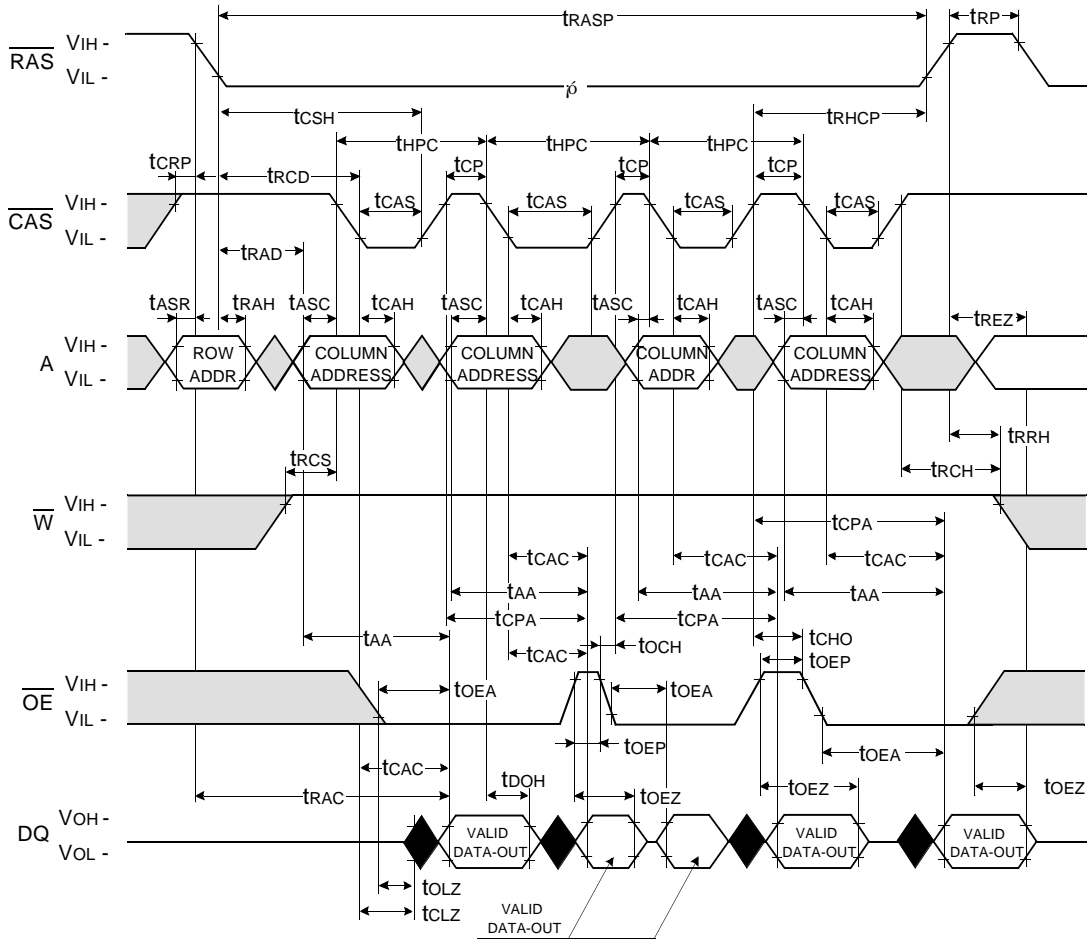
READ - MODIFY - WRITE CYCLE



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HYPER PAGE READ CYCLE



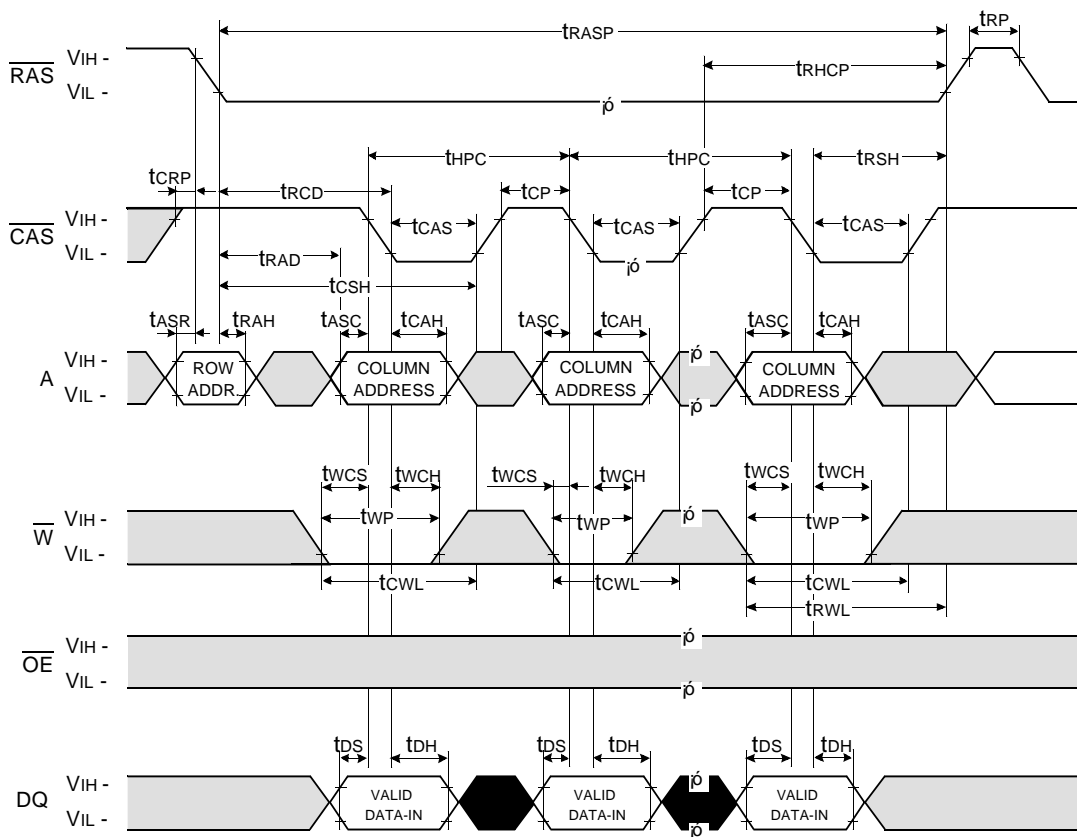
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DRAM MODULE

M53231600CE0/CJ0-C

HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

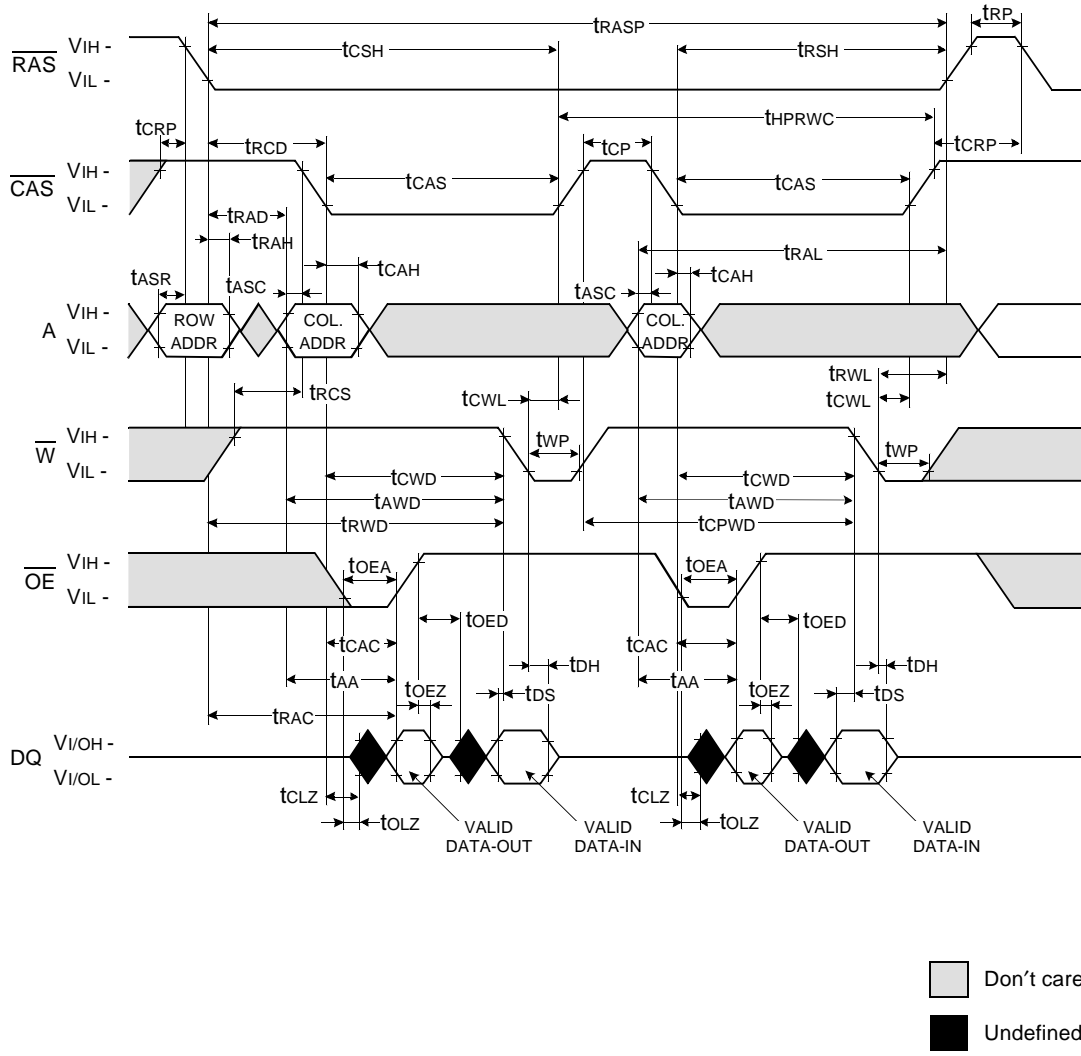


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DRAM MODULE

M53231600CE0/CJ0-C

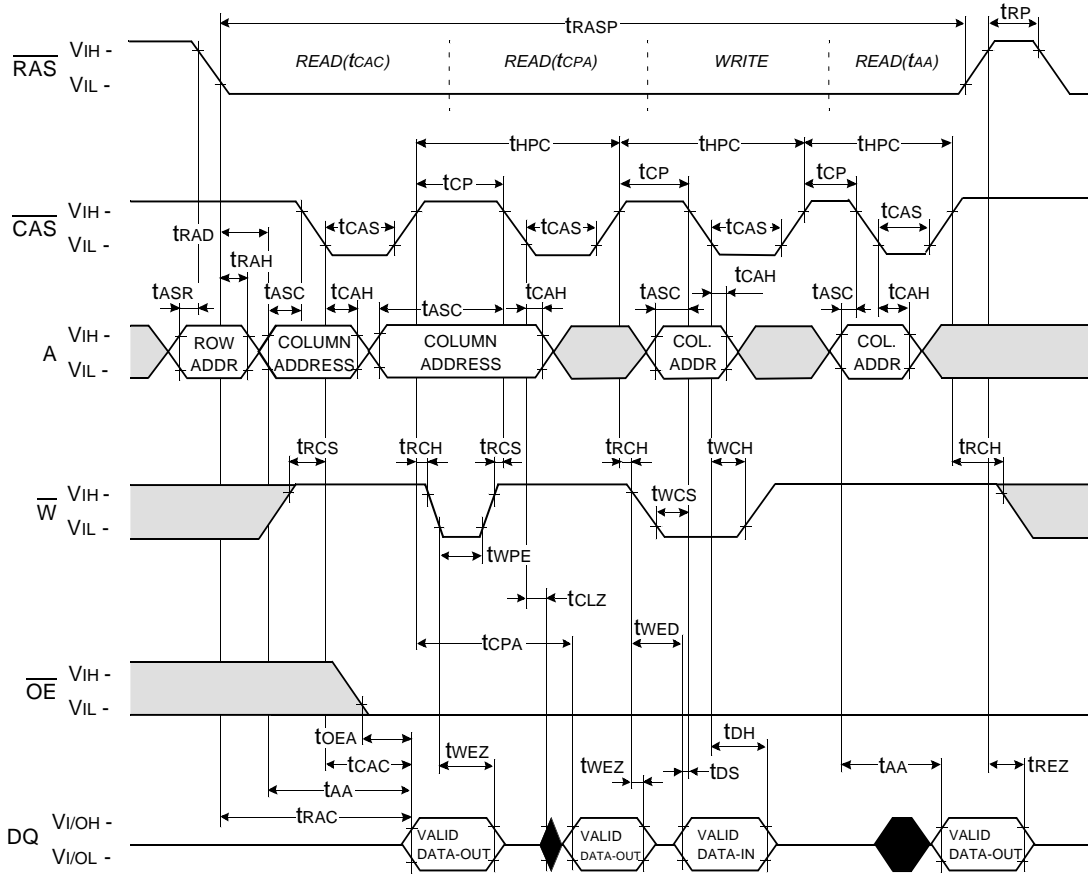
HYPER PAGE READ-MODIFY-WRITE CYCLE





DRAM MODULE

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HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't care
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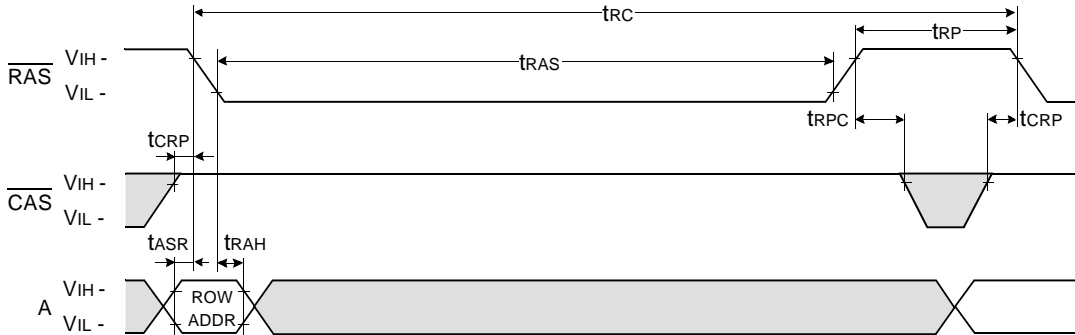
DRAM MODULE

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RAS - ONLY REFRESH CYCLE*

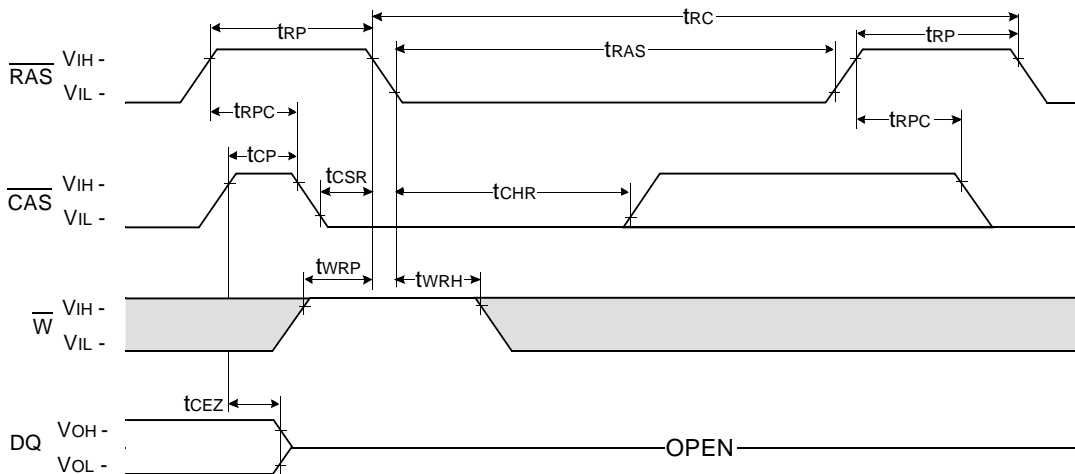
NOTE : \overline{W} , \overline{OE} , DIN = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



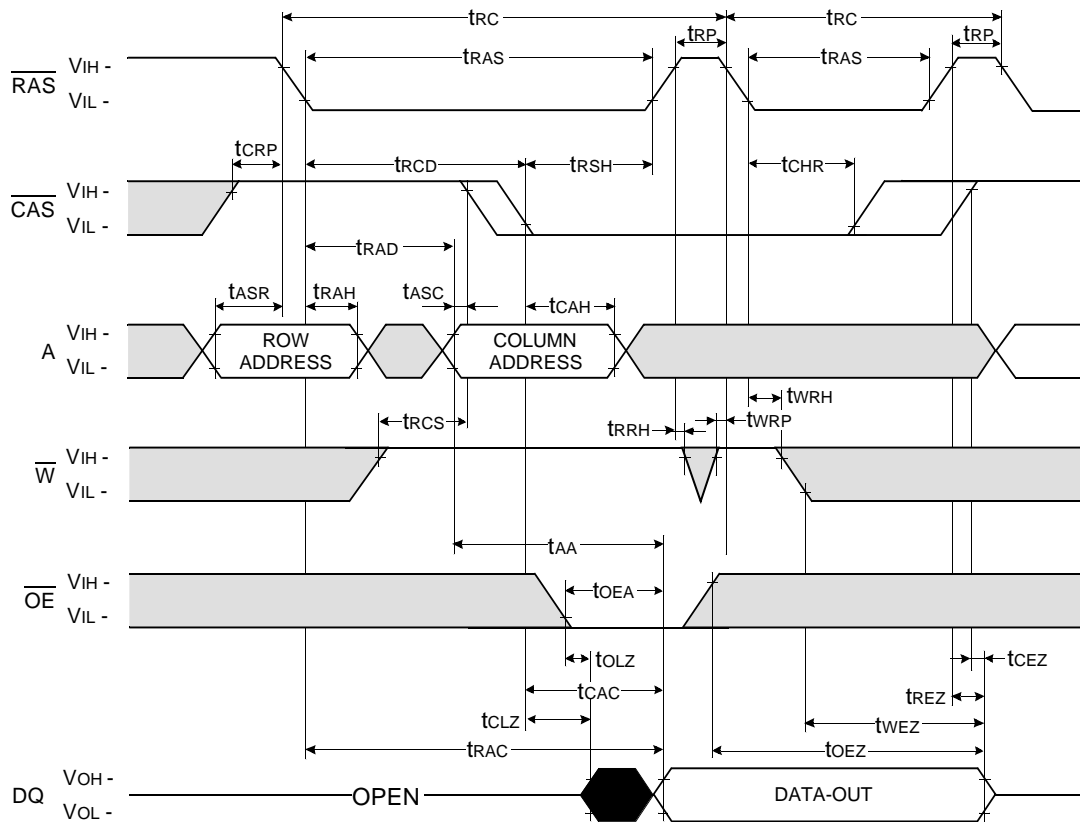
Don't care
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* In RAS-only refresh cycle of 64Mb A-die & B-die, when \overline{CAS} signal transits from Low to High, the valid data may be cut off.

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HIDDEN REFRESH CYCLE (READ)



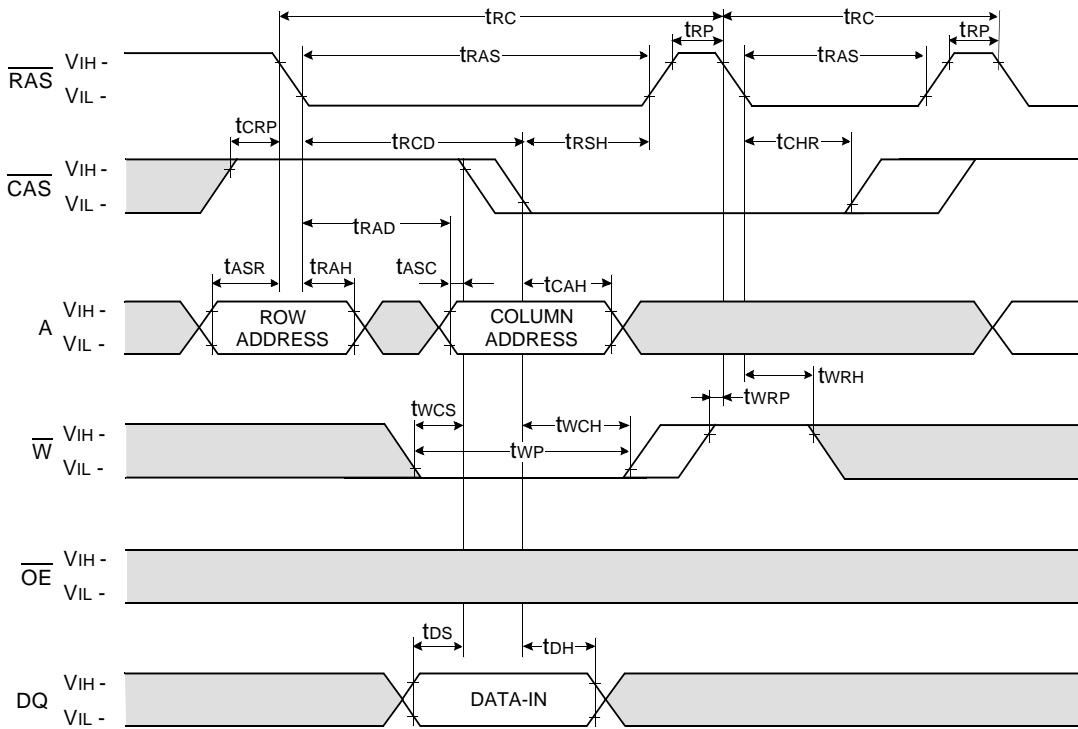
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DRAM MODULE

M53231600CE0/CJ0-C

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

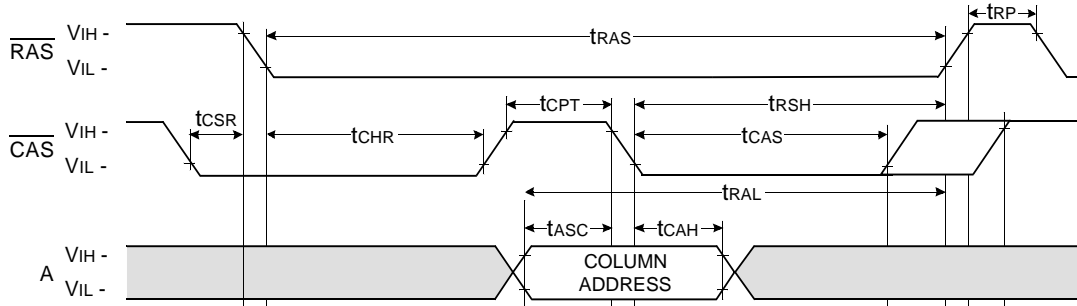


□ Don't care
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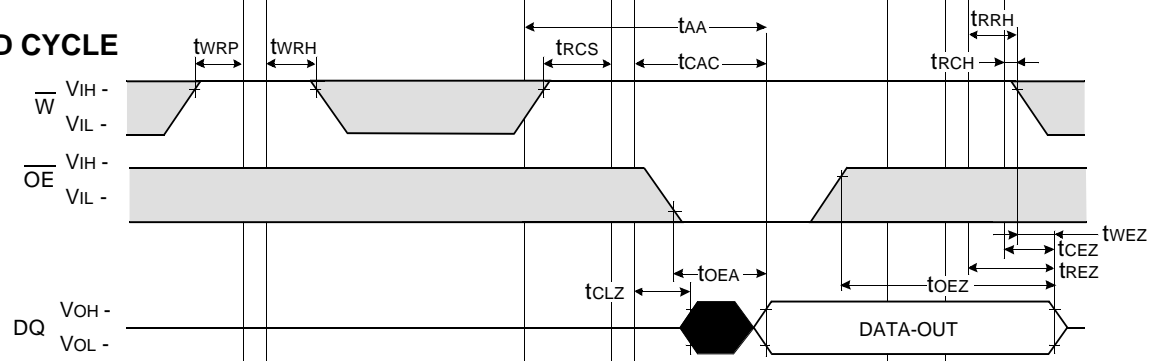
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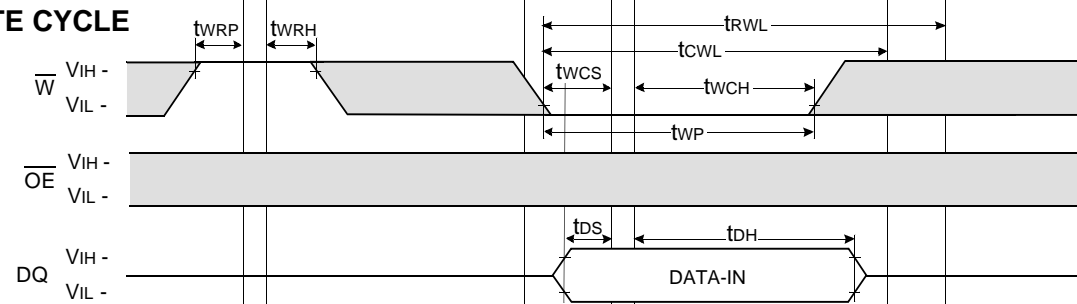
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



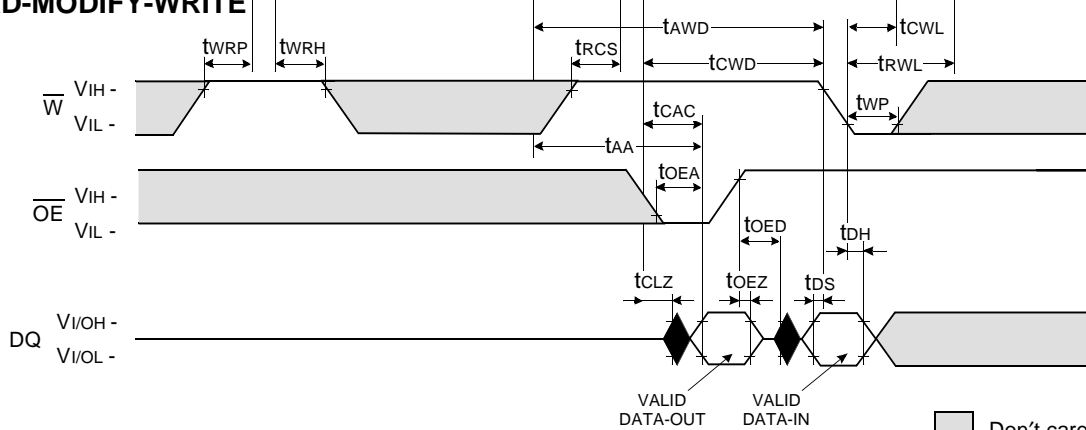
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

Don't care
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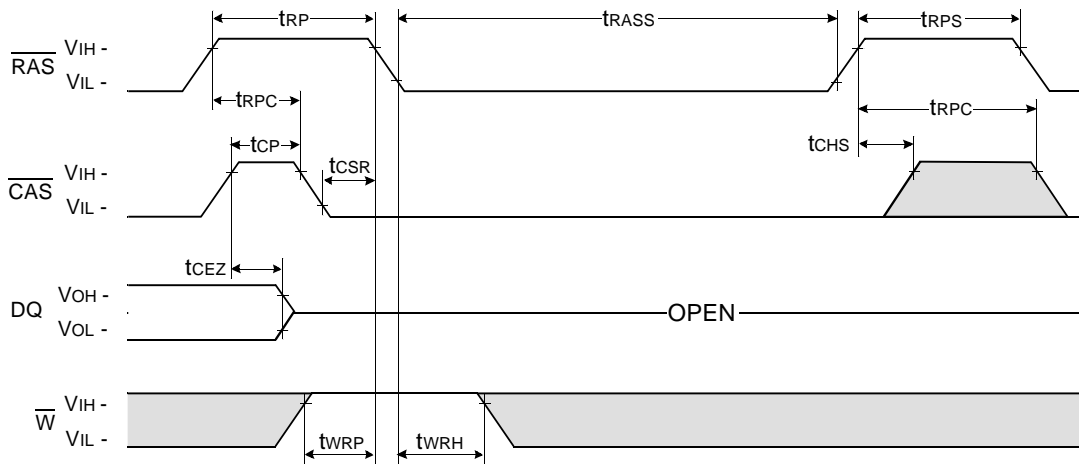
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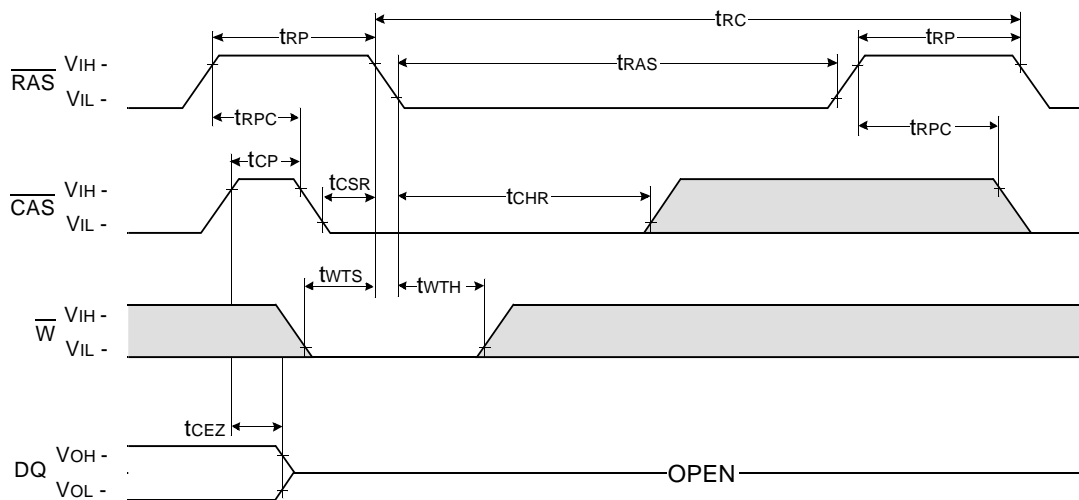
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care



TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care



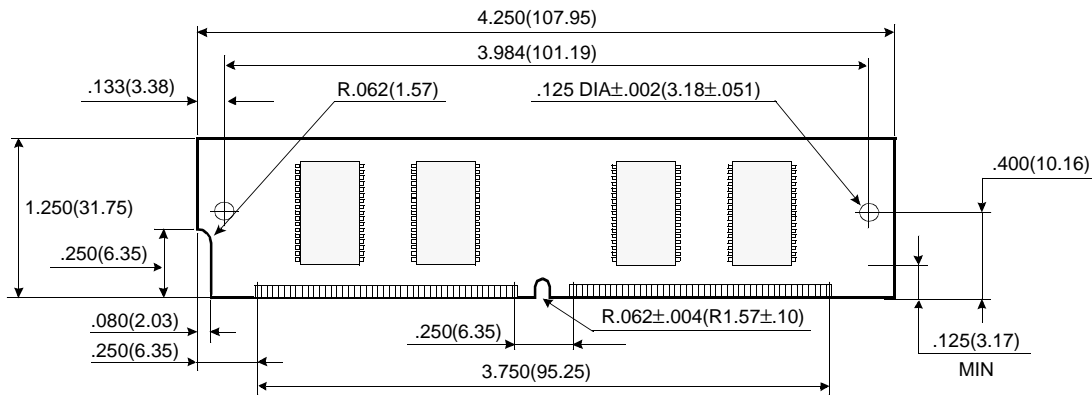
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DRAM MODULE

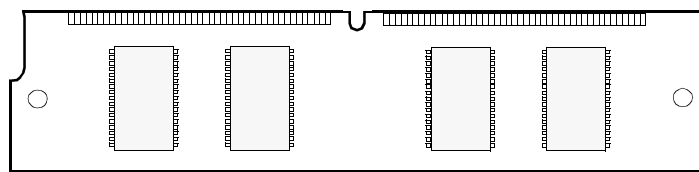
M53231600CE0/CJ0-C

PACKAGE DIMENSIONS

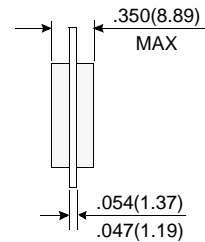
Units : Inches (millimeters)



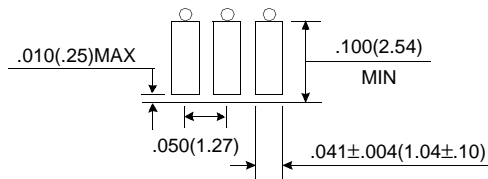
(Front view)



(Back view)



Gold/Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 16Mx4 DRAM, SOJ
DRAM Part No. : M53231600CE0/CJ0 -- K4E640411C