

DRAM MODULE

M53620800CW0/CB0 & M53620810CW0/CB0 with Fast Page Mode
8M x 36 DRAM SIMM using 4Mx4 and 16M Quad CAS, 4K/2K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M5362080(1)0C is a 8Mx36bits Dynamic RAM high density memory module. The Samsung M5362080(1)0C consists of sixteen CMOS 4Mx4bits DRAMs in 24-pin SOJ package and two CMOS 4Mx4 bit Quad CAS DRAM in 28-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M5362080(1)0C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t _{RAC}	t _{CAC}	t _{RC}
-50	50ns	13ns	90ns
-60	60ns	15ns	110ns

FEATURES

- Part Identification
 - M53620800CW0-C(4096 cycles/64ms Ref, SOJ, Solder)
 - M53620800CB0-C(4096 cycles/64ms Ref, SOJ, Gold)
 - M53620810CW0-C(2048 cycles/32ms Ref, SOJ, Solder)
 - M53620810CB0-C(2048 cycles/32ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	V _{ss}	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	$\overline{\text{V}}_{\text{ss}}$
4	DQ1	40	$\overline{\text{CAS}}_0$
5	DQ19	41	$\overline{\text{CAS}}_2$
6	DQ2	42	$\overline{\text{CAS}}_3$
7	DQ20	43	$\overline{\text{CAS}}_1$
8	DQ3	44	$\overline{\text{RAS}}_0$
9	DQ21	45	$\overline{\text{RAS}}_1$
10	V _{cc}	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	V _{cc}
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	A11	65	DQ16
30	V _{cc}	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{\text{RAS}}_1$	69	PD3
34	$\overline{\text{RAS}}_0$	70	PD4
35	DQ26	71	NC
36	DQ8	72	V _{ss}

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs(4K Ref)
A0 - A10	Address Inputs(2K Ref)
DQ0 - DQ35	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS}}_0$, $\overline{\text{RAS}}_1$	Row Address Strobe
$\overline{\text{CAS}}_0$ - $\overline{\text{CAS}}_3$	Column Address Strobe
PD1 -PD4	Presence Detect
V _{cc}	Power(+5V)
V _{ss}	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	V _{ss}	V _{ss}
PD3	V _{ss}	NC
PD4	V _{ss}	NC

* Pin connection changing available

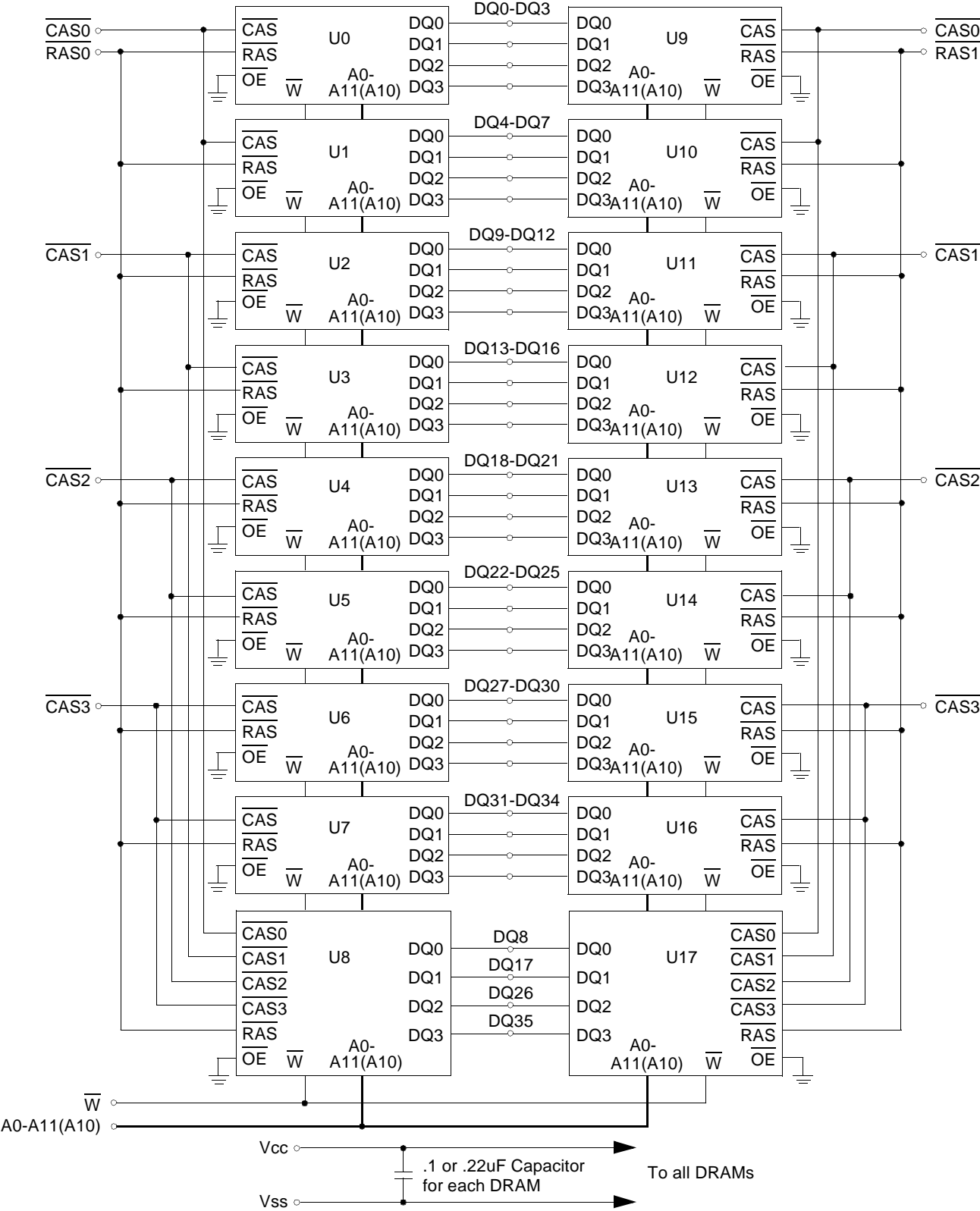
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* NOTE : A11 is used for only M53620800CW0/CB0 (4K ref.)



DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



DRAM MODULE

ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	18	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1 ^{*1}	V
Input Low Voltage	V _{IL}	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}.

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53620800CW0/CB0		M53620810CW0/CB0		Unit
		Min	Max	Min	Max	
I _{CC1}	-50	-	828	-	1008	mA
	-60	-	738	-	918	mA
I _{CC2}	Don't care	-	36	-	36	mA
I _{CC3}	-50	-	828	-	1008	mA
	-60	-	738	-	918	mA
I _{CC4}	-50	-	738	-	828	mA
	-60	-	648	-	738	mA
I _{CC5}	Don't care	-	18	-	18	mA
I _{CC6}	-50	-	828	-	1008	mA
	-60	-	738	-	918	mA
I _{I(L)}	Don't care	-90	90	-90	90	uA
I _{O(L)}		-10	10	-10	10	uA
V _{OH}	Don't care	2.4	-	2.4	-	V
V _{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$)

I_{CC3} : $\overline{\text{RAS}}$ Only Refresh Current * ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ cycling @trc=min)

I_{CC4} : Fast Page Mode Current * ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$ Address cycling : tpc=min)

I_{CC5} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$)

I_{CC6} : CAS-Before-RAS Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0\leq\text{V}_{\text{IN}}\leq\text{V}_{\text{CC}}+0.5\text{V}$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0\text{V}\leq\text{V}_{\text{OUT}}\leq\text{V}_{\text{CC}}$)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{\text{RAS}}=\text{V}_{\text{IL}}$. In I_{CC4}, address can be changed maximum once within one page mode cycle, tpc.



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CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	110	pF
Input capacitance[W]	CIN2	-	130	pF
Input capacitance[RAS0, RAS1]	CIN3	-	80	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	40	pF
Input/Output capacitance[DQ0-35]	CDQ	-	25	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Access time from RAS	tRAC		50		60	ns	3,4
Access time from CAS	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
CAS to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	ns	6
Transition time(rise and fall)	tT	3	50	3	50	ns	2
RAS precharge time	tRP	30		40		ns	
RAS pulse width	tRAS	50	10K	60	10K	ns	
RAS hold time	tRSH	13		15		ns	
CAS hold time	tCSH	50		60		ns	
CAS pulse width	tCAS	13	10K	15	10K	ns	
RAS to CAS delay time	tRCD	20	37	20	45	ns	4
RAS to column address delay time	tRAD	15	25	15	30	ns	10
CAS to RAS precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		10		ns	
Column address to RAS lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		ns	8
Read command hold time referenced to RAS	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to RAS lead time	tRWL	13		15		ns	
Write command to CAS lead time	tCWL	13		15		ns	
Data-in set-up time	tDS	0		0		ns	9
Data-in hold time	tDH	10		15		ns	9
Refresh period (4K Ref)	tREF		64		64	ms	
Refresh period (2K Ref)	tREF		32		32	ms	
Write command set-up time	tWCS	0		0		ns	7
CAS setup time(CAS-before-RAS refresh)	tCSR	5		5		ns	
CAS hold time(CAS-before-RAS refresh)	tCHR	10		10		ns	
RAS precharge to CAS hold time	tRPC	5		5		ns	



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AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{IH}/V_{IL}=2.4/0.8V, V_{OH}/V_{OL}=2.4/0.4V, Output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35	ns	3
Fast page mode cycle time	tPC	35		40		ns	
$\overline{\text{CAS}}$ precharge time(Fast page cycle)	tCP	10		10		ns	
$\overline{\text{RAS}}$ pulse width(Fast page cycle)	tRASP	50	200K	60	200K	ns	
W to $\overline{\text{RAS}}$ precharge time(C-B-R refresh)	tWRP	10		10		ns	
W to $\overline{\text{RAS}}$ hold time(C-B-R refresh)	tWRH	10		10		ns	
$\overline{\text{CAS}}$ precharge(C-B-R counter test)	tCPT	20		20		ns	
Hold time $\overline{\text{CAS}}$ low to $\overline{\text{CAS}}$ high	tCLCH	5		5		ns	11

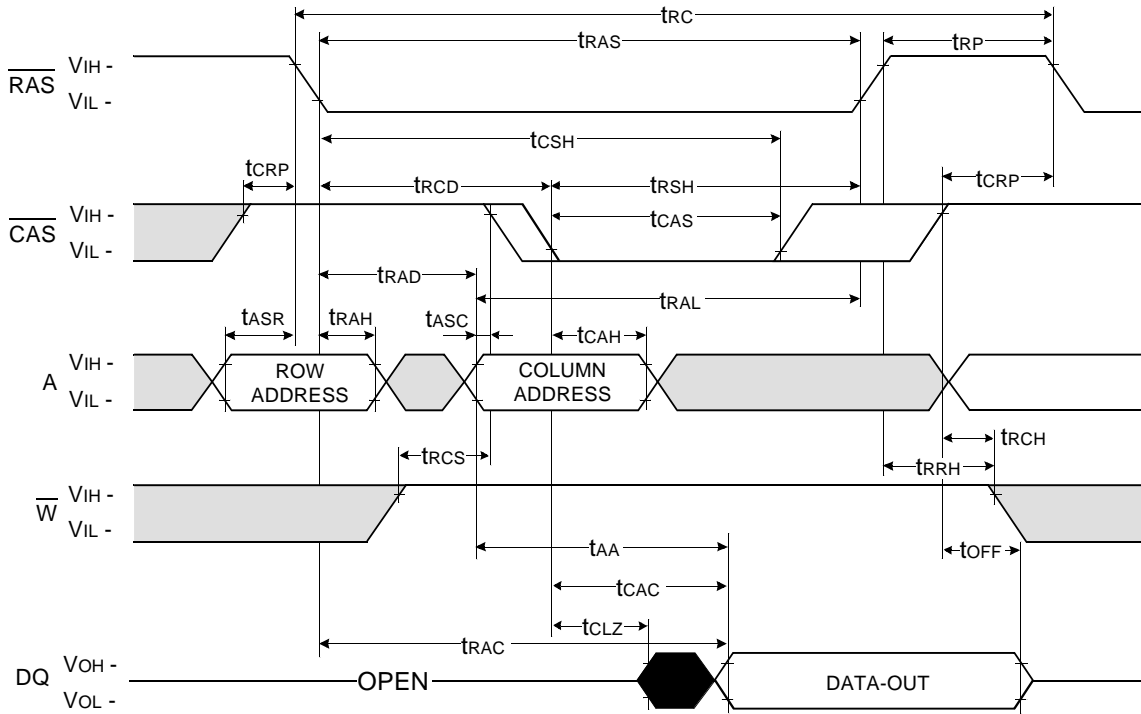
NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RC}D(max) limit insures that t_{RC}A(max) can be met. t_{RC}D(max) is specified as a reference point only. If t_{RC}D is greater than the specified t_{RC}D(max) limit, then access time is controlled exclusively by t_{CA}C.
5. Assumes that t_{RC}D≥t_{RC}D(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. twcs is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥twcs(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RC}H or t_{RR}H must be satisfied for a read cycle.
9. These parameter are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
10. Operation within the t_{RA}D(max) limit insures that t_{RC}A(max) can be met. t_{RA}D(max) is specified as reference point only. If t_{RA}D is greater than the specified t_{RA}D(max) limit, then access time is controlled by t_{AA}.
11. In order to hold the address latched by the first $\overline{\text{CAS}}$ going low, the parameter t_{CL}CH must be met.



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READ CYCLE

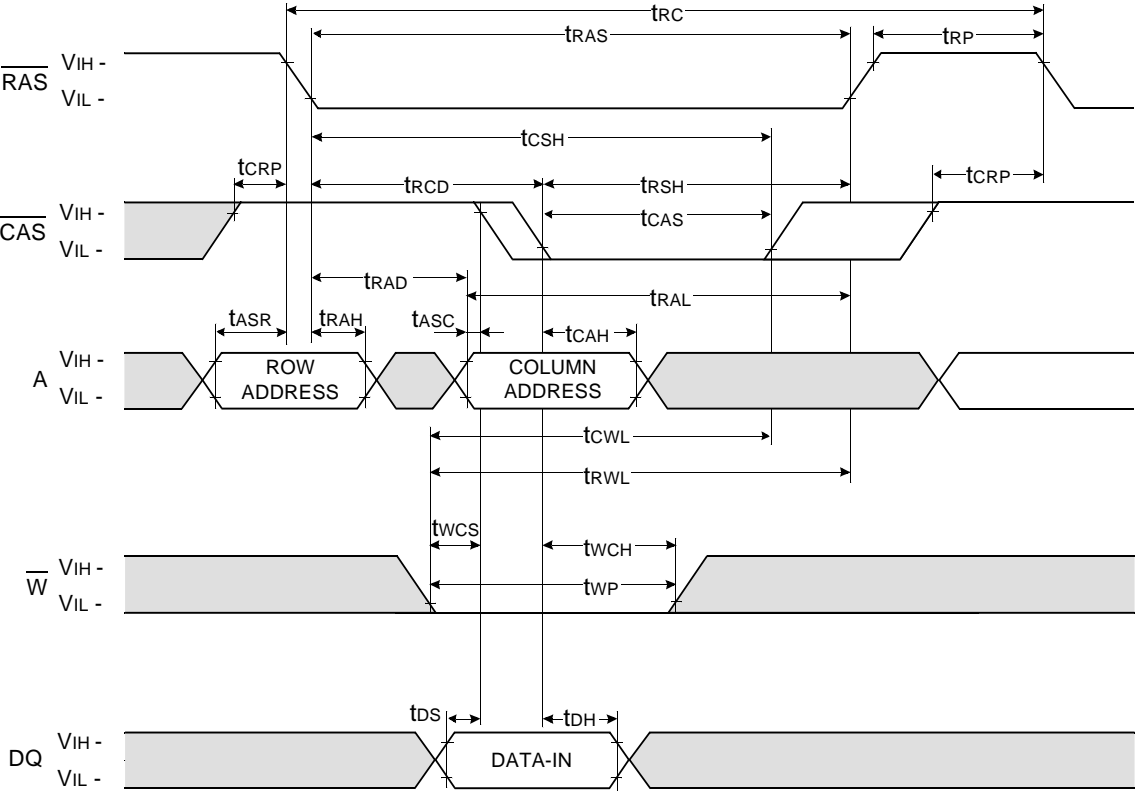


□ Don't care
■ Undefined

DRAM MODULE

WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



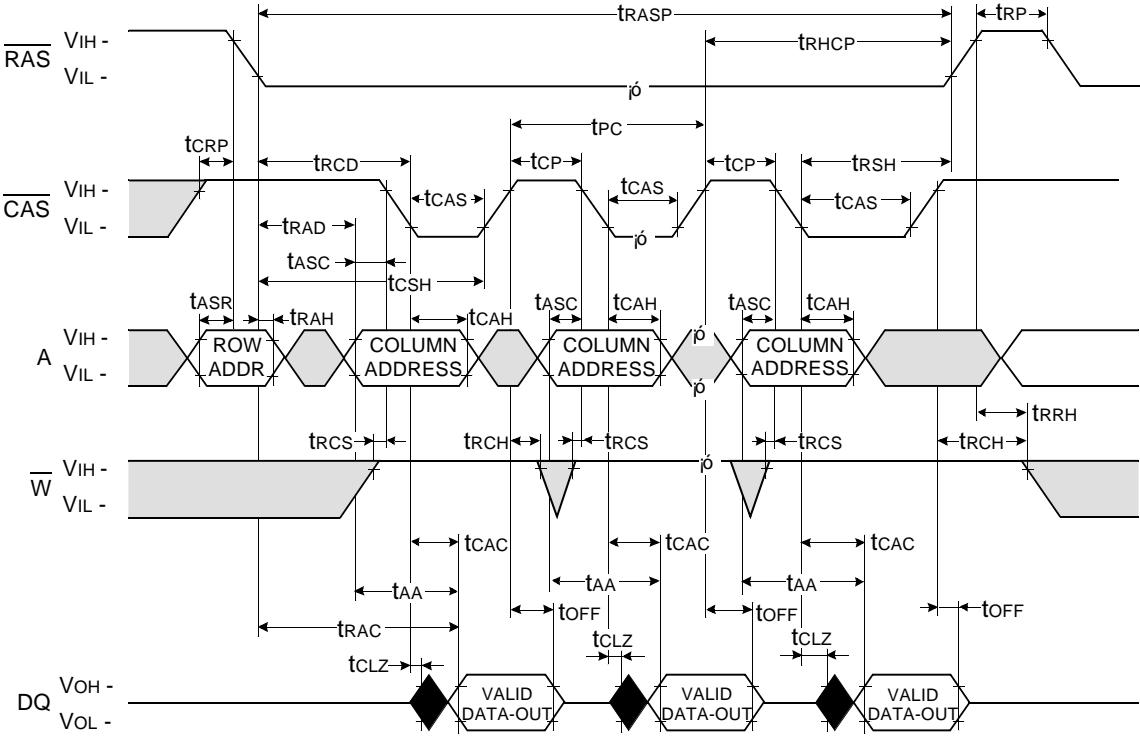
□ Don't care
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DRAM MODULE

FAST PAGE READ CYCLE

NOTE : DOUT = OPEN

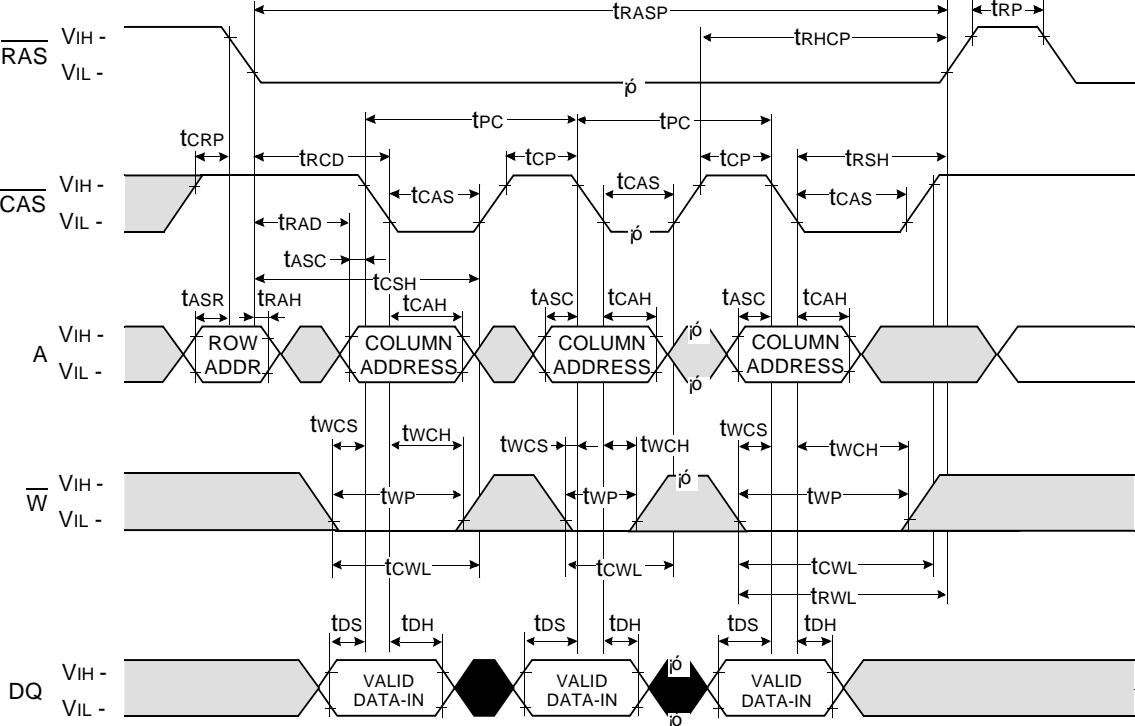


Don't care
Undefined

DRAM MODULE

FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care
■ Undefined

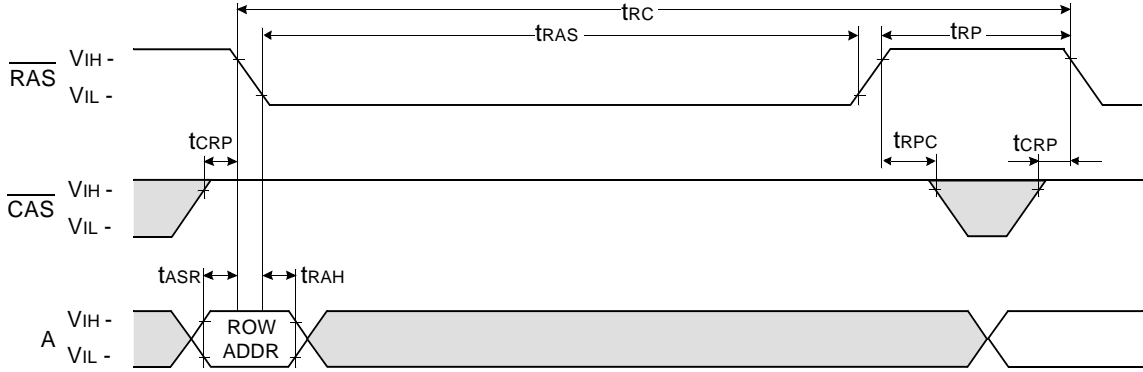


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RAS - ONLY REFRESH CYCLE

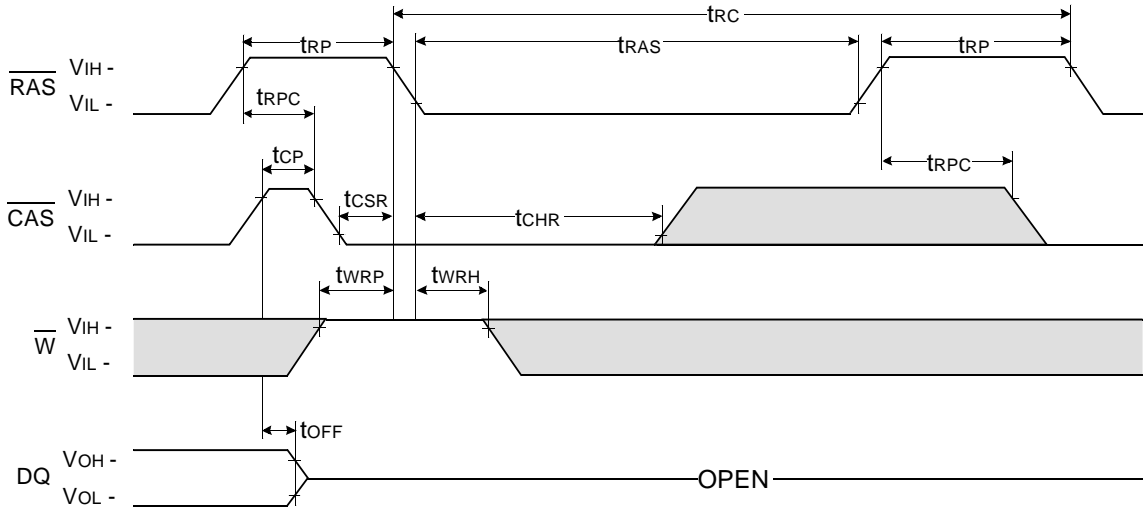
NOTE : \overline{W} , \overline{OE} , DIN = Don't care

DOUT = OPEN



CAS - BEFORE - RAS REFRESH CYCLE

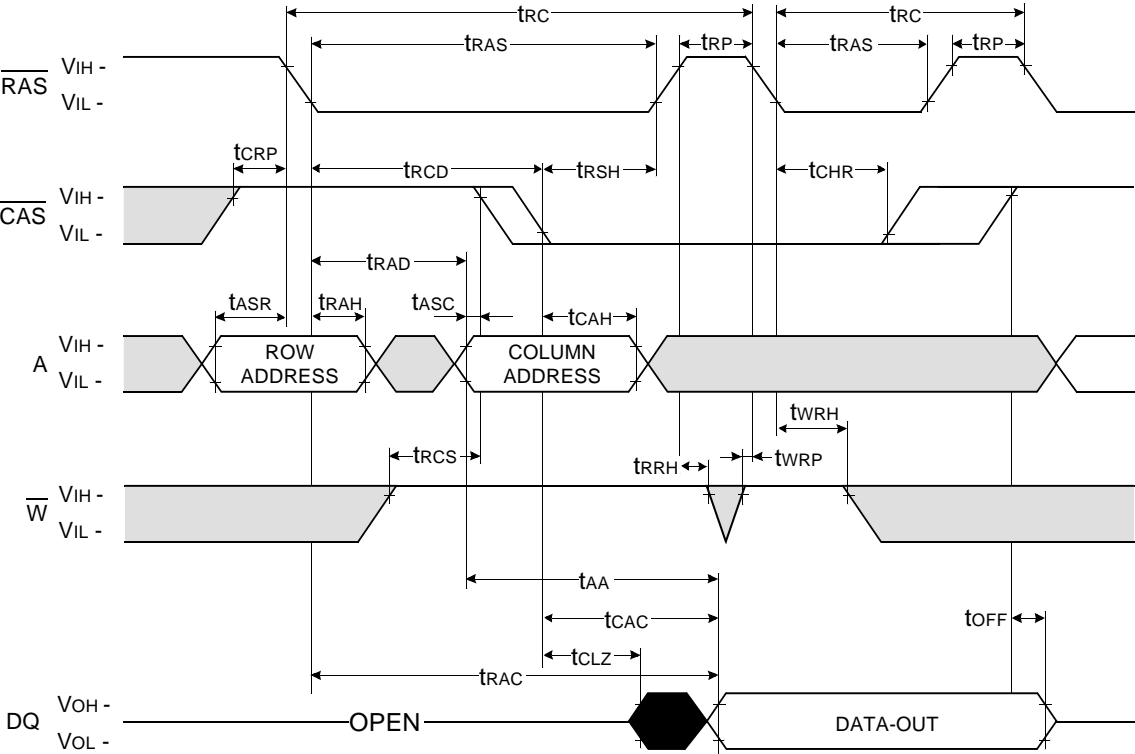
NOTE : \overline{OE} , A = Don't care



□ Don't care
■ Undefined

DRAM MODULE

HIDDEN REFRESH CYCLE (READ)

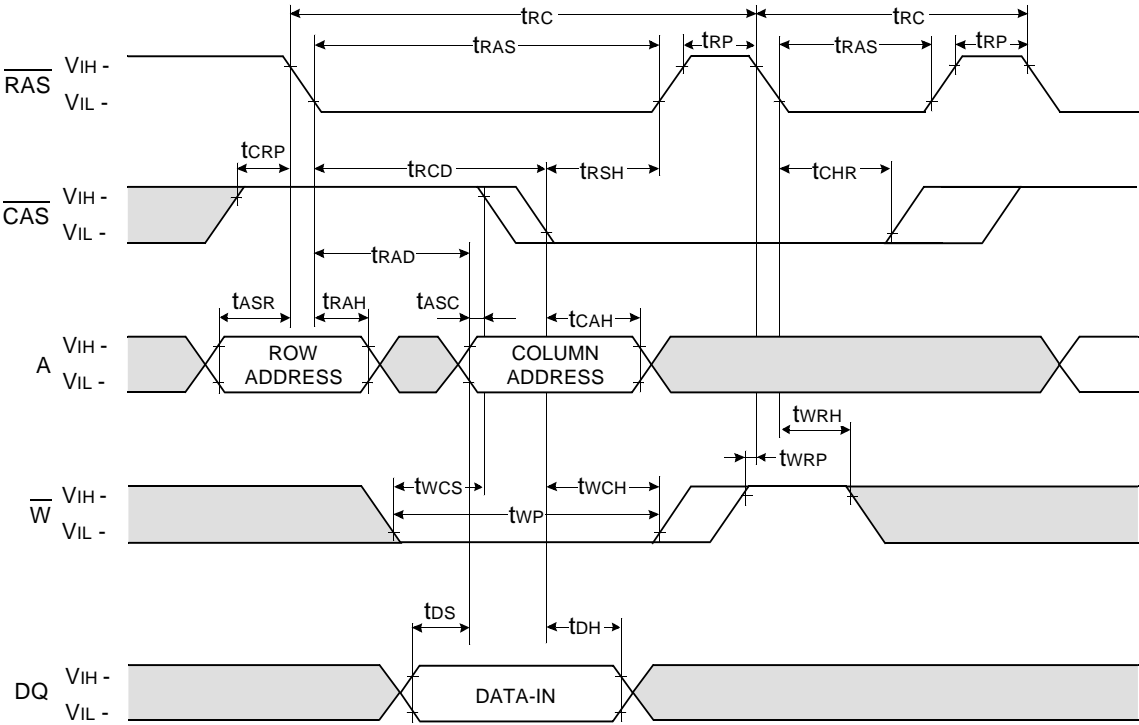


□ Don't care
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DRAM MODULE

HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN

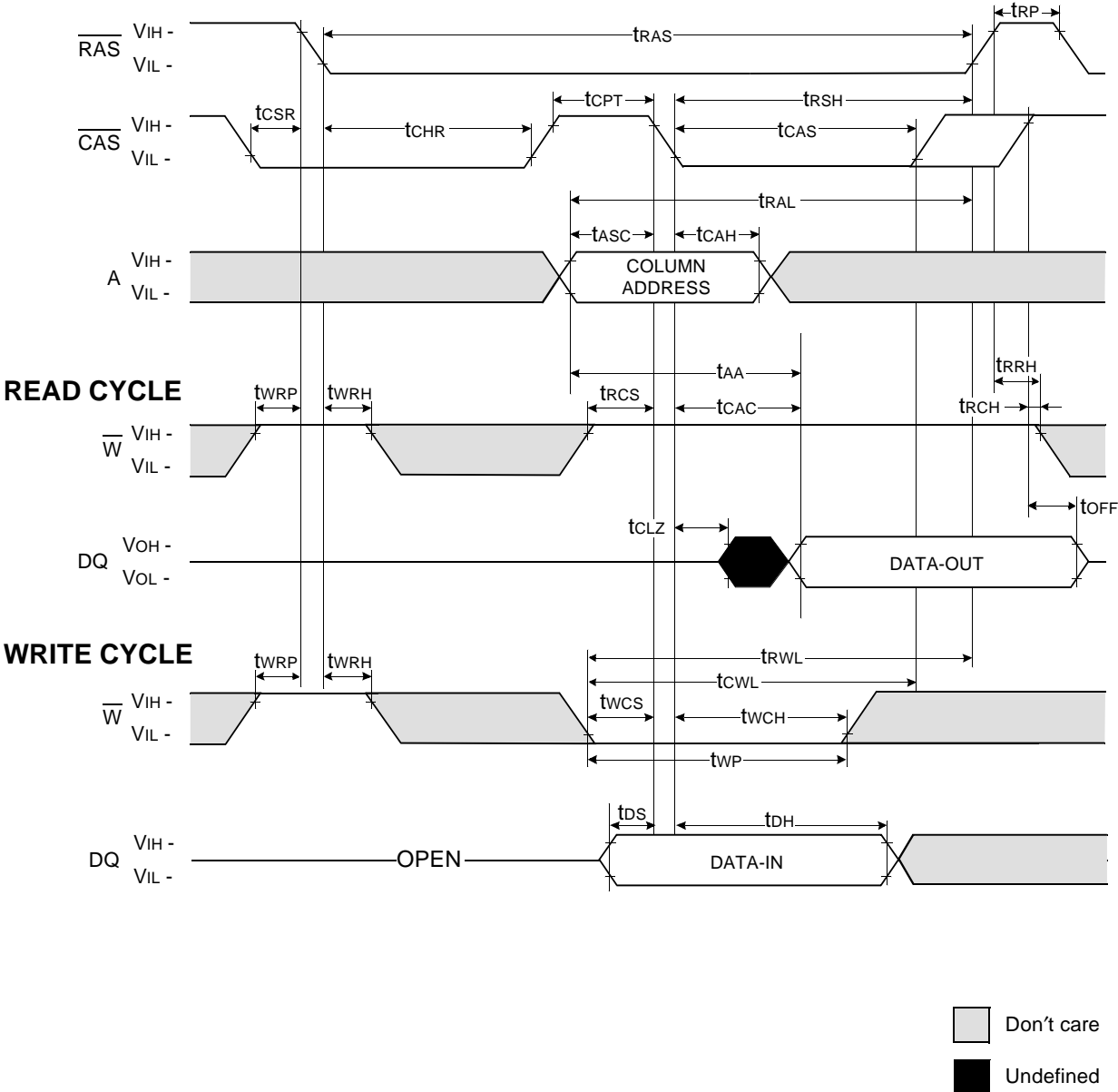


□ Don't care
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DRAM MODULE

CAS-BEFORE-RAS REFRESH CYCLE



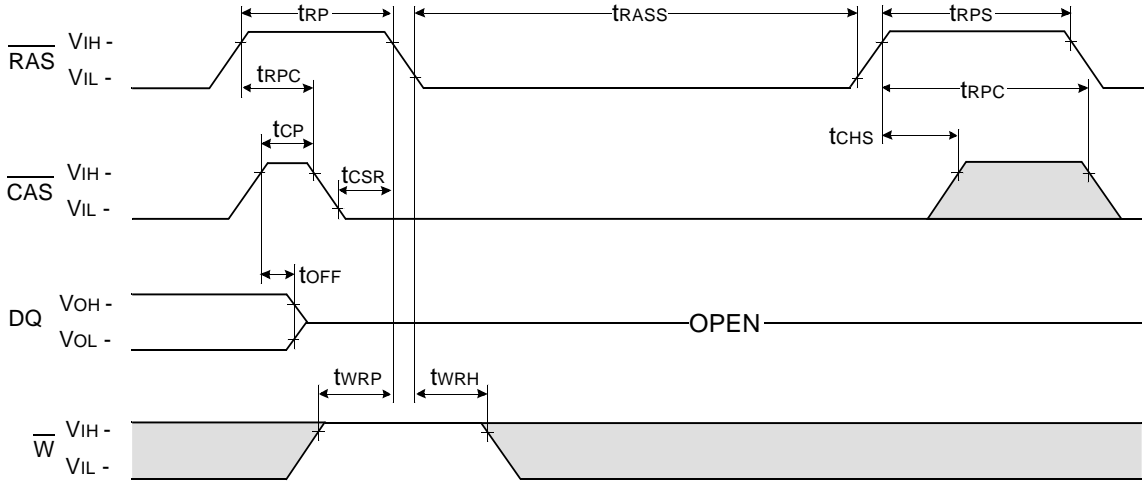
NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.



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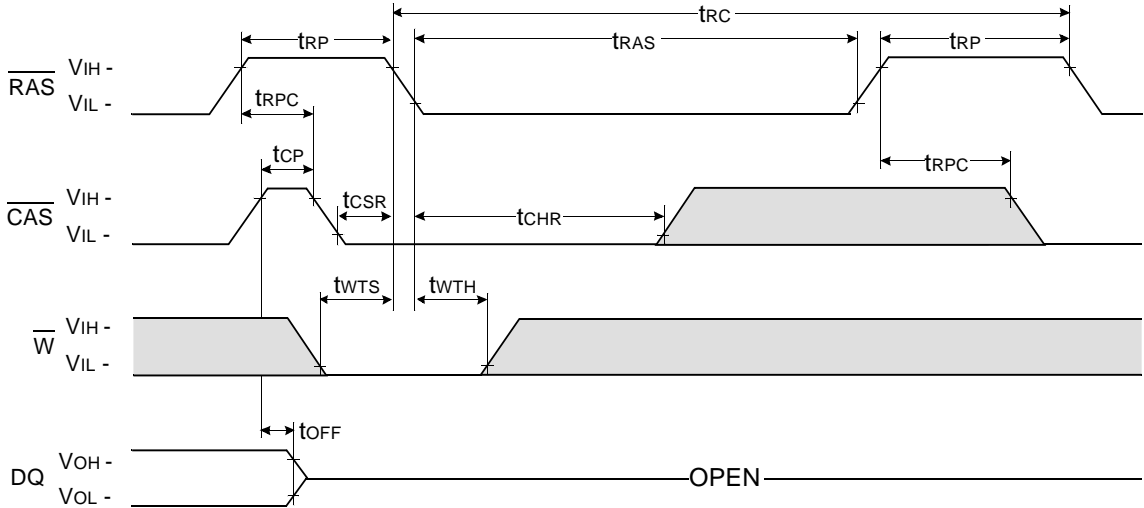
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : OE, A = Don't care



TEST MODE IN CYCLE

NOTE : OE, A = Don't care



□ Don't care
■ Undefined



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